

# MOS Models: Comments: On Analytic And Calculator-Aided Design Suitability

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## ABSTRACT:

Some present MOS static models are put into the same format and discussed with respect to the need of accurate analytic characterizations and suitability for pocket calculator aided design. Attention is called to the advantages of the simple model of Kohli.

## 1. INTRODUCTION:

The versatility of MOS transistors is now well recognized and, as a consequence, with more and more applications good models become more and more important. To be sure there are a number of models [1] - [13]. Some of these are extremely good for describing the effects of processing, and, as such, are especially good for layout and individual transistor design [2] [9]. Others are particularly useful for computer-aided analysis of integrated circuits especially of large scale designs [8] [11]. However, more recently a new class of models has appeared which essentially curve fit the transistor characteristics [12] [13]. These latter models have, as one editor has remarked, stirred some controversy, apparently because the need for them is not felt at the processing or even computer-aided design level. Here we discuss their need for analytic manipulations, packaged chip usage, and calculator-aided design work. We limit our treatment to the static triode characteristics of n-channel devices having constant  $V_T$  (fixed substrate bias) and operating with nonnegative drain - source voltage.

## 11. DISCUSSION ON THE MODELS

Probably the most quoted and used model is that of Shichman-Hodges which actually contains some of the previous models as special cases. Consequently, for our purposes, discussion of earlier models can be concentrated on it.

### A. Shichman-Hodges Model [7]

Reasoning from the device physics and using an "indefinite admittance" type of approach (also used by Meyer [9]) the basic Shichman-Hodges model gives the drain current,  $i_d$ , as

$$i_d = S(x) - S(y) \quad (1a)$$

$$\begin{aligned} x &= v_g - v_s - V_T, \quad y = v_g - v_d - V_T \\ (v_{ds} = x - y \geq 0) \end{aligned} \quad (1b)$$

where

$$\begin{aligned} S(u) &= K_0 u^2 l(u), \quad l(.) \\ &= \text{unit step function} \end{aligned} \quad (1c)$$

and  $v_g$  = gate voltage,  $v_s$  = source-terminal voltage,  $v_d$  = drain-terminal voltage, all with respect to a fixed but arbitrary (indefinite ground) point,  $V_T$  threshold voltage and  $K_0$  = gain constant given in terms of layout and material constants ( $= \mu c w / 2L$ ). Although (1) is in very convenient form, our experience shows that a least squares fit to triode static curves of packaged MOS FET's (MC14007 and CA3600) gives no better than 10-30% accuracy. However, the use of (1) in determining CMOS pair amplifier gain gives infinite error in the gain at the normal quiescent operating point (the amplifier transfer characteristic origin) [14]. The situation is improved by using the modified form suggested by Shichman and Hodges

$$i_d = H(x, y) - H(y, x) \quad (2a)$$

$$H(u, v) = K_0 u^2 (1 + l |u - v|) l(u) \quad (2b)$$

Where  $x$  and  $y$  are again given by (1b) and  $l =$  drain-source coupling constant. Although the accuracy in matching experimental curves is somewhat improved (being about 8-30%) and derived CMOS pair gains do become finite, this model has a serious problem for analytical work due to its mathematical nonanalyticity arising from the absolute value term. Consequently, in performing optimizations where the second derivative is needed one is faced with using distributional results in handling resulting impulses, which of course are also not appropriate for a calculator. Note that when operating in the "resistive" region, both  $H(x, y)$  and  $H(y, x)$  are nonzero, a disadvantage for programming but a beautiful theoretical result since the constant current region, where only one of the H's is nonzero, is seen to determine the full characteristic.

### B. Taki Model [13]

Rather than proceed through material constants Taki has presented a curve fitting model which when expressed in our indefinite variables can take the form

$$i_d = T(x, y) \\ = [K_T x^2 \tanh \{ \alpha (x-y)/x \}] l(x) \quad (3)$$

where  $K_T$  and  $\alpha$  are empirical constants and again  $x$  and  $y$  are the voltage of (1b). This has the advantage of giving an extremely close fit to experimentally determined device curves; for the MC14007 and CA3600 transistors we found 1-5% accuracy. However, the tanh function, though programmable with extra key strokes, is not the most convenient for calculator-aided work nor for other analytic considerations (including differentiations)

### C. Kohli Model [12]

In her doctoral dissertation Kohli presented a very simple curve fitting model which when put in the indefinite frame work and using the above notations is

$$i_d = K(x, y) \\ = K_K x^2 [1 - \exp\{-k(x-y)/x\}] l(x) \quad (4)$$

where again  $K_K$  and  $k$  are empirically determined constants. Kohli's model has a simple analytic form, gives 3-15% accuracy in curve fitting, has only one term  $K(.,.)$ , and is readily keyed into a pocket calculator with memory. Note that the function has at most finite jumps when differentiating through the second derivative.

### III. SUMMARY

In summary, there is need for simple analytic models for MOS transistors such that packages of transistors can be accurately characterized for forthcoming circuits designed using them. Since these designs will more and more be made with calculators and will involve differential equations and optimizations, models that are most suited for these needs will become more and more important. To date the model of Kohli appears the best available for these purposes. Refinements of it, including incorporation of substrate bias effects, and means of determining the relevant constants using pocket calculators are presently available [15].

### REFERENCES

- [1] S. R. Hofstein and F. P. Heiman, "The Silicon Insulated Gate Field-Effect Transistor," Proceedings of the IEEE, Vol. 51, No. 9, September 1963, pp. 1190-1202.
- [2] C. J. Sah, "Characteristics of the Metal-Oxide-Semiconductor Transistors," IEEE Transactions on Electron Devices, Vol. ED-11, No. 7, July 1964, pp. 324-345.
- [3] R. Greene and T. Soldano, "Increasing the Accuracy of MOS Calculation," Proceeding of the IEEE, Vol. 53, No. 9, September 1965, pp. 1241-1242.
- [4] R. S. C. Cobbold, "MOS Transistor as a 4-Terminal Device" Electronics Letters, Vol. 2, No. 6, June 1966, pp. 189-190.
- [5] P. Richman, "Characteristics and Operation of MOS Field-Effect Devices," McGraw-Hill, New York, 1967.
- [6] B. D. Roberts and C. O. Harbourt, "Computer Models of the Field Effect Transistor," Proceedings of the IEEE, Vol. 55, No. 11, November 1967, pp. 1921-1929.
- [7] H. Shichman and D. A. Hodges, "Modeling and Simulation of Insulated-Gate Field-Effect Transistor Switching Circuits," IEEE Journal of Solid-State Circuits, Vol. SC-3, No. 3, September 1968, pp. 285-289.
- [8] D. Frohman-Bentchkowsky and L. Vadasz, "Computer-Aided Design and Characterization of Digital MOS Integrated Circuits," Journal of Solid-State Circuits, Vol. SC-4, No. 2, April 1969, pp. 57-64.
- [9] J. E. Meyer, "MOS Models and Circuits Simulation," RCA Review, Vol. 32, No. 1, March 1971, pp. 42-63.
- [10] F. A. Lindholm, "Unified Modeling of Field-Effective Devices," IEEE Journal of Solid-State Circuits, Vol. SC-6, No. 4, August 1971, pp. 250-259.
- [11] G. Merckel, J. Borel, and N. Z. Cupcea, "An Accurate Large-Signal MOS Transistor Model for Use in Computer-Aided Design," IEEE Transactions on Election Devices, Vol. ED-1 No. 5, May 1972, pp. 681-690.
- [12] C. K. Kohli, "An Integrable MOS Neuristor Line: Design, Theory and Extensions," Ph.D. Dissertation University of Maryland, April 1977.
- [13] T. Taki, "Approximation of Junction Field-Effect Transistor Characteristics by a Hyperbolic Function," IEEE Journal of Solid-State Circuits, Vol. SC-13, No. 5, October 1978, pp. 724-726.

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