Bias Voltage Variation of CMOS Amplifier Transfer Functions*

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Abstract:

The voltage transfer function and the cut-off frequency of a CMOS linear inverting amplifier are known, from experimental observations, to vary with the applied bias voltage. A theoretical derivation of this variation is presented in this paper. An expression for the CMOS amplifier small signal AC voltage transfer function is derived from an MOS transistor model characterized by a square - law - exponential functional equation. From the AC voltage transfer function, expressions for the magnitude of the DC voltage gain and the cut - off frequency are obtained as functions of the applied bias voltage in a form suitable for pocket calculator aided circuit analysis and design. The theoretical results are checked against experimental data.

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I. Introduction

It has been observed that the voltage transfer function of the CMOS linear inverting amplifier varies with the applied bias voltage [1]. This characteristic finds ready applications, for example, in the design of voltage tunable active-R filters [2, 3]. In this paper we theoretically derive an expression for the CMOS amplifier small signal AC voltage transfer function, from which the magnitude of the small signal DC voltage gain and the cut-off frequency are obtained as functions of the applied power supply (bias) voltage. The derivation uses exponential functions to model the static DC characteristics of the MOS transistors as described in references [4, 5]. The obtained functions are particularly suitable for evaluation by a programmable pocket calculator. A comparison of the theoretical and experimental data for the variation of the DC voltage gain versus the applied bias voltage and the cut-off frequency versus the applied bias voltage, is presented.

We start the derivation by determining in Section II, the high frequency equivalent circuit of the CMOS amplifier as seen at the

is used in Section III to derive the voltage transfer functions and the high-frequency cut-off for the amplifier. The theoretical and experimental data, for the variation of the DC voltage gain with respect to the applied bias voltage, is presented in Section IV, and the data for the variation of the cut-off frequency versus the applied bias voltage is presented in Section V. A discussion of the results follows in section VI.

II. High frequency equivalent circuit

The Symmetrically biased inverting linear CMOS amplifier circuit is shown in Figure 1. In order to derive the voltage transfer functions and the cut-off frequency for this amplifier we first determine the small signal high-frequency equivalent circuit for the amplifier as seen at the output terminals.

We characterize the MOSFET DC current-voltage relationship by the model described in reference [5]. When the substrate is shorted to the source, the MOSFET static characteristics take the form

$$I_D = f(x, y) \tag{1a}$$

$$f(x,y) = \frac{\beta x^2}{1+\alpha x^m}\left(1 - e^{-\frac{Ky}{x}}\right)1(x) \quad , 1(\cdot) = \text{unit step} \tag{1b}$$

$$x = V_{GS} - V_{TO} \tag{1c}$$

$$y = V_{DS} \tag{1d}$$

Where I_D, V_{GS}, V_{TO}, V_{DS} are positive for n-channel MOSFET and negative for P-channel MOSFET; I_D = drain current, V_{GS} = gate-source voltage, V_{DS} = drain-source voltage, V_{TO} = turn on voltage (constant); α, β, m, K are device constants determined experimentally [5]. Using the variables as defined on figure 1, with subscripts n and p indicating n-channel and p-channel model

for each of the MOSFETS in Figure 1 as:

$$I_{Dn} = \frac{\beta_n (V_i + V_{DD} - V_{Ton})^2 \left(1 - e^{-\frac{K_n [V_o + V_{DD}]}{[V_i + V_{DD} - V_{Ton}]}}\right)}{1 + \alpha_n (V_i + V_{DD} - V_{Ton})^{m_n}} \quad (2a$$

$$I_{Dp} = -\frac{\beta_p (V_i - V_{DD} + V_{Top})^2 \left(1 - e^{-\frac{K_p [V_o - V_{DD}]}{[V_i - V_{DD} + V_{Top}]}}\right)}{1 + \alpha_p (V_i - V_{DD} + V_{Top})^{m_p}} \quad (2$$

where the unit step $1(\cdot)$ has been set to unity for small signal operation region.

Using the small letters v_i, v_o, i_{dn}, i_{dp} to represent small signal variations of V_i, V_o, I_{Dn}, and I_{Dp} respectively, we linearize the model for small signal applications by taking the Taylor Series expansion of equations (2) about the operating point $V_i = V_o = 0$ to get

$$i_{dn} = g_{on} v_o + g_{mn} v_i \quad (3a)$$

$$i_{dp} = g_{op} v_o + g_{mp} v_i \quad (3b)$$

where $$g_{on} = \left.\frac{\partial I_{Dn}}{\partial V_o}\right|_{V_i = V_o = 0} = \quad (3c)$$

$$g_{mn} = \left.\frac{\partial I_{Dn}}{\partial V_i}\right|_{V_i = V_o = 0} = \quad (3d)$$

$$g_{op} = \left.\frac{\partial I_{DP}}{\partial V_o}\right|_{V_i = V_o = 0} = \qquad (3e)$$

$$g_{mp} = \left.\frac{\partial I_{DP}}{\partial V_i}\right|_{V_i = V_o = 0} = \qquad (3f)$$

Thus, for small signal applications, the static characteristics for each MOSFET as seen at the output terminals of the amplifier in Figure 1 can be modelled by a linear equivalent circuit consisting of a controlled current source and a conductance as given by equations (3). We introduce the dynamic element (Capacitors) to this controlled source model to get the high frequency equivalent circuit for each MOSFET. Replacing each MOSFET in Figure 1 by its equivalent circuit, we obtain the small-signal high-frequency linear equivalent circuit for the CMOS amplifier. as seen at the output terminals, which is shown in Figure 2.

We now use this equivalent circuit in the next section to derive the voltage transfer functions

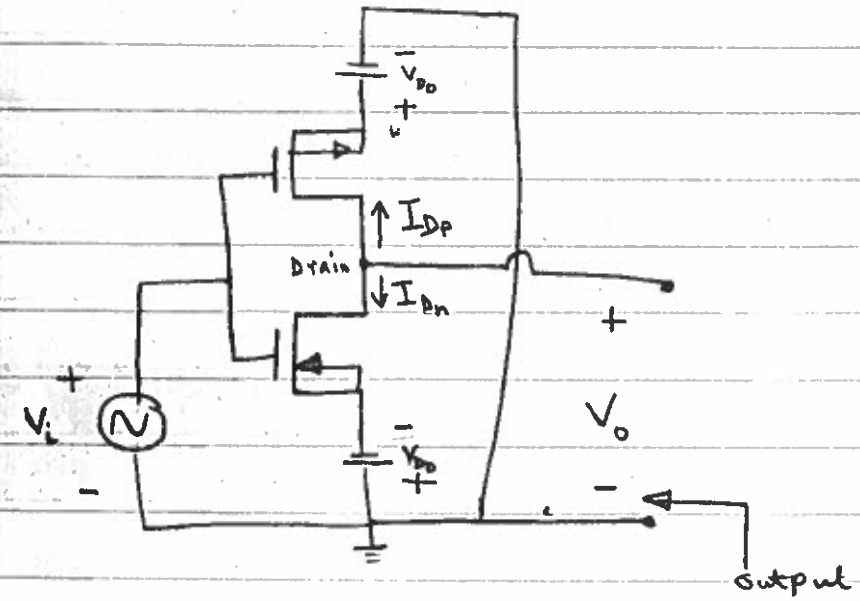

Figure 1. Symmetrically biased CMOS inverting Amplifie

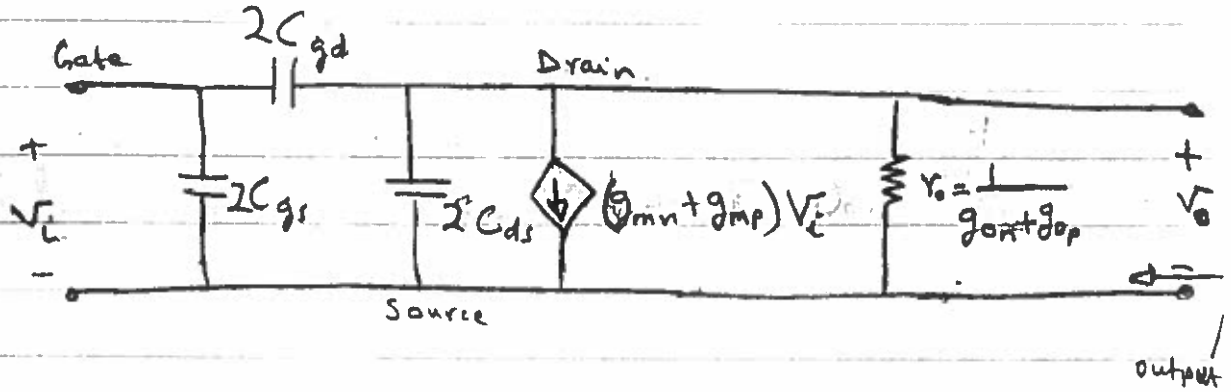

Figure 2.

Small Signal High-frequency equivalent circuit model for the CMOS amplifier, looking into output terminals. (C_{gs}, C_{gd}, and C_{ds} are gate-source, gate-drain, and drain-source capacitances, respectively).

VII. References

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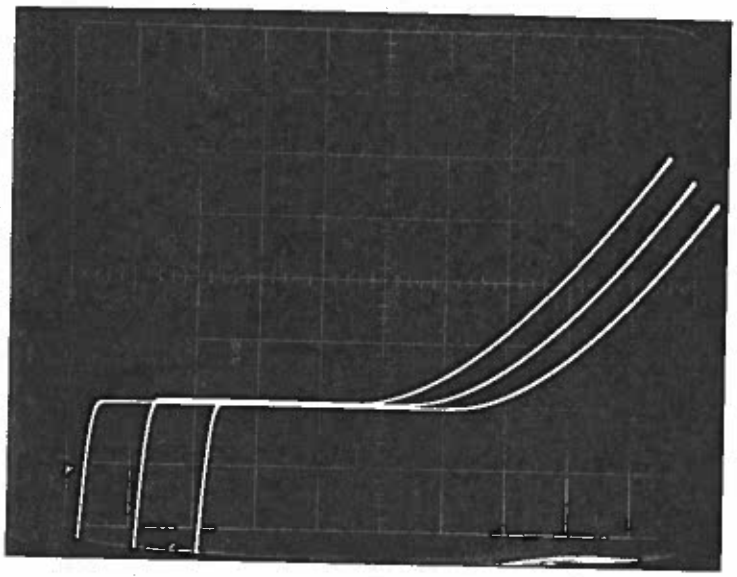
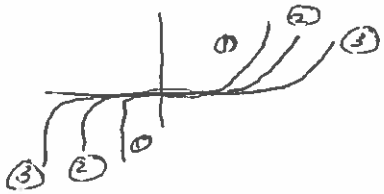


Hor: 1 v/div

Ver: 2 ma/div

CA3600E

n-channel



left curve (1)

$v_{BS} = 0$

(2) $v_{BS} = -1$

(3) $v_{BS} = -2$

$v = 0$ } 3 div from left most scale line

$i = 0$ } 2 div from bottom most scale line