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Direct-Coupled MOS Squaring Circuit

O. A. SERIKI AND R.W. NEWCOMB

Abstract—**A direct-coupled MOS squaring circuit is presented and discrete circuit test results are given. A version of the basic circuit uses one linear resistor while another is an all-MOS circuit. In both cases, limitations on input amplitude are obtained to ensure the squaring behavior.**

I. INTRODUCTION

In the fields of communication systems, analog computation, noise investigation and measurement of power in complex waveforms, several required functions can be realized through analog multiplier circuits. Consequently, many techniques have been developed to perform analog multiplication [1]. One of these schemes is the quarter-square multiplier, which utilizes two squaring circuits to obtain the product of two input variables.

To realize such a squaring circuit, the nonlinear characteristics of some device must be exploited. For example, the exponential nature of the voltage-current characteristics of the junction diode or the bipolar transistor has been used [2], [3] resulting generally in complex circuits. Of particular interest because of the almost ideal square-law behavior in much of the saturation region of MOS transistor operational characteristics, is the possibility of designing squaring circuits to a high degree of accuracy using MOS transistors [4]. In the published circuits, however, the output and the circuit interconnections are capacitor-coupled in order to overcome biasing problems.

In this paper we describe a direct-coupled MOS transistor circuit. This uses one resistor which can be a linear one or an MOS transistor connected as a resistor which allows extension of the circuit to an all MOS structure, thus making it much easier to produce in an integrated circuit form.

II. THE BASIC CIRCUIT

The basic circuit shown in Fig. 1(a) is a two-stage arrangement. The first stage consisting of equal transistors M_1, M_2, and M_3 (here all chosen n-channel) is a linear amplifier with

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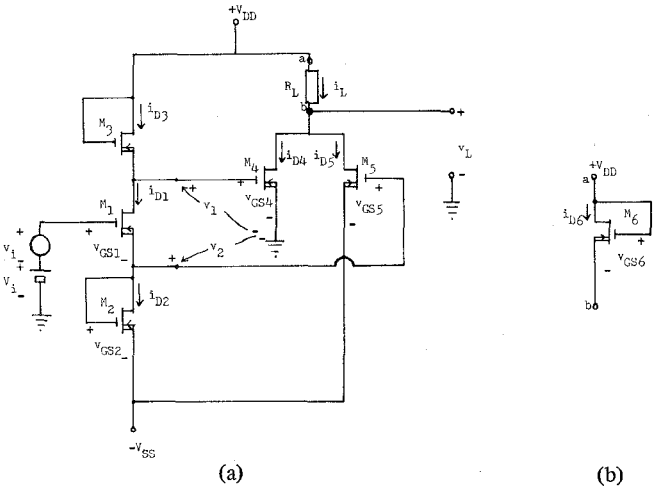

(a) (b)

Fig. 1. Basic squaring circuit. (a) With linear resistor R_L. (b) MOS replacement of R_L for all-MOS circuit.

output voltage v_1 and v_2 measured with respect to ground, having their signal components the negative of each other. In the second stage, which does the squaring, the current i_L flowing through R_L is the sum of the drain currents, i_{D4} and i_{D5}, of two equal transistors M_4 and M_5, these latter currents being squares of shifted inputs when the transistors are properly biased.

To develop analytical results, we recall that if biased to operate in the square-law region, the drain current i_D of an n-channel MOS transistor is related to its gate-to-source voltage, v_{GS}, by [5, p. 59]

$$i_D = K(v_{GS} - V_T)^2 \tag{1}$$

where V_T is the transistor threshold voltage, K a constant of the transistor, and i_D is the instantaneous value of the total drain current. Here we take $i_D = I_D + i_d$ where I_D is the dc bias component and i_d is the signal component of current. Equation (1) also holds for a p-channel transistor where all parameters are taken negative. Given the dc bias value, V_i, of the signal source, the dc bias voltages V_{DD} and $-V_{SS}$ in Fig. 1(a) are chosen so that the transistors are to be biased to operate in the middle of the square-law saturation region. Since all transistors in the circuit are of the same type (here n-channel transistors are chosen for convenience), we can assume that they are well-matched. In other words, V_T and K are the same for all the transistors. And since (1) holds and the currents i_{D1}, i_{D2}, and i_{D3} flowing through the transistors are the same, the gate-to-source voltages v_{GS1}, v_{GS2}, and v_{GS3} are equal. Since $v_{GS1} + v_{GS2} = 2v_{GS1} = 2v_{GS2} = 2v_{GS3} = V_i + V_{SS} + v_i$, Kirchhoff's voltage law shows that the voltages v_1 and v_2 are given by

$$v_1 = V_{DD} - V_{GS3} = V_{DD} - \tfrac{1}{2}(V_i + V_{SS}) - \tfrac{1}{2}v_i \tag{2a}$$

$$v_2 = v_{GS2} - V_{SS} = \tfrac{1}{2}(V_i - V_{SS}) + \tfrac{1}{2}v_i. \tag{2b}$$

Hence, a signal v_i fed into the input of the first stage divides equally, but with opposite signs, between v_1 and v_2 to form the signal components of the voltages which control the gates of transistors M_4 and M_5 of the second stage.

The current i_L flowing through the resistor R_L is the sum of the drain currents i_{D4} and i_{D5}. Applying (1) to each of these second stage drain currents and writing $v_L = V_{00} + v_o$ for the output voltage with v_o, the signal component and V_{00}, the dc bias component, the total output voltage, v_L, is given by

$$v_L = V_{00} - KR_L(a_2 - a_1)\, v_i - \tfrac{1}{2}KR_L v_i^2 \tag{3}$$

where

$$a_1 = V_{DD} - \tfrac{1}{2}V_{SS} - \tfrac{1}{2}V_i - V_T \quad (4a)$$

$$a_2 = \tfrac{1}{2}V_{SS} + \tfrac{1}{2}V_i - V_T \quad (4b)$$

$$V_{00} = V_{DD} - KR_L(a_1^2 + a_2^2). \quad (4c)$$

As defined above, the first term, V_{00}, of (3) is the dc bias component of v_L, while the second term is a reproduction of the input signal v_i. Since this second term is not desired in the output of a squaring circuit, it contributes to the amount of distortion or error introduced by the circuit. The last term is an undistorted reproduction of the square of the input signal and this is the desired output signal. It is worth noting that the output has no other undesired harmonic present apart from the first, which can be reduced or eliminated completely by satisfying the condition

$$a_2 - a_1 = 0 \quad (5a)$$

which, from (4a) and (4b), is equivalent to the condition

$$V_{DD} = V_i + V_{SS}. \quad (5b)$$

Setting

$$a_1 = a_2 = a = \tfrac{1}{2}V_{DD} - V_T \quad (5c)$$

which is positive for the operation of our circuit, the signal component, v_o, and the dc bias component, V_{00}, of the output voltage are

$$v_o = -\tfrac{1}{2}KR_L v_i^2 \quad (6a)$$

$$V_{00} = V_{DD} - 2KR_L a^2 \quad (6b)$$

provided of course that the gate-to-source voltages of the output transistors, M_4 and M_5, are greater than the threshold voltage V_T. These threshold constraints come directly from (2a) [and equally (2b)] to give (using (5b) and (5c))

$$|v_i|_{\text{peak}} \leqslant 2a. \quad (6c)$$

The dc bias of the output voltage, V_{00}, can be set at a desired level by the proper choice of the circuit parameters in (6b) provided of course that the condition for the operation of the transistors in the square-law region is maintained, which is done by choosing R_L along with V_{SS}, V_{DD} then being given by (5b).

If the resistor R_L of Fig. 1(a) is replaced by a "resistor connected" MOS transistor, an all MOS squaring circuit results, with the replacement as shown in Fig. 1(b). Using $v_{GS6} = V_{DD} - v_L$ and assuming M_6 identical to M_4 and M_5, in which case $i_{D6} = K(v_{GS6} - V_T)^2$, the expression for the voltage output from Fig. 1(b) is determined as before and gives the equation

$$v_L - (2a_3)^{-1}v_L^2 = (2a_3)^{-1}(a_3^2 - a_1^2 - a_2^2) - (2a_3)^{-1}(a_2 - a_1)v_i - (4a_3)^{-1}v_i^2 \quad (7a)$$

where

$$a_3 = V_{DD} - V_T \quad (7b)$$

and a_1 and a_2 are as in (4). Now setting again $a_1 = a_2 = a$ and substituting $v_L = V_{00} + v_o$, (7a) gives

$$2(a_3 - V_{00})v_o - v_o^2 = [V_{00}^2 - 2a_3V_{00} + a_3^2 - 2a^2] - \tfrac{1}{2}v_i^2. \quad (7c)$$

On further setting the bracketed term of the right of (7c) to 0, we obtain

$$V_{00} = a_3 - 2^{1/2}a. \quad (8a)$$

Here the negative square root has been used since the positive one normally takes V_{00} above V_{DD}. In order to obtain a close approximation to a perfect square at the output of the circuit, the peak value of the term v_o must dominate that of v_o^2. Hence

$$|v_o|_{p-p} = |v_o|_{\text{peak}} >> |v_o^2|_{\text{peak}}/|2(a_3 - V_{00})| = (2^{3/2}a)^{-1}|v_o^2|_{\text{peak}}. \quad (8b)$$

Thus, the constraint

$$2^{3/2}a >> |v_o|_{p-p} \quad (8c)$$

which when satisfied leads, by (7c), to

$$v_o \approx -v_i^2/(4\sqrt{2}a). \quad (8d)$$

Using the output constraint of (8c) in (8d) gives

$$|v_i|_{\text{peak}} << 4a \quad (8e)$$

which shows a limitation on allowed inputs in the case of the "resistor connected" MOS load. Reasonably, in this case one could choose $|v_i|_{\text{peak}} \leqslant 4a/10$ and, thus, on comparing with (6c), we see that the dynamic range is about one-fifth of that when a linear resistor is used as a load.

From (5) and (6) or (8) a practical circuit can be designed for Fig. 1(a) or (b).

III. Experimental Results

The circuits of Fig. 1 were built using MOS transistor packages model MC14007CP with n-channel parameters K and V_T measured as 0.55 mA/V^2 and 2 V, respectively. Keeping (5b), the dc bias voltages were chosen as $V_{DD} = V_{SS} = 8$ V when $V_i = 0$. In order to obtain a reasonable voltage swing at the output, a 1 kΩ resistor was chosen for R_L. The dc bias voltages, V_{00}, measured at the outputs of both circuits (3.5 V for the linear resistor and 3.2 V for the MOS resistor) agree well with the calculated values from (6b) and (8a) (being 3.6 V and 3.17 V, respectively).

In Fig. 2(a) we illustrate the results for $4 = 2a > |v_i|_{\text{peak}} = 2 > 4a/10 = 0.8$, that is, well within the operating limits for the linear R_L circuit and pushing the MOS load case beyond its limits. In the linear R_L case, the peak (to peak) value of v_o, $|v_o|_{p-p}$, is 1.1 V which is in excellent agreement with the theoretical value calculated by (6a); note that since v_o is of one sign its peak value is also its peak-peak value. In the MOS load case, the same input (of 2 V peak) yields an output of about one-third the size, this being $|v_o|_{p-p} = 0.4$. Numerically the peak value of 0.4 V is checked quite accurately (to within 3 percent) using the full formula (7c). But since the assumption of $|v_i|_{\text{peak}} << 4a$ is violated, we expect some error in using (8d); we calculate an error of about 12 percent in using (8d), but note that Fig. 2(a_1) still shows that the circuit squares reasonably well. On reducing the input to $|v_i|_{\text{peak}} = 1.5$ V, we found that the error in using (8d) was below 0.6 percent.

As expected from (6a) and (8d), and seen by the above numbers, the gain coefficient of the linear resistor squarer can be made larger than that of the all MOS circuit, depending on the value of the linear resistor. The gain coefficient is larger by a factor of $KR_L 2^{1/2}(V_{DD} - 2V_T)$; for $R_L = 1$ kΩ, as used for the experiment of Fig. 2(a), this is a factor of 3.11 which agrees well with the experiment.

IV. Discussion

A direct-coupled MOS squaring circuit has been designed and tested. The results agree very well with what the design equations predict.

In the analysis of the basic circuit presented here it was assumed that all the transistors are well matched. Because only n-channel transistors of the same type were used in our experiments, this assumption was reasonably good for the

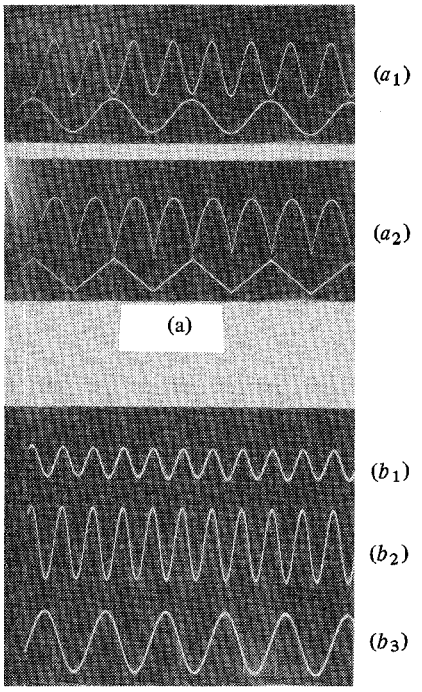

Fig. 2. Waveform response of circuits.
(a) Linear R_L circuit responses.
Vertical scales: 5 V/div. (input), 1 V/div. (output).
Horizontal scales: 0.1 ms/div.
(a_1) Sinusoidal input.
(a_2) Triangular input.
(b) Sinusoidal input responses.
Vertical scales: 2 V/div. (input), 0.5 V/div. (output).
Horizontal scales: 0.1 ms/div.
(b_1) All MOS circuit.
(b_2) Linear R_L circuit.
(b_3) Input.

circuit constructed. But actually, the theory and practice, directly extend to the case of unmatched transistors, the main change being a shift in constants obtained and the relation of V_{DD} to V_{SS} of (5b). Thus, the adjusting V_{SS} for a fixed V_{DD} and V_i, the circuit will square for a wide range of differences between transistors. One can of course use all p-channel, as well as a mixture of types of transistors. In this regard, we observe that in the test circuit of Fig. 1 the substrate of every transistor is connected to its source thereby avoiding the substrate modulation effect on V_T. Actually, by a proper combination of transistor types coupled with the adequate adjustment of V_{SS} for a fixed V_{DD} and V_i, the circuit could be made to operate quite well when all the transistors are fabricated on a single chip as in common CMOS technology. For example, using p-channel transistors for M_3 (and M_6 in the case of the all MOS circuit) and connecting their substrates to V_{DD} and using n-channel transistors for M_1, M_2, M_4, and M_5 and connecting their substrates to $-V_{SS}$ has experimentally given good results (with all other quantities as before, V_{SS} = 6 V was required rather than the 8 V used for the experiments reported in Section III).

The circuit with the linear resistor has a larger output voltage swing than the all-MOS transistor circuit. Because of the presence of v_o^2 in (7c), we can see that in general the linear resistor gives such a result, being a more accurate squarer over a larger range of inputs. It should be observed, too, that by equating V_i to V_{00}, values of parameters can be found for which the circuits can be directly cascaded. This may only allow physical realization for certain $V_i = V_{00}$ by the circuit given; for example $V_{00} = 0$ will not allow proper biasing of M_4. By inserting another supply at the source lead of M_4 this problem can of course be circumvented.

It should be commented upon that the adjustment to hold $a_1 = a_2$ for eliminating the term linear in v_i at (3) and (7a) is the crucial one. Practically this requires closely holding a relationship between V_{DD} and $V_{SS} + V_i$, as exhibited here by (5b). Experimentally, this can necessitate sensitive bias adjustments which, however, are conveniently controlled with just one of the bias sources. In practice, a desire for automatic control of this bias source would of course lead to a more complex circuit than that given here.

The potentiality of analog MOS large-scale integrated circuits has recently been demonstrated [6]. We believe that squaring circuits such as the ones presented here could have wide application in this area, particularly the all MOS version, if further investigated for adaptation to suit large-scale integration. In this connection, we note amidst others two particular requirements, the need to establish the conditions for squaring when the transistors are operated with source and substrate at different bias potentials, and the need for high precision auxiliary regulating circuits for the bias sources.

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Practical Optimization of Noise and Distortion in Sallen and Key Filter Sections

PETER J. BILLAM

Abstract–**This communication presents simple analytic formulas for the noise and distortion aggravation performance of Sallen and Key filter sections, under the approximation that the resistor noise contribution is small compared with the amplifier noise. This performance is optimized analytically and subject to component constraints.**

I. Noise

Noise in active filters has two main origins: the network resistors and the amplifiers. The analytical optimization used in this communication is made possible because in practical cir-

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