MOS Neuristor Lines†

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An MOS-RC line is considered which has all the properties of neuristors, as defined by Crane. For this the nonlinear diffusion equations describing distributed structures are derived and discussed. Experimental evidence is presented as well as extensions.

Voy a nombrar las cosas, los sonoros
Altos que ven el festejar del viento [1].

1. INTRODUCTION

In his Ph.D. dissertation Crane [2, 3] introduced the concept of the neuristor, this being [2, p. iii] "defined as a device having the form of a one-dimensional channel along which signals may flow, the signals taking the form of propagating discharges having the following properties: 1. Threshold of stimulability, 2 uniform velocity of propagation, 3. attentuationless propagation, 4. refractory period following the passage of a discharge, after which the neuristor can support a discharge." At the time, although various possibilities were put forth, no physical realizations existed in electronic form, and, thus, the name "heuristor" was coined [4].

However, as the concept became known, a number of electronic realizations appeared [5–26] as well as characterizations of such and related electronic schemata [27–56]. And, since the neuristor, by its definition above, possesses many of the properties of nerve axons and cells, their various models [57–81] are neuristor-like devices. It should be emphasized, though, that the neuristor was conceived not as a model of the nerve axon but as a device for computer construction, for which it has been shown capable of carrying out all digital logic functions [2, 82–84]. Consequently, to be useful in the context of computer construction, neuristors compatible with large scale integrated circuit technology should be available; this is the major shortcoming associated with all of the devices and models referenced above.

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With this in mind, under the joint Polish–American "Active Microelectronic Systems" program, Dr. Wilamowski and his colleagues developed a bipolar transistor RC neuristor line [85, 86] fully compatible with standard integrated circuit technology. A slightly different circuit was developed using CMOS (complementary metal oxide silicon) technology on the American side of the program [87] where the possibility of frequency coding of repetitive neuristor pulses was observed [88, 89] and checked on the Polish circuit [90]. Therefore, these and similar circuits merit further investigation in which case we here discuss a closer variant of the Polish circuit using CMOS devices, giving primarily experimental evidence to support its operation.

Con la mirada inmóvil del verano
Mi cariño sabrá de las veredas [1].

2. CIRCUITS

In the following paragraph we introduce the basic neuristor circuit we wish to discuss here, giving physical reasoning on its operation and experimental verification of its important properties. From these some valuable extensions are put forth.

2.1. Basic Circuit

The basic circuit to be introduced here is shown in Fig. 1 which represents a cascade of identical sections beyond the source. Each section of Fig. 1 is to be considered as a passive $R_l - C_l$ two-port "line" section with an active, nonlinear, and (most importantly) dynamic one-port load across its second port. For comparison one section of the circuit of Wilamowski *et al.* [85] from which it stems is shown in Fig. 2; as can be seen the major difference is the substitution of the MOS transistors for the bipolar ones. In Fig. 1 the connection node numbers are those of the pins on the MC-14007CP, CMOS transistor, package used for all experimental verifications given in this paper. Figure 3 shows typical pulses obtained experimentally, as discussed below, the top trace being the periodic input voltage, with negative pulses, and the bottom trace being the line voltage response at pin 3 of the fifth section of an eight section line of the form of Fig. 1.

The principle of operation is quite similar to that for Fig. 2 and will now be reviewed. For this reference to Fig. 4, which shows the line input (at the top) and voltages v_1, v_2, v_3 at pins 1, 2, 3 of the fifth stage and at pin 3 of the fourth stage, will prove helpful. In the resting state, when $v_{in} = 0$, capacitor C_2 is discharged with zero voltage across it while capacitor C_l is fully charged to the bias voltage V_B; no current flows and, hence, the voltages v_1 and v_{10} of pins 1 and 10 sit at ground potential while pins 2, 3, and 12 sit at the bias

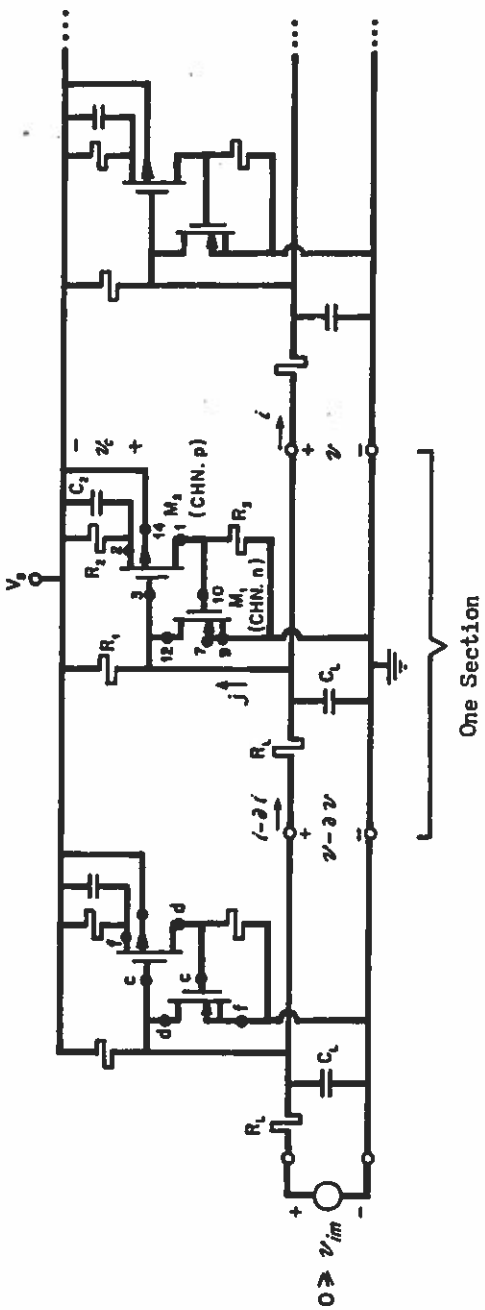


Fig. 1. Basic neuristor line circuit for negative pulse transmission.

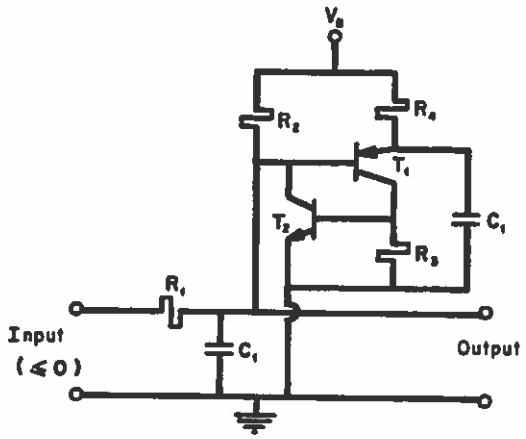


Fig. 2. One section of circuit of Wilamowski *et al.* [85].

potential V_B. From these observations we see that with zero input the gate-to-source voltage of the *n*-channel MOS transistor M_1 is given by $v_{gs_1} = v_{10} - v_9 = 0$ and similarly for the p-channel transistor M_2, $v_{gs_2} = v_3 - v_2 = 0$. In other words, under zero input conditions both M_1 and M_2 are turned off (i.e., zero drain current flows) since necessary requirements for their respective conduction are $v_{gs_1} > V_P$ and $v_{gs_2} < -V_P$, where $V_P > 0$ is the *n*-channel pinch-off voltage of the complementary MOS pair (this voltage being about 2 volts for our MC14007CP devices). With the application of a

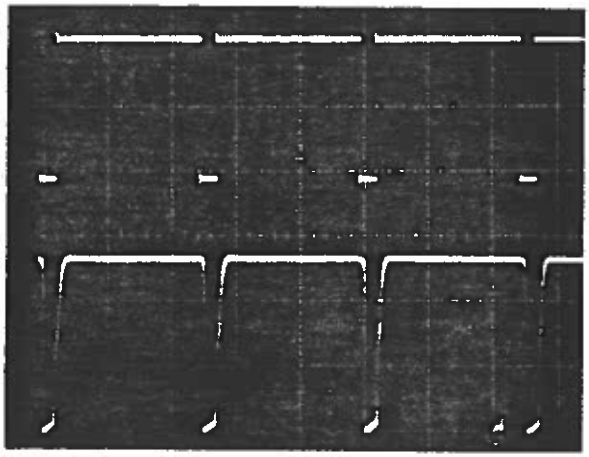


Fig. 3. Typical pulses of Fig. 1 (10 μsec/div). Top: Input voltage (2 V/div.; 0 = top graticule). Bottom: Voltage at pin 3 of fifth stage (5 V/div.; 0 = bottom graticule)

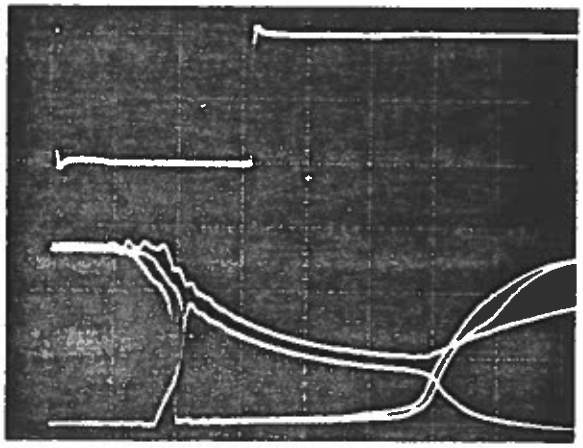


Fig. 4. Expanded internal voltages (0.5 μsec/div.). Top: Input voltage (2 V/div.). Bottom four traces—Internal voltages (5 V/div.): Top at left—v_2, fifth stage; Upper middle at left—v_3, fifth stage; Lower middle at left—v_3, fourth stage; Bottom at left—v_1, fifth stage.

sufficiently large negative input pulse, v_3 is lowered while v_2 can only slowly lower, being held by the capacitor C_2; with proper choice of parameters this turns on M_2. Sufficient current, as the activated source–drain current of M_2, flowing through R_3 raises the potential v_1 turning on M_1, a delay occurring due to the intrinsic delay in transferring the signal through M_2, and, more controllably, through the necessity of discharging C_l (through R_l and R_1 effectively in parallel) in order to lower v_3 to turn on M_2. The added current through R_1 due to the activation of M_1 further lowers v_3, this being the actual cause of a very sharp drop in the voltage v_3 [see Fig. 4 where this phenomena is seen at about 1 μsec in the fifth stage output (the input to this fifth section occurring as the fourth stage output at about 0.9 μsec)]. Consequent to this sharp drop in v_3, C_2 continues to charge up, this charging taking place following the MOS nonlinear (square-law) drain current characteristic until $v_3 - v_2$ approaches $-V_P$ (see Fig. 4 at about 2.9 μsec) during which time a quick change through the linear operation region of M_2 can occur as M_2 turns off. After a sufficient drop in v_1 a similar change in transistor M_1 takes place, it also turning off (see at about 3.4 μsec in the fifth stage output of Fig. 4). Here the state of refractoriness is fixed by the state of discharge of C_2, while the possibility for oscillations with a steady input exists if the situation is such that M_2 turns on again with sufficient discharge of C_2 (as occurs in Fig. 8 below).

Experiments were carried out to illustrate some of these points with oscilloscope traces shown in Figs. 3–9 (taken from a Tektronix 5403 with

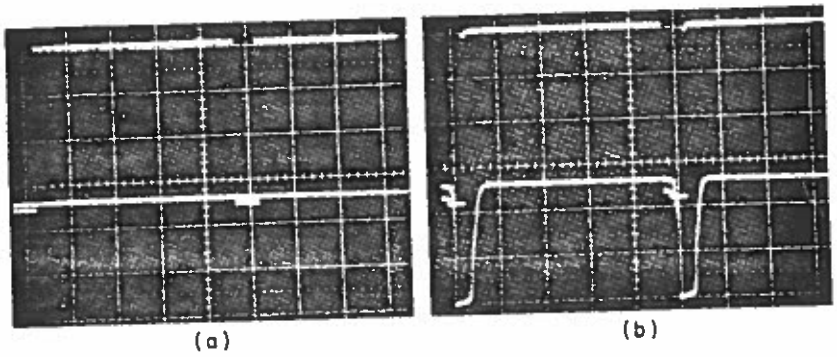


Fig. 5. Amplitude threshold (5 μsec/div.). (a) Input amplitude just below threshold. (b) Input amplitude just above threshold: Tops—Input (0.5 V/div.); Bottoms—Voltage at fifthstage (5 V/div.).

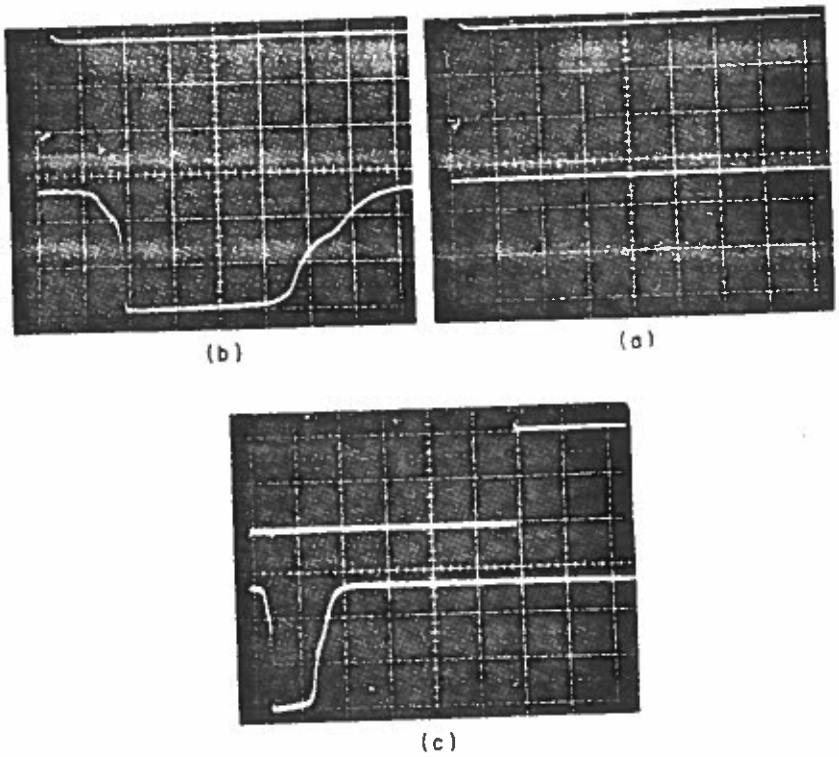


Fig. 6. Pulse width threshold. (a) Input pulse width just below threshold (0.5 μsec/div.). (b) Input pulse width just above threshold (0.5 μsec/div.). (c) Independence from input pulse width above threshold (2 μsec/div.): Tops—input (2 V/div.): Bottoms—voltage at fifth stage (5 V/div.).

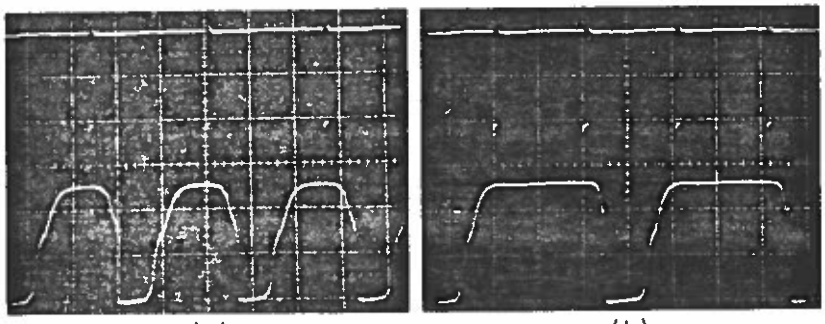


Fig. 7. Refractory period (2 μsec/div.). (a) Input repetition rate just prior to refractoriness. (b) Input repetition rate just after refractoriness. Tops—input (2 V/div.); Bottoms—voltage at fifth stage (5V/div.).

5A48 dual trace and 5B42 delaying time base plug-ins and a 013-0090-00 × 1 probe). In all of these the upper trace is the periodic negative going applied voltage pulse (from a HP 8002 pulse generator) while the lower trace is generally the voltage on the line (pin 3) at the fifth section of an eight section line (with a resistor R_t to ground at the right). The circuit element values were $R_t = R_1 = R_2 = 5.6$ kΩ, $R_3 = 2.7$ kΩ, $C_t = 0$ (except 50 pF and 100 pF in the last two parts of Fig. 9), $C_2 = 270$ pF, and $V_B = 13$ V (from a HP 721A power supply). In all of the traces, the very top and bottom grid lines show ground potential.

Commenting specifically on these traces, Fig. 5 shows that a pulse is excited when the input amplitude is above 1.85 V. Figure 6 shows that when the input pulse width is larger than 0.17 μsec (at 4 volts amplitude) an output is triggered; it also shows that this output is independent of the input pulse width when longer than its threshold width. Figure 7 illustrates that the refractory period is 5.5 μsec, since when input pulses occur more frequently some cannot trigger outputs. The interesting pulse repetition rate control by input amplitude is illustrated in Fig. 8 where the control is easy to be exercised over the range $-5.2\text{ V} > v_{in} > -7.3\text{ V}$. Finally, Fig. 9 shows the delay as it changes due to changes in C_t and R_t, the first two leftmost curves using only the intrinsic input capacitance of the transistor circuit (seemingly this intrinsic capacitance is about 10 pF being close to the parallel combination of the two gate-to-source capacitances of about 5 pF each). Experimentation also showed the delay per stage to be about identical for the middle five stages, of the eight stage line, being also as illustrated between the fourth and fifth stage in Fig. 4 (thus, about 0.1 μsec/stage).

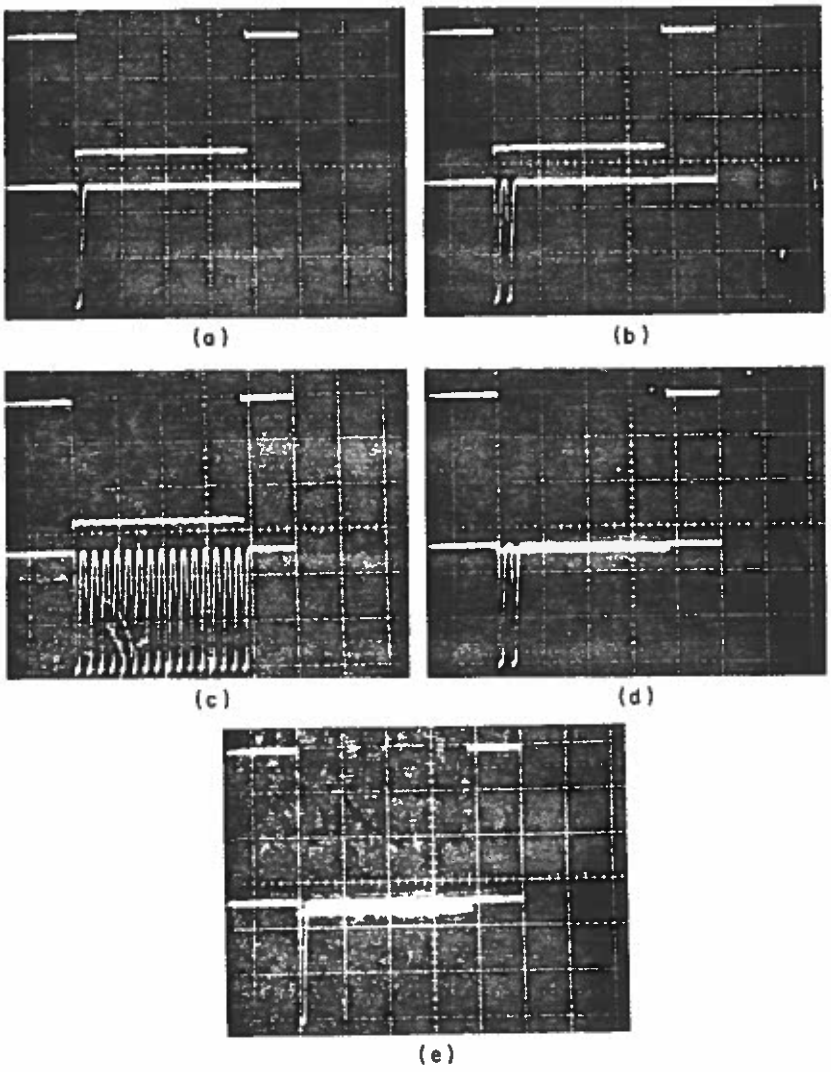


Fig. 8. Voltage controlled Pulse repetition rate (20 μsec/div.). (a) Input for single pulse output. (b) Input for double pulse output. (c) Input for continuous pulse generation. (d) Larger input for double pulse output. (e) Larger input for single pulse output: Tops—input (2 V/div.); Bottoms—voltage at fifth stage (5 V/div.).

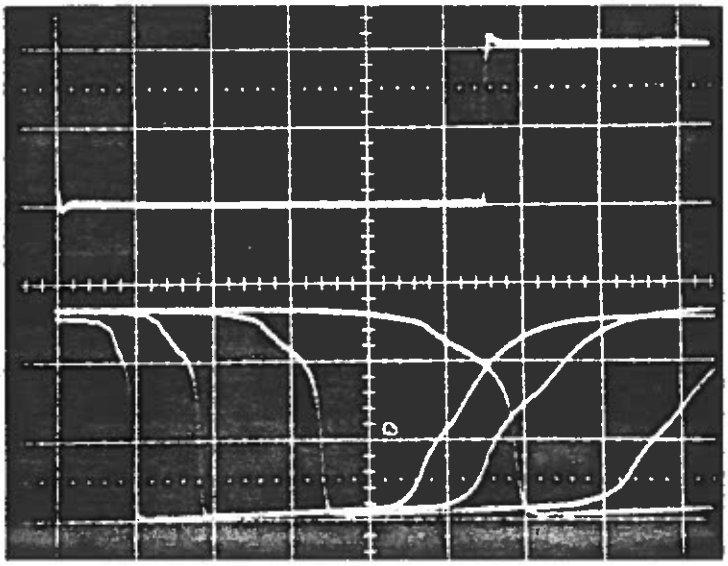


Fig. 9. Delay control by R_l and C_l (0.5 μsec/div.: V_{ll} = 13 V). Top: input (2 V/div.). Bottom (5 V/div.): Leftmost—R_l = 2.7 kΩ, C_l = 0 pF; Second—R_l = 5.6 kΩ, C_l = 0 pF; Third—R_l = 5.6 kΩ, C_l = 50 pF; Rightmost—R_l = 5.6 kΩ, C_l = 100 pF.

2.2. Modifications and Other Circuits

By using the symmetries of CMOS devices, Fig. 1 is readily modified to transmit positive going pulses, as shown in Fig. 10. If one desires a line transmitting positive and negative pulses, one naturally thinks of realizing these two lines, of Figs. 1 and 10, as a simultaneous line, but the existence of two opposite resting levels on C_l, which one would like to be common, initially negates this attempt. However, interchanging ground and the bias points while reversing the sign of the bias voltages in these two types of "one-port loads" brings the resting level on C_l to zero. Doing this, while sharing R_1, gives a line, a section of which is shown in Fig. 11, which will transmit both positive and negative pulses. As a comment on its operation, we mention that it has proven rather touchy to operate, requiring rather close coordination between bias and input voltages, apparently due to substrate couplings. As a further comment we note that Fig. 11 is a nice configuration for complete integration since all capacitors have a common terminal at ground. In order to have identical positive and negative pulse characteristics the complementary transistors of the two parts (p-channel of upper circuit with n-channel of lower circuit, for example) most

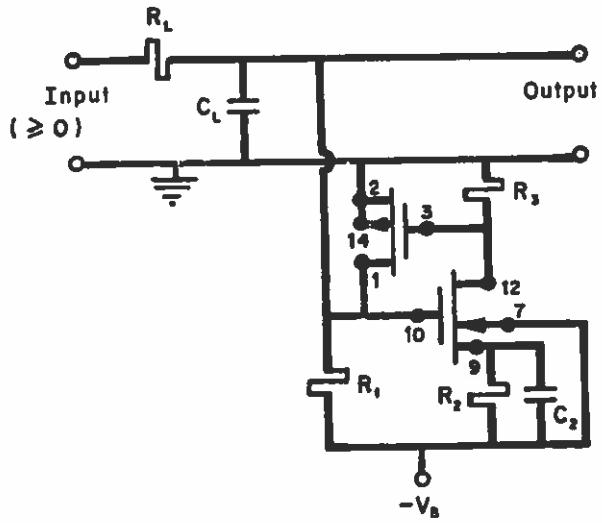


Fig. 10. One section of Fig. 1 modified for positive pulse transmission.

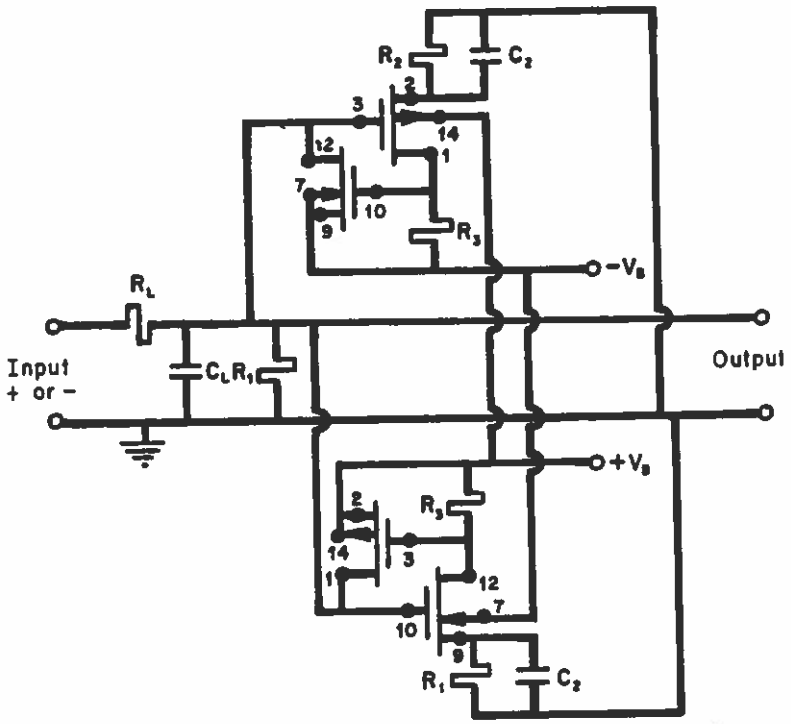
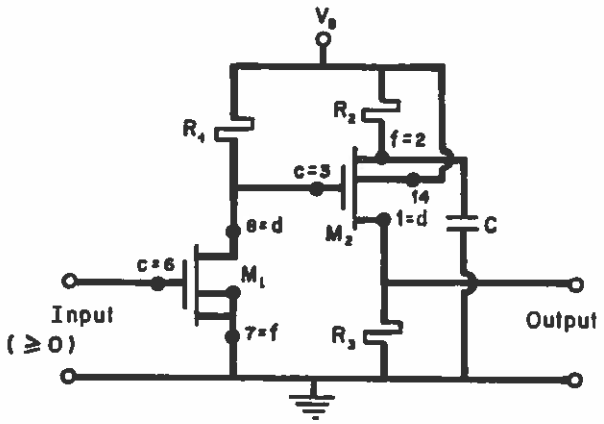


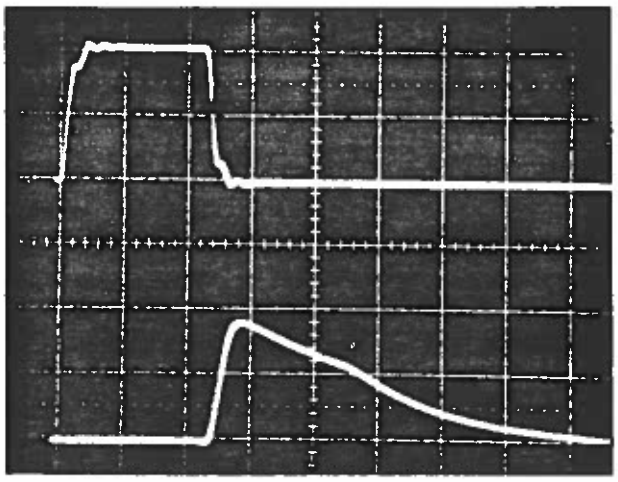
Fig. 11. Neuristor line section for positive and negative pulse transmission.

conveniently should be well matched, something still relatively hard to accomplish in integrated circuit technology though.

The circuits discussed to this point have all been of the nature of loaded lines, and, thus, most convenient for consideration of distributed realizations. A different configuration is shown in Fig. 12 of a previously developed but unpublished circuit which satisfies all of the neuristor definition conditions.



(a)



(b)

Fig. 12. Simple unilateral neuristor line section and response. (a) Circuit—typical values: $R_1 = R_2 = 20$ kΩ, $R_3 = 2.7$ kΩ, $V_B = 9$ V, $C = 100$ pF. (b) Response (2 V/div., 0.2 μsec/div.): Upper trace—input (zero at fifth trace); Lower: fifth stage output (zero at first trace).

Here the n-channel input transistor M_i merely acts as an inverter, which also gives unilateral transmission and isolation, while the p-channel M_2 gives the nonlinear and active structure with feedback necessary for pulse shaping. This section then transmits positive pulses and unilaterally from left to right. Probably the circuit of Fig. 12 is the simplest neuristor available, though the absence of real gain in the feedback path precludes it from having the voltage controlled repetition rate property, or so it seems. But this is remedied by inserting a feedback transistor, M_1 in the same relation to M_2 we had in Fig. 1, as per our previously published circuit [87], now studied extensively by Kulkarni-Kohli [88]. Further, the circuit can be made to transmit positive and negative pulses through a conjunction similar to that used to obtain Fig. 11, and probably more successfully due to the isolation of the stages (positive results are contained in [88, p. 30]).

Y la pobreza del lugar, y el polvo
Sitios de piedra decidida y limpia [1].

3. MATHEMATICAL ANALYSIS

In this section we show that by standard circuit analysis reasonable results can be obtained, as the delay per stage or the describing differential equations. However, we will see that the "state of the art" of modern mathematics is not to the point that analytic characterizations can be obtained from the nonlinear partial differential equations describing distributed MOS neuristors.

On all of the lumped circuits presented here it is a relatively straightforward matter to perform a computer aided analysis using standard models for the MOS transistors. This has been carried out [88] to good agreement on the derivative [87] of Fig. 12, from which a simple accurate model of the MOS transistor has been introduced by Kulkarni-Kohli [88, p. 36]; this will be used at Eqs. (2) and (4) below. However, due to the availability in the U.S. of CMOS packages at very low cost (about three transistor pairs for 0.30 U.S. dollars), it has been actually easier to carry out the experiments discussed earlier. Nevertheless, for design purposes it is important to have design equations for parameters of interest. Since for envisaged uses the delay per stage is probably the most important parameter to be controlled, we develop this before continuing to more abstract topics.

Applying circuit theory to any stage, but the first, of Fig. 1 we can roughly calculate the time delay through it as follows. The stage is activated by turning on M_2 which is accomplished by discharging C_i by an amount V_p. Roughly, this capacitor sees an effective resistance R_e of R_1 in parallel with R_i (since the previous state is assumed activated, which effectively grounds the coupling R_i and because the unactivated MOS transistors appear as open circuits).

The discharge law of the single time-constant circuit will then be $v_3(t) = V_B - V_B \exp(t/R_e C_l)$; at the turn on time t_1 of M_2 we have $v_3(t_1) \approx V_B - V_P$, or on solving

$$t_1 \approx R_e C_l \ln(V_B/V_P) \qquad \text{with} \quad R_e \approx (R_1 R_l)/(R_1 + R_l). \tag{1a}$$

Added to t_1 to obtain the actual delay t_d is the intrinsic delay t_i of each transistor (the time when drain current starts to flow after the gate-source voltage reaches its turn-on level). Thus

$$t_d = t_1 + 2t_i. \tag{1b}$$

Numerically we can check against Fig. 4 by using $t_i \approx 10$ nsec, $C_l \approx 10$ pF, $R_1 = R_l = 5.6$ kΩ, $V_B = 13$ V, $V_P = 2v$, from which Eqs. (1) give $t_d \approx 0.07$ μsec while Fig. 4 shows about 0.1 μsec of delay per stage; Eq. (1a) is rough, but exhibits the important design parameters (see also Fig. 9). Other such formulas can be worked out for the remaining neuristor characteristics [85], though again these give more in the way of design insight than accurate determinations.

More challenging is the analysis of truly distributed circuits for which we will set up the pertinent partial differential equations for the MOS loaded lines; for these, as will become apparent, computer aided analysis is much more pertinent in the absence of analytic mathematical techniques by which to proceed.

First we consider characterization of the MOS devices, for which we introduce a function $F(\cdot, \cdot, \cdot)$ of three variables

$$F(x, y, z) = \beta(x - z)^2\{1 - \exp[-Ky/(x - z)]\}u(x - z), \tag{2}$$

where β and K are positive constants and $u(\cdot)$ is the unit step function

$$u(x) = \begin{cases} 1 & \text{if} \quad x > 0, \\ 0 & \text{if} \quad x \le 0. \end{cases} \tag{3}$$

Then, as shown in a curve fitting manner by Kulkarni-Kohli [88, p. 36], matched n- and p-channel CMOS transistors are accurately described, respectively, by

$$i_{ds} = F(v_{gs}, v_{ds}, V_P), \qquad \text{n-channel}, \quad V_P > 0, \tag{4a}$$

$$i_{ds} = -F(-v_{gs}, -v_{ds}, -V_{P_p}), \qquad \text{p-channel}, \quad V_{P_p} = -V_P, \tag{4b}$$

where i_{ds} is the drain-source current, etc. (for the MC14007CP package, $K \approx 5$, $V_P \approx 2$ V, $\beta \approx 0.64 \times 10^{-3}$ A/V^2). Using these relationships we can turn to an analysis of a section of Fig. 1.

We have, on summing currents at node 12,

$$j = R_1^{-1}(v - V_B) + i_{ds_1}, \tag{5a}$$

and from Eq. (4a)

$$\begin{aligned} i_{ds_1} &= F(v_{gs_1}, v_{ds_1}, V_P) = F(v_1, v, V_P) \\ &= F(-R_3 i_{ds_2}, v, V_P). \end{aligned} \tag{5b}$$

From Eq. (4b), using the capacitor C_2 voltage v_c as defined in Fig. 1,

$$\begin{aligned} i_{ds_2} &= -F(-v_{gs_2}, -v_{ds_2}, V_P) \\ &= -F(-[v - (v_c + V_B)], [v_c + V_B + R_3 i_{ds_2}], V_P). \end{aligned} \tag{5c}$$

To proceed, Eq. (5c) needs to be solved for the i_{ds_2} which occurs on both of its sides and this solution substituted into Eq. (5b); such a solution always exists, as is seen by plotting the left side and the right side [using Eq. (2)] of Eq. (5c) and noting that for fixed values of v, v_c, R_3, V_B, V_P, K, and β there is one and only one intersection. Thus, we can functionally obtain

$$i_{ds_2} = G(v, v_c). \tag{6a}$$

Analytically it is difficult to give a more explicit formula for $G(\cdot, \cdot)$, but note that in our circuit the second argument, $y = [v_c + V_B + R_3 i_{ds_2}]$, in Eq. (5c) never goes negative in which case the unit step is $u(y) = 1$; if further $K = \infty$ then we obtain

$$i_{ds_2} = G(v, v_c) = -\beta(v_c + V_B - V_P - v)^2 u(v_c + V_B - V_P - v), \tag{6b}$$

which is a useful square-law approximation to the actual current.

Continuing, a straightforward substitution of Eq. (6a) into (5b) and then into (5a) yields

$$j = R_1^{-1}(v - V_B) + F(-R_3 G(v, v_c), v, V_P), \tag{7}$$

which gives the relationship of the one-port terminal current j in terms of the one-port terminal voltage and internal capacitor (state-variable) voltage v_c, where also we observe that in the resting state, $v = V_B$, $v_c = 0$, we have $j = 0$.

Next the dynamical equation for v_c is found by summing currents at node 2:

$$i_{ds_2} = R_2^{-1} v_c + C_2 \dot{v}_c \qquad (\text{where} \quad \dot{x} = dx/dt) \tag{8a}$$

or, from Eq. (6a)

$$C_2 \dot{v}_c = -R_2^{-1} v_c + G(v, v_c). \tag{8b}$$

Now consider Fig. 1 to be a distributed circuit with a section of length ∂x, in which case we can set up partial differential equations describing the line as follows. Across $R_l = r_l \, \partial x$ we have $(v - \partial v) - v = R_l(i - \partial i)$ and through $C_l = c_l \, \partial x$ we have $-\partial i = (c_l \, \partial x)(\partial v/\partial t) + j$ where from Eq. (7) we can

express the current j as $j = f(v, v_c)\,\partial x$ with $f(V_B, 0) = 0$. Similarly from Eq. (8b) we can write, using $C_2 = c_2\,\partial x$, $(c_2\,\partial x)(\partial v_c/\partial t) = g(v, v_c)\,\partial x$ where $g(V_B, 0) = 0$. The equations of interest for a distributed realization will then be (on taking the limit as ∂x tends to 0)

$$(\partial^2 v/\partial x^2) = r_l c_l(\partial v/\partial t) + r_l f(v, v_c), \tag{9a}$$

$$(\partial v_c/\partial t) = c_2^{-1} g(v, v_c) \tag{9b}$$

with $v(x, t)$ having $v(0, t) = v_{in}(t)$ specified. Equations of this form are known as nonlinear diffusion equations in mathematics [91]. Stimulated by the problems in neural modeling, there has recently been considerable interest in such equations by mathematicians who have treated either special cases, often of very simple functions f and g, [92–112], or very general situations [113–121].

The main interests in Eqs. (9) have to do with traveling wave solutions, that is solutions which are only a function of $z = x - vt$ where v is the velocity of travel; we note that then

$$(\partial/\partial x) = -v^{-1}(\partial/\partial t) = (d/dz) = ', \tag{10}$$

which leads to so called "dynamic steady state" [54, p. 175] state variable equations

$$v' = w, \tag{11a}$$

$$w' = -v^{-1} r_l c_l w + r_l f(v, v_c), \tag{11b}$$

$$v_c' = -c_2^{-1} v g(v, v_c). \tag{11c}$$

For these we know $v = V_P$, $v_c = w = 0$ define an equilibrium point, corresponding to the resting state of our line. Now it is known that if f and g were linear the (parabolic) set of partial differential equations (9) have no nonresting state traveling wave solution [110, p. 882], consequently the question of existence of solutions of Eqs. (11) is not easily dismissed. The real problem, which has as yet not been analytically solved in general [110, p. 886], is that of determining the velocity v of wave propagation, under appropriate boundary conditions, those treated so far(for very special f and g) representing either a single traveling pulse or a periodic train of traveling pulses [112–122]. However, using the time-delay found at Eq. (1) we can of course estimate the velocity v for our MOS circuits.

Although not much more can really be said analytically on the form of solutions one can try to linearize Eqs. (11). Linearization is most easily accomplished when in the active region as one need use only the square law behavior of the MOS transistors [as at Eq. (6b)]. Because of step function discontinuities, though, this is only tractable when linearization occurs about the excited state, of most practical interest for stability considerations of the transmitted pulse, but this excited state must first be analytically assumed.

Nevertheless, in the abstract mathematical sense probably most progress has been made in this direction [114–119].

> Las portales profundos, las mamparos
> Cerrados a la sombra y al silencio [1].

4. DISCUSSION

The MOS transistor being of simple construction and having nonlinear active voltage-controlled current source characteristics has seemed to be a fundamental building block for electronic circuits. Here we have illustrated its versatility in the realization of neuristor lines of various configurations. In fact the basic realization of either Fig. 1 or Fig. 2 has appeared most naturally to be implemented with MOS devices once its principle of operation, using currents controlled by voltages, is understood.

But what we have presented here also seems to be just a start in the area. To be sure, we are able to construct neuristor lines, as per Fig. 11, which transmit positive and negative pulses. Nevertheless, the practical lack of complete symmetry in constructing CMOS pairs makes the actual operation more difficult than for the single signed pulse lines. This lack of symmetry was ignored, for simplicity, in our setting up of the mathematical analysis of the basic line, since at Eq. (4) we assumed that the same parameters β, K, V_P described both the n-channel and the p-channel devices, which is not quite true. But correcting for this disymmetry on the basic line is straightforward. And, although we have seen that setting up describing equations, as Eqs. (9), is straightforward, it is not an easy matter to carry out an analysis of these equations, in which case most of the design to date has been carried out empirically either numerically on the computer or experimentally in the laboratory. In short we lack a complete mathematical theory of neuristor lines.

Besides just being a start in the mathematical sense, what we present is also a start in the physical sense in that physical constructs to this date are all by way of lumped sections while totally distributed integrated circuit neuristor lines, especially following Fig. 11, should be quite possible. Likewise since MOS transistors can readily realize resistors and capacitors, another promising direction of investigation, even in the lumped section case, is to obtain neuristor lines constructed solely from MOS devices. Other improvements, as electronically controlled delay, seem possible. Further, the material presented has covered only neuristor lines themselves. Although these are sufficient to realize all components for making computers, there is another class of circuits, called "neural junctions" [123–126], which can be used to combine neuristors in possibly new and interesting configurations. And, since neuristors are level detecting pulse generators, they

can be considered for use wherever such are desired, as for example in delta modulators, which we presently have under investigation.

In the References we have listed a number of the more pertinent references, without thought to much selectivity. Consequently, for those wishing to get a firmer start in the field we recommend that, besides Crane's basic though somewhat general paper [3], the immediately following paper of the same issue by Nagumo *et al.* [9], still seems to us the specific paper of most interest. For those most interested in the mathematics, Hastings' tutorial paper [110] is quite understandable and covers the primary points of interest. As time goes on we believe the theory of "catastrophes" [127] will be seen to be more and more applicable. And for those wishing more, possibly relevant, works we add references [128–208], a few of which we have as yet not been able to locate. In the near future we do hope to make available an annotated collection of the references.

Finally, we believe that in the above we have shown again the possibility of making neuristors which can be constructed in integrated circuit form. Improvements are needed as mentioned but as illustrated by the various oscilloscope traces, the neuristor properties are obtained, and, thus, the nickname "heuristor" can now be taken as a play on the creator's shortened forename!

Y nombraré las cosas, tan despacio
Que cuando pierda el paraiso de mi calle
Pueda llamalas de pronto con el alba [1].

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Y después de fuerte aguaje
Viene la apacible calma;
En el desierto la palma
Doblando va su follaje [209].

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