VOLTAGE CONTROLLED OSCILLATIONS

IN THE MOS NEURAL LINE*

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Abstract

An electronic simulation of the rythmic response property of the nerve axon to steady stimulii is presented. In particular, by a suitable choice of parameters the MOS neural line shown in Fig.1, simulates the voltage controlled oscillation property, in addition to its other axonal properties previously obtained[1].

1. INTRODUCTION

Rythmic responses to steady stimulii are a characteristic property of the nerve axon, and an essential feature of the nervous system where information is transmitted down the nerve fibers in frequency codes[2],[3]. The frequency of these rythmic responses increases with the d.c. level of the input stimulii, maintaining the output pulse size and shape and, thereby, signalling intensity by frequency. The voltage controlled frequency response varies widely from neuron to neuron depending on their physical dimensions.

Here we show that the MOS neural line shown in Fig.1 simulates, with a proper choice of the line parameters, the voltage controlled oscillation property, in addition to its other axonal properties previously obtained[1]. By varying the capacitances in the line, it is shown that a wide range of frequencies can be obtained, as evidenced also in biological studies[3].

2. EXPERIMENTAL RESULTS

The MOS neural line shown in Fig.1 is made to simulate the voltage controlled oscillation (VCO) property in addition to the standard properties of (a) threshold of stimulability, (b) refractory period, (c) pulse shaping and (d) constant velocity of propagation for a proper choice of the line parameters R_1, R_2, R_3 and V_B. In particular, R_1= 2.0KΩ, R_2= 6.9KΩ, R_3= 4.7KΩ and V_B= 10.0 volts were chosen to illustrate the VCO property. Figure 2 shows the VCO property of an 8-stage experimental neuristor line. Here the input and the fourth stage output are super-imposed for two different d.c. input levels, V_i=5.3v and V_i=5.45v. Note the increase in frequency with the d.c. input voltage level from approximately 180 KHz to 250 KHz, respectively.

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The variation in the frequency of oscillations with the d.c. input voltage level is shown in Fig.3 for a single neural stage, with the capacitance C, of the first stage as a parameter. Note that lower frequencies are generated for higher capacitance values, giving a wide range of oscillation frequencies for the neural stage. These generated frequencies are in general very sensitive to the supply voltage V_B of the line. In particular, for an input voltage of V_i=5.4v and C=680pf, the variation in frequency with the supply voltage V_B is also plotted in Fig.3, illustrating a lowering in frequency with an increase in the supply voltage V_B. These properties were also verified numerically by a computer-aided analysis using the SPICE program.

3. PRINCIPLE OF OPERATION

Consider the operation of a single MOS neural stage (shown between dashed lines in Fig.1). The operation of the stage under discussion here is similar to that described in ref.(1), except that after the generation of the first action potential output, in response to an above threshold step input, the voltage v_{23}, the source-to-gate voltage of the primary transistor of the stage, the p-channel MOSfet M_2, can increase, due to the feedback current from M_3. This in turn pulses on the MOSfet M_2 causing another output pulse to be immediately generated. This phenomena is repeated as long as the input is present since the input value is responsible for bringing the output voltage v_0, again, after the generation of the output pulse, above the pinch-off value V_{Pn} of the gate-to-source voltage of the n-channel feedback transistor M_3, for sustained oscillations.

To analyze in somewhat more detail we note that when operating in the 'variable resistance' region, the n-channel MOS law(4,p.51) is

$$i_{ds}=2K_n((v_{gs}-V_{Pn})v_{ds}-\tfrac{1}{2}v_{ds}^2) \quad \ldots\ldots\ (1)$$

where we continue to use symbols as defined in ref.(1). We also note that for the neuristor line circuit

$$v_3 = v_{ds1} = V_B - R_1 i_1 \quad \ldots\ldots\ (2)$$

where v_3 is the voltage of point 3, the drain of M_1, with respect to ground. Too, for an input voltage v_i which is d.c., v_i= V_i, of sufficient magnitude the transistor M_1 will be operating in the variable resistance region. Thus, when the feedback transistor M_3 is turned off, giving $i_1=i_{ds1}$, we have an initial value of v_3, call it v_{3I}, which satisfies, from eqs.(1) and (2),

$$R_1K_nv_{3I}^2 - (1 + 2R_1K_n(V_i-V_{Pn}))v_{3I} + V_B = 0 \quad (3)$$

Equation (3) proves rather sensitive to parameter variations, but within component tolerances checks experimentally. For example, for V_i=5.2v, v_{3I}=3.2v is experimentally observed, while for V_i=5.4v, v_{3I}= 2.0v results. Note that v_{3I} decreases with increasing input d.c. level V_i.

On the generation of the first action potential the output voltage, v_o, across R_3 is given by(1,eq.1)

$$v_o = R_3K_n(v_{32}-V_{Pp})^2 \quad \ldots\ldots\ (4)$$

since the p-channel MOSfet M_2 acts as a current source with $i_{ds}= K_p(v_{gs}-V_{Pp})^2$, K_p =-K_n. When $v_o=v_{gs3}$ achieves a certain value V_o sufficiently greater than the pinch-off voltage of the feedback MOSfet M_3, M_3 becomes conducting in the variable resistance region, adding its drain-to-source current i_{ds3} to that of M_1 through R_1. Experimentally V_o=$2V_{Pn}$ is found. This gives a new value of v_3, call it v_{3N}, given, by substituting eq.(1) into eq.(2) using i_1= $i_{ds1}+ i_{ds3}$, as a solution of

$$2R_1K_nv_{3N}^2-(1+2R_1K_n(V_i+V_o-2V_{Pn}))v_{3N}+V_B=0 \quad (5)$$

Again, experimentally, for V_i=5.2v, v_{3N}=1.3v is observed, while for V_i=5.4v, v_{3N}=1.2v.

The voltage v_3 is seen (experimentally) to rapidly jump between the two values v_{3I} and v_{3N} determined by eqs.(3) and (5), with the jumps occurring at times determined by the charging and discharging of the capacitor C, while, as seen above, $v_{3N} \ll v_{3I}$. This lower value of v_3 determined by eq.(5) decreases the gate-to-source voltage v_{32} of the primary transistor M_2, turning it on more and causing the output voltage to rise again and repeat the same cycle of operations as for the first output pulse described in ref.(1). Note, that an additional voltage drop at node 3, caused by the drain-to-source current of the feedback MOSfet M_3, sets the system into oscillation. As the difference between these voltages, v_{3I} and v_{3N}, indicated respectively by eqs. (3) and (5), is reduced, low amplitude, high frequency oscillations result, due to smaller changes in the conductance of M_2. Eventually, when $v_{3I} \sim v_{3N}$, no oscillations result, since no changes in the voltage $v_{32}=v_{gs2}$ controlling M_2 take place after the first output pulse. This is true for a sufficiently large V_i, which inverts the voltage at node 3 completely. So, an upper limit on input voltage also exists for these oscillations. An explicit expression for the generated frequencies can be derived by considering the charging and discharging of C, but this gives a complicated expression. It is evident, though, that any expression that will approximate the experimental data well should take into account the changing nonlinear conductance of the primary transistor M_2 during the oscillations.

The high frequency, low amplitude, oscillations generated by the stage get caught in the refractory zone of the remainder of the stages, so it is possible that not all of the oscillations generated by the first stage get transmitted as 'characteristic' action potentials. To eliminate this problem, the refractory period of the remaining stages is lowered with respect to the first stage by choosing lower capacitance values, C=100pf being used in our experiments for all stages except the first one, which has a higher capacitance value, as listed in Fig.3.

Note that the maximum frequency of oscillations, f_{max}, that can propagate on the line is determined by the inverse of the absolute refractory period, t_{ref}, for the remainder of the line beyond the first stage as determined in ref.(1). That is

$$f_{max} = 1/t_{ref} = 620 \text{ KHz} \quad \ldots\ldots\ldots (6)$$

for the chosen line parameters.

4. DISCUSSION

The VCO property was obtained for a small range of d.c. input voltage levels, typically a range of 0.3 volts from $V_i=5.15$v to 5.45v. This range was increased to approximately 0.8v for a complementary neural line constructed by replacing all n-type MOSfets by p-type MOSfets, and vice versa, and the supply voltage V_B to $-V_B$, thereby transmitting negative action potentials. This increase in the range is essentially due to the lower threshold of the feedback MOSfet M_3 which allows the oscillations to start for lower values of V_i. The p-type MOSfet M_3 of the complementary line has a threshold voltage of 1.4v as compared to 2.4v for the n-channel MOSfet M_3 for the regular line used here. The parameters of the complementary line also underwent changes ($R_1=R_2=5.6K\Omega$, $R_3=2.7K\Omega$) to optimize the input voltage range for which oscillations were obtained.

These results are reported in ref.(5) and were subsequently obtained by our Polish colleagues working with bipolar neural lines[6].

5. REFERENCES

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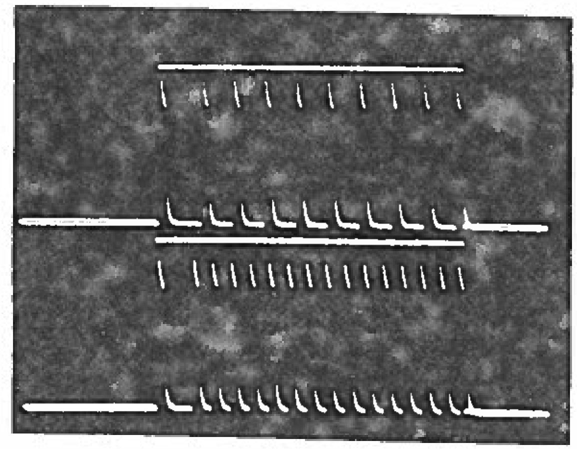

Fig.2. Voltage Controlled Oscillations. Input pulses to first stage and output pulses at fourth stage super-imposed. Horizontal=10μsec/div. Vertical= 2.0v/div.

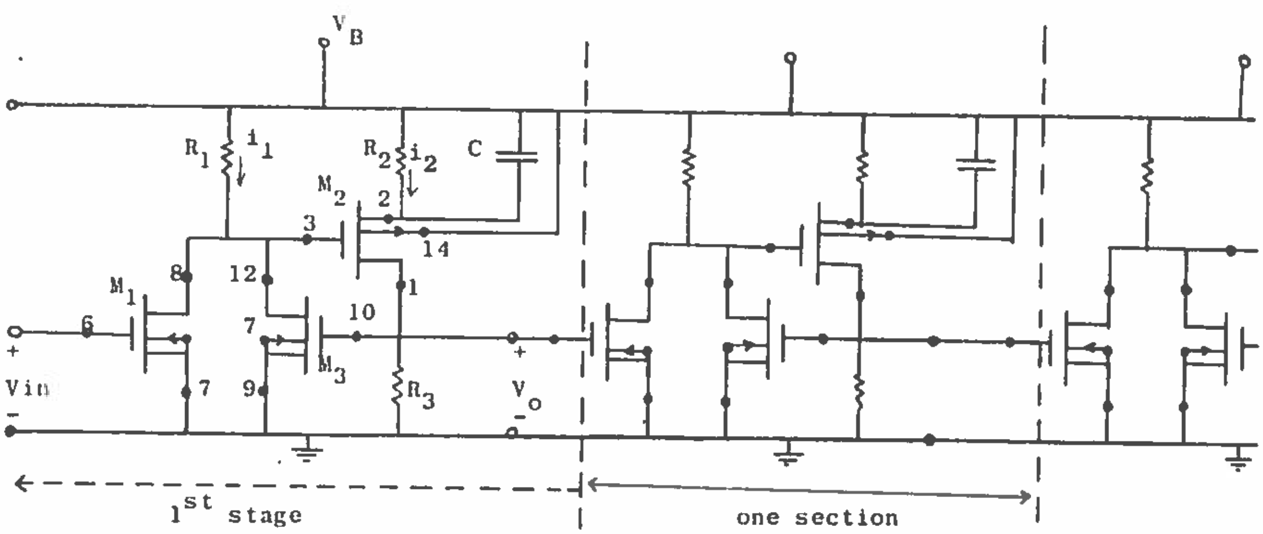

Fig.1. An Integrable MOS neuristor line.

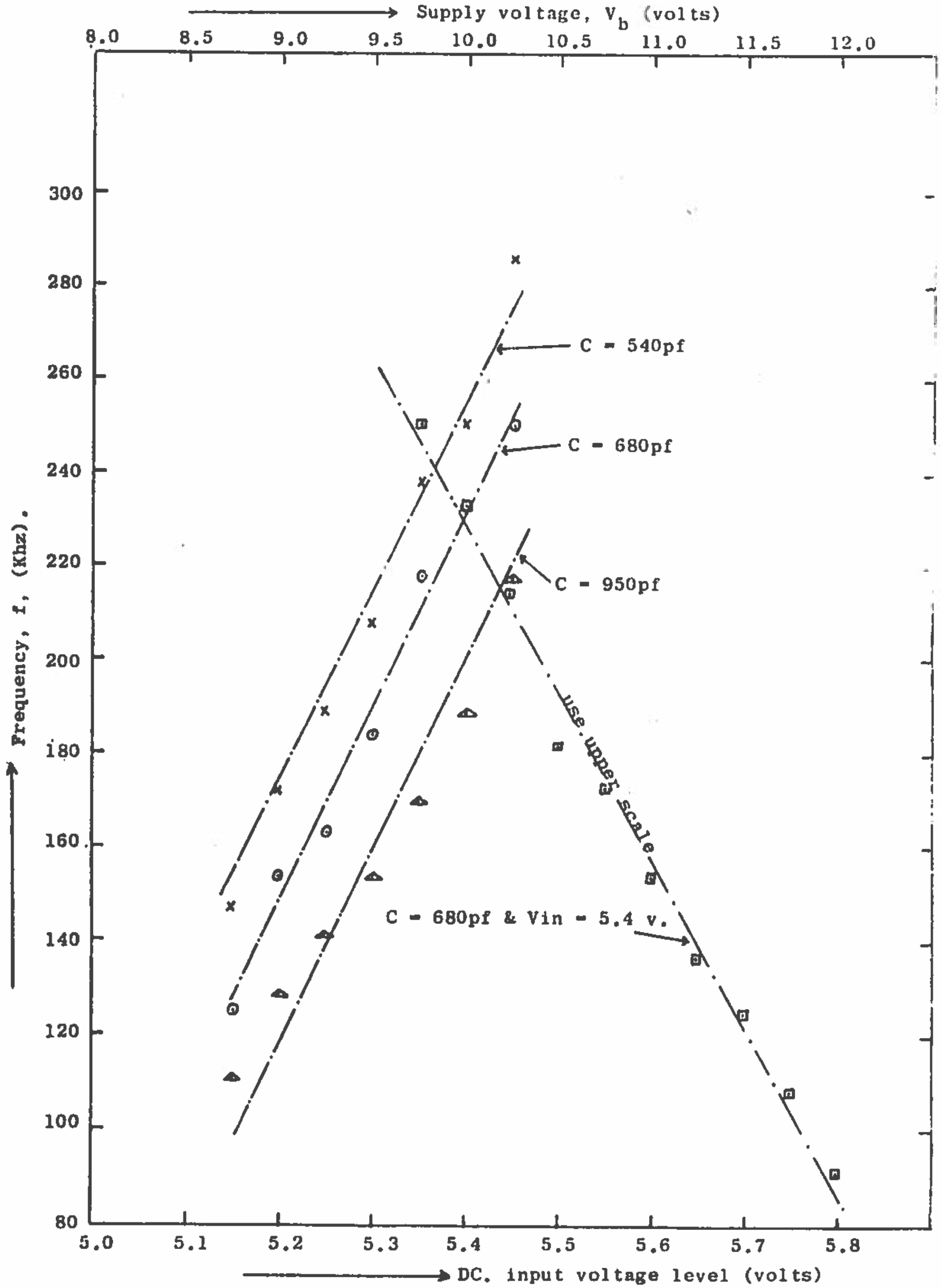

Fig.3. Experimental curves illustrating variation in frequency: (a) with input voltage level for C=540pf, 680pf and 950pf for first stage and C=100pf for other stages. (b) with supply voltage V_B for C=680pf and V_i=5.4v.

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