of 10·5 GHz and measured 14 × 7 cm; in microstrip on alumina it could be reduced to about 3 × 1·5 cm.

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D. J. GUNTON

Royal Radar Establishment
St. Andrews Road
Malvern, Worcs. WR14 3PS, England

5th March 1976

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NEURISTOR-LINE PULSE-TRAIN SELECTOR

Indexing term: Neural nets

A pulse-train selector using neuristor lines in T–R-junctions is presented. Use of T- and R-type junctions using two lines having different refractory periods t_{r1} and t_{r2} allows the selection of pulse subtrains from the input pulse train, for which a time interval between pulses is in a given time range (t_{r1}, t_{r2}). Practical realisation of the selector is also given.

It is known that the neuristor line has the following properties:[1–3]

(*a*) constant pulse-propagation velocity

(*b*) threshold point

(*c*) the pulse-shaping action

(*d*) refractory period

(*e*) annihilation of pulses in the case of their collision.

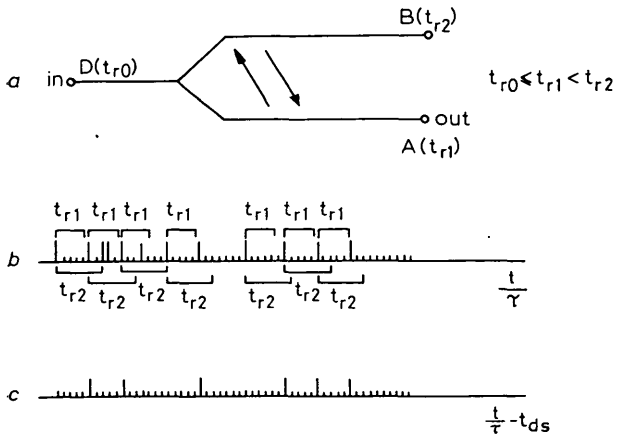

Fig. 1
a Concept of pulse-train selector
b Prescribed input pulse-train on normalised time axis
c Selected pulse subtrain from the output of the selector for selection range $(4 \cdot 5\tau, 7\tau)$. t_{ds} is delay time of the selector (between output and input)

It is also known that neuristor lines can be used for realisation of the two types of junction:[1]

(*a*) T-type (trigger), in which pulses can propagate in all directions along the lines

(*b*) R-type (refractory), in which the existence of pulses in a prescribed line causes an attenuation of pulses in other lines of the junction.

Using the properties of T- and R-junctions, threshold point and annihilation of pulses, it is possible to realise neuristor logic elements.[1, 2] Similarly, using the T–R-junction and the refractory properties of the neuristor line, it is possible to realise the pulse-train selector described here.

The general idea of the selector network with two neuristor lines A and B having different refractory periods t_{r1} and t_{r2}, respectively, is shown in Fig. 1*a*. In the connection of the line B to the line A by an R-junction, the input pulse transmitted in the two lines will be attenuated in line A as a consequence of a pulse on line B. This property is used in the selector circuit.

The initial pulse applied to the T-junction of the selector starts the refractory period in both lines A and B, and the network is then in its 'stand-by' state (ready to work). The 'stand-by' state means that the next pulse may be transmitted through line A and reach the OUT terminal when the pulse is applied to the T-junction after the refractory time t_{r1} and before the refractory time t_{r2} (for $t_{r1} < t_{r2}$). After transmission of the pulse through line A, the network is again in the 'stand-by' state, since, again, the refractory period is initiated in line A and also in line B as a consequence of the connection of line A to line B by the R-junction. The refractory time t_{r1} of line A forms an 'insensitive' time zone after the pulse propagation through it, and ensures that the pulses applied to the input of the line at time intervals smaller than t_{r1} are not transmitted to the output of the network. If the next pulse applied to the T-junction appears at a time larger than t_{r2} after the presence of the last transmitted pulse into line A, it will not be transmitted through the network, but only turns the network to the 'stand-by' state. The operation of the selector is explained in Figs. 1*b* and *c*. In Fig. 1*b*, the prescribed input pulse train on a normalised time axis is shown, and, in Fig. 1*c*, the selected pulse subtrain from the output of the selector is shown for an example where the selection range is $(4 \cdot 5\tau, 7\tau)$. Here τ is the delay time of the active sections of the lines. The neuristor line marked as D in Fig. 1*a* is the input line and can be used for shaping the input pulses when these are not of a proper shape; it is assumed $t_{r0} \leqslant t_{r1}$.

The practically realised selector circuit is shown in Fig. 2. The neuristor-line circuits used here are modified from the circuit described in Reference 3. The modification consists of the insertion of a diode in series with the resistor R_3 between the base and emitter of the transistor T_2. In this case, the effect of supply-voltage changes on the operation of the circuit is reduced and also the minimal ratio of refractory period to the delay time of a single section of the neuristor line is reduced. For example, in the circuit presented in Reference 3, this ratio is approximately 40 and in the modified circuit of Fig. 2 is approximately 7. Thus the modified circuits allow the selection of pulses having smaller repetition periods than does the unmodified circuit. Also, for application of the modified neuristor line to memory-cell realisation, the number of necessary line sections is less.

The refractory period of a single-line section, which determines the properties of the selector network, is[3]

$$t_r = R_4 C_1 \ln \left[\frac{V_b - V_{BE2}}{V_{in}/a - V_{BE1}} \right] + t_d \quad \ldots\ldots \quad (1)$$

where

V_b = supply voltage

V_{in} = input pulse amplitude

V_{BE1} = the minimum base–emitter voltage on transistor T_1, necessary for saturation of transistor T_2

V_{BE2} = base–emitter voltage determining the cutoff state of transistor T_2

$a = R_1/R_2 + 2$

t_d = duration of transmitted pulse (pulsewidth)

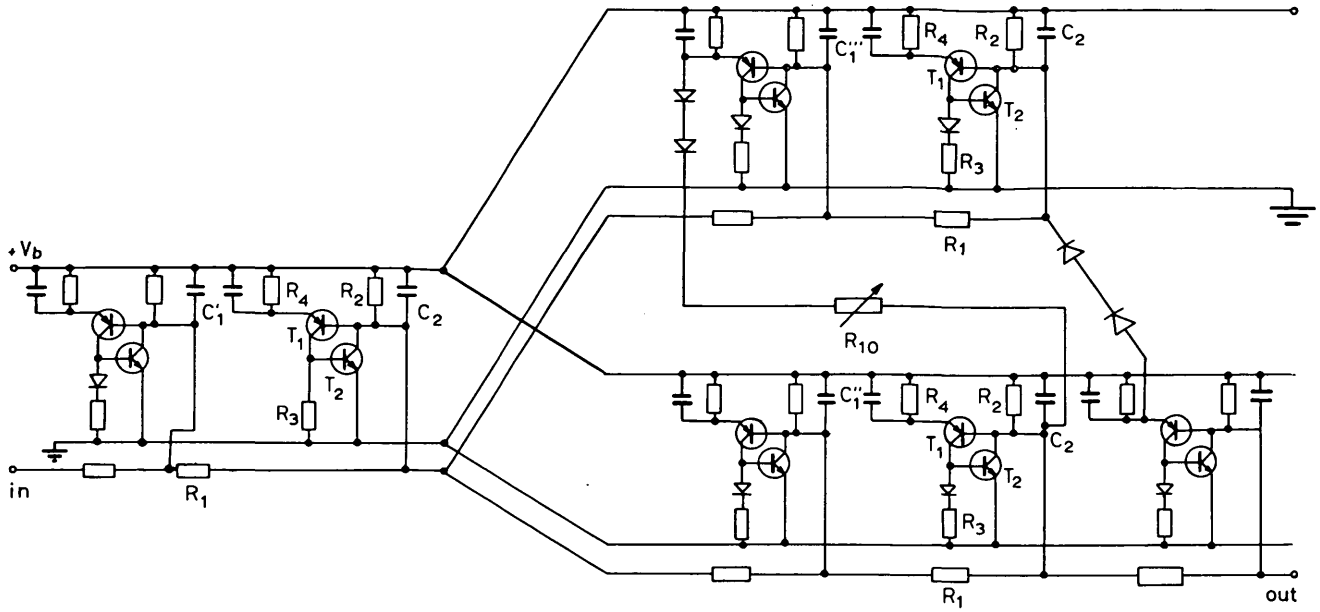

Fig. 2 *Practically realised pulse-train selector circuit*
$R_1 = 22\,k\Omega$, $R_2 = 5{\cdot}6\,k\Omega$, $R_3 = 50\,\Omega$, $R_4 = 25\,k\Omega$, $C_2 = 56\,pF$, $C_1' = C_1'' = 68\,pF$, $C_1''' = 75\,pF$

In the selector network described, with element values as shown in Fig. 2, the selection range was checked experimentally (4·5 μs; 5 μs).

The coupling between the second section of line A and the first section of the line B should be chosen so that the 'effective' refractory period of line B is t_{r2}, i.e. the end of the refractory period in line B caused by the pulse from line A should be at the same instant as it would be if it were triggered by a pulse at the input of line B. This can be obtained by setting the variable resistor R_{10}.

Since information in the pulse train can be carried by different times between pulses, the use of these pulse selectors as coders and the decoders should make it possible to realise logic 'in time'.

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Z. CZARNUL
M. BIALKÓ

Department of Electronics
Technical University of Gdańsk
80-952 Gdańsk, Poland

R. W. NEWCOMB

Electrical Engineering Department
University of Maryland
College Park, Md. 20742, USA

26th February 1976

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PRODUCTS OF GRAPH PROJECTIONS AS A MODEL FOR MULTISTAGE COMMUNICATION NETWORKS

Indexing terms: Communication networks, Graph theory, Network topology

The multistage graph provides an underlying structure for conventional telephone networks (the number of 'stages' in practice being about seven). A systematic analysis in terms of channel graphs and terminal graphs is carried out using products of graph projections. A unified theory emerges, and facilitates the synthesis and study of multistage switched networks of high connectivity.

At the UK Science Research Council Rencontre of users and inventors of combinatorial mathematics in Aberdeen, 1975, Cattermole presented various problems involving switched communication networks.[1-3, 5] For the multistage graph (introduced by Takagi[6]), which gives an approximate representation of telephone networks, the following problems arise:

Problem 1: Can some graph-theoretical construction be used to systematically obtain large multistage graphs of high connectivity?

Problem 2: Does any concept of product of graphs enable us to concisely formalise the way that multistage graphs are built up from channel graphs and terminal graphs?[3, 6]

Problem 3: Is there a binary operation on the set of n-stage graphs, which acts multiplicatively on the connectivity κ? In Reference 2, Cattermole shows that the connectivity of the Cartesian product $G_1 \times G_2$ of graphs is equal to the sum of the connectivities of G_1 and G_2, but can we obtain for n-stage graphs a 'product' π with $\kappa(G_1 \,\pi\, G_2) = \kappa(G_1) \times \kappa(G_2)$?

The answer to Problem 2 is 'no'. A typical channel regular multistage graph G, together with its channel graph C and terminal graph T are given in Fig. 1. Their numbers of vertices are 30, 12 and 17, respectively. There are many product concepts for graphs, but all have the vertex set of the product equal to the product of the vertex sets, and we shall never obtain $12 \times 17 = 30$.

Looking instead to another branch of mathematics, category theory,[4] we find a different type of operation, the fibred product of projections, which has proved to be a useful tool in algebraic topology. A definition of fibred product of n-stage graphs can be appreciated without knowledge of category theory, and, given as a particular case of the pullback operation,[7] enables us to obtain an affirmative answer for all three problems.

Our graphs G, C and T each have a natural projection map onto the path graph P_6 consisting of 6 vertices linked by a 5-edge path. These projections p_1, p_2, p_3, respectively, are in fact morphisms in the category of graphs, since they each send adjacent vertices to adjacent vertices. More generally, given any two graph projections $p_1 : G_1 \to G_3$ and $p_2 : G_2 \to G_3$, we define their *fibred product* to be the projection $p : G_1 \,\Pi\, G_2 \longrightarrow G_3$, where $G_1 \,\Pi\, G_2$ has vertex set $V(G_1 \,\Pi\, G_2) = \{(v_1, v_2) \in V(G_1) \times V(G_2) : p_1(v_1) = p_2(v_2)\}$, with adjacency $(v_1, v_2) \sim (v_1', v_2')$ whenever v_1 is adjacent to v_1' in G_1 and v_2 is adjacent to v_2' in G_2; p is defined by $p(v_1, v_2) = p_1(v_1)$, which equals $p_2(v_2)$.