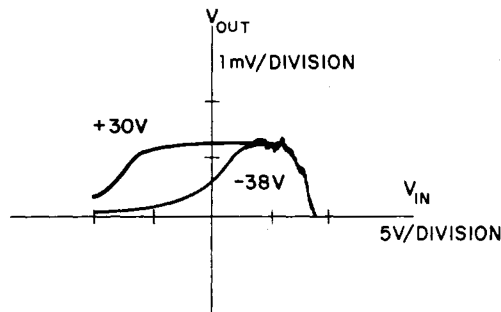

Fig. 3. ONE and ZERO sense voltage for 0.1 mil × 0.1 mil capacitor in simulated 200 × 200 array, written at +30 V and −38 V. Ramp rate = 3.5 V/s, R_{sense} = 20 kΩ, WRITE time = 0.2 μs.

(5–10 V). Fig. 2 shows a simplified diagram of a system used in experimental arrays. A negative voltage ramp is applied to a word line and the current in an appropriate digit line is sensed. The resulting voltage represents a dynamic *C-V* curve showing the drop in capacitance as the silicon under the intersection is driven into depletion. This ΔC is the signal information.

C-V curves corresponding to two different remanent charge states at the nitride-oxide interface are shown in Fig. 3. These two curves are oscilloscope traces from an experimental array, having aluminum lines varying in width from approximately 0.1 mil to 0.8 mil, and crossing n-doped silicon channels of like dimensions isolated by etched trenches. The capacitor measured by these traces (the smallest in the array) was 0.09 mil × 0.15 mil. In order to simulate readout conditions in a practical memory, a 20-mil-wide metal line and a 20-mil-wide diffusion were also added to the array, thus simulating the loading effects of a 200 × 200 memory of nominal 0.1-mil × 0.1-mil bits. Fig. 4 shows the experimental array layout and the general equivalent circuit of an $n \times n$ array. Clearing was accomplished with +30-V pulses and ONE's written with −38-V pulses each of 0.2 μs duration. The READ ramp sweeps between ± 11 V with a slope of 3.5 V/μs. The output signal is 1.1 mV across a 20-kΩ resistor as in the circuit of Fig. 2. The background voltage (horizontal axis) upon which the signal rides is 4.9 mV and is due primarily to parasitic coupling between the large probes used for voltage input and sensing.

In these experiments, MNOS devices with conductive nitride and thick oxide (40 A) were used. This complementary mode structure[3] results in charging currents occuring primarily through the nitride layer rather than through the oxide, as in the more common thin-oxide (20 A) MNOS structure. The thick-oxide device may result in better control and reproducibility of the dielectric charging properties. Since almost all uses of MNOS in the past have been predicated on the need for true nonvolatility (i.e., storage time in excess of 10 years), proposed engineering exploration of MNOS has usually concentrated on the use of thin-oxide devices, which have slower discharge rates.

In order to explore ultimate limitations to density, it was thought advisable to use air isolation rather than junction isolation, which is limited by the lateral widening of the depletion regions at the isolating junctions. For densities of 5000 to the linear inch or greater, some form of planar dielectric isolation would be desirable rather than air isolation to minimize resist adhesion and exposure problems.

The MNOS structures (Fig. 1) used in these experiments were prepared by: 1) performing a shallow As n+ predeposition into a (100) p-type wafer, 2) growing 1 μm of 0.15 Ω · cm n-type epi, 3) performing a metal-contact-area phosphorus n+ predeposition, 4) depositing and defining silicon-nitride which was used as a mask against an anisotropic Si etch in KOH to leave n-epi mesas with 57°-sloped sidewalls on a p-substrate plane, 5) growing a 4000-A self-aligned field oxide away from the mesa tops using the silicon-nitride mask from the previous step, 6) removing the silicon-nitride mask and growing a 40-A oxide, and 600-A-memory nitride, 7) removing all nitride surrounding the active capacitor area, and 8) depositing and patterning metal contacts and lines orthogonal to the n-epi mesa lines.

Fundamental limits to MNOS capacitor density and memory array size, assuming the lithographic definition capability of hundreds of angstroms demonstrated with electron beam exposure techniques, will be determined ultimately by signal-to-noise considerations. Fig. 4 shows the equivalent circuit of a capacitor array during READ operation with a possible amplifier connection. The effect of unselected sites along the digit lines is to shunt the current sensing node with a capacitance (n-1) C. This shunt capacitance increases the effective rise time of

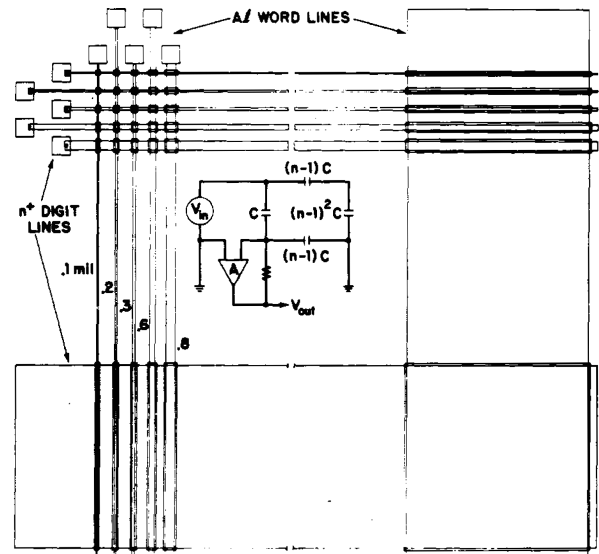

Fig. 4. Mask layout and equivalent circuit of MNOS test array.

the current sensing node thereby limiting the rate of the voltage ramp, and hence the magnitude of the output voltage. (V_{out} is inversely proportional to the time τ of the ramp, which must be greater than the time constant at the sense node.) The critical questions to be answered by future experiments are how large can the matrix edge size "n" be made, and how small the MNOS capacitor C before the available signal is overwhelmed by thermal noise or parasitic coupling effects. The results from Fig. 3 indicate satisfactory signals from an equivalent 200 × 200 array. Experiments are planned in the near future to fabricate and test matrices using 1-μm and $\frac{1}{2}$-μm lines. The successful exploitation of ultra-high-density arrays depends critically on being able to provide on-chip sense and drive circuits which can connect to such tightly packed lines with reasonable utilization of the silicon area. An important subject for investigation is the so-called fatigue problem, which limits the number of times a given location may be written. There is considerable uncertainty about both the cause and extent of this problem.

While the peripheral circuit design problems may prove to be substantial, this is potentially the highest density solid-state storage technique known to the authors, and could lead to larger cheaper memories than previously contemplated.

An Integrable MOS Neuristor Line

C. KULKARNI-KOHLI AND R. W. NEWCOMB

Abstract—**An integrable MOS design of a neuristor line simulating the conventional properties is presented, the line requiring as few as two sections to simulate the desired properties. In addition the line is low power while consuming no power during the resting state.**

I. Introduction

Since the introduction of the neuristor by Crane [1], many discrete component designs of neuristor lines have appeared in the literature [2]-[5], these lines simulating some or all of the conventional properties. But in general, these lack the integrability feature needed to obtain meaningfully large quantities of the devices, this being due to the use of inductors, tunnel diodes, extremely high values of capacitors, etc. Only recent papers [6], [7] propose neuristor lines suitable for realization by integrated circuits. The paper of Wilamowski *et al.* [6] proposes a bipolar transistor neuristor line, while the paper of Reible and Scott

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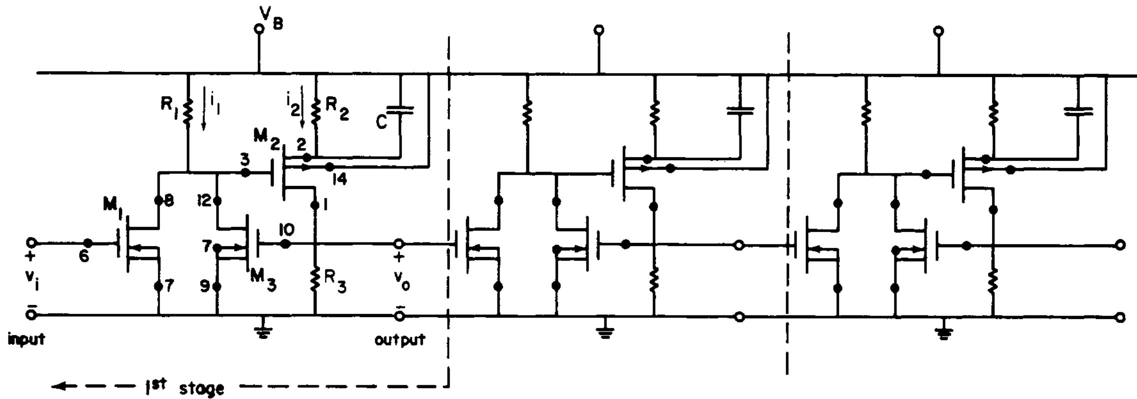

Fig. 1. Integrable neuristor line $R_1 = R_2 = 5.6\ \text{k}\Omega$, $R_3 = 2.7\ \text{k}\Omega$, $C = 100$ pF, $V_B = 10$ V. M_1 and M_3, n-channel, M_2, p-channel, MOSFET's type MC 14007CP.

[7] proposes a distributed superconductive neuristor utilizing the Josephson effect. The distributed nature of this device makes it truly a "transmission line," but the technology needs to be evolved to the precision they demand. Taking off from [6], the integrable neuristor line proposed here is of a different design, using MOSFET's, resistors and capacitors, and can be integrated using the MOS technology. The design is low power in that it does not use resistive dc paths for pulse propagation, and no power is consumed in a stage when it is in the resting state between pulses. Experimental verification on a 16 stage line has shown that it possesses the desired properties of:

a) threshold of stimulability (in pulse amplitude and width),
b) constant-pulse propagation velocity,
c) refractory period,
d) pulseshaping.

II. The Neuristor Line Section

The proposed neuristor line consists of a cascade of three-transistor sections, one section being shown in Fig. 1. In Fig. 1, the nodes are numbered as the pins on the MC 14007CP package of CMOS devices used experimentally. During the resting state (i.e., zero input voltage), all MOSFET's are turned off and the capacitors are shorted to the supply voltage V_B. Thus during the resting state there are no currents flowing in the circuit, and, therefore, no power is consumed.

Application of a positive pulse to the input, node 6, of height above V_{TH}, the threshold voltage of the stage, turns on the n-channel MOSFET M_1 which acts as an inverter. This reduces the voltage at node 3, which in turn activates the primary transistor of the stage, the p-channel MOSFET M_2. This causes the capacitor C to charge through M_2 and R_3, thereby increasing the voltage across R_3 to give the output. Through the n-channel M_3, acting as another inverter, this further reduces the voltage at node 3, causing it to rapidly drop to zero. Eventually the discharge of C causes the gate-source voltage of M_2, V_{32}, to fall below its cutoff value, dropping the output voltage to zero while recharging the capacitor and, in the passing of the input pulse, bringing the gate voltage of M_2 back to V_B. Thus the desired pulse output is obtained at node 4, and in turn is taken as the input to the next identical stage. Because the input inverter M_1 is MOSFET, no appreciable loading of one stage by the next results while, also, unidirectional propagation is achieved.

Analytically much of the behavior of the neuristor line and its properties can be roughly determined by assuming the MOS devices are either cutoff, for which the drain to source current i_{ds} is zero, or turned-on to operate in the square-law region, for which the law of i_{ds} versus gate-source voltage v_{gs} is [8, p. 46]

$$i_{ds} = K[v_{gs} - V_P]^2 \tag{1}$$

where V_P is the pinch-off voltage and K is another constant for the device. Using subscripts n and p to distinguish these constants for n-channel and p-channel devices, for n-channel MOSFETs all parameters in (1) are positive, and $v_{gs} \geqslant V_{Pn}$, and for p-channel devices these are all negative with $-v_{gs} \geqslant -V_{Pp}$. For complementary CMOS devices one desires $V_{Pn} = -V_{Pp} = V_P$ and $K_n = -K_p = K$, which we will assume, though this may not always be achieved exactly in practice. Experimentally we found $K = 0.625 \times 10^{-3}$ and $V_P = 2$ for the MC 14007CP devices used.

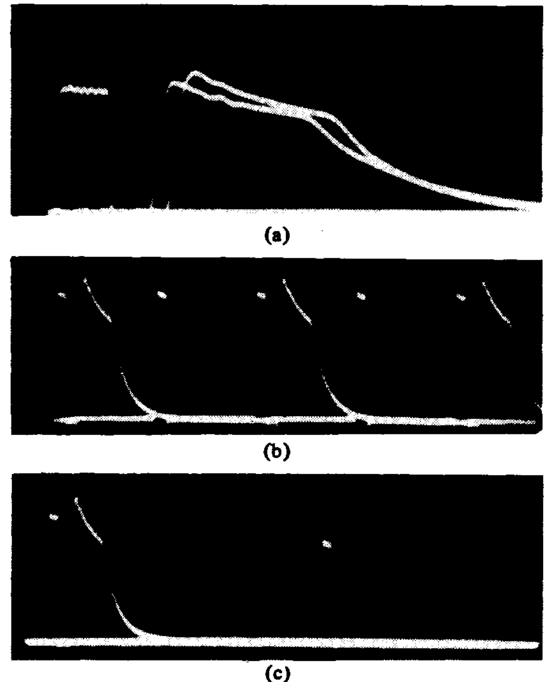

Fig. 2. Typical Waveforms. Scales: For (a) Horz. = 0.2 μs/div, Vert. = 2.0 V/div. For (b) and (c) Horz. = 1.0 μs/div, Vert. = 2.0 V/div. Input pulses (square) to first stage. Output pulses at fourth stage illustrating: (a) (Top) Delay between third and fourth stages and input. (b) Refractory period. (c) Threshold phenomena.

III. Properties

Some of the neuristor line's properties can be conveniently discussed here, though a study in depth is best considered elsewhere since they require an extensive development. Experimentally, though, several of these properties are illustrated through the oscilloscope traces of Fig. 2, where the rectangular pulse is the input to the first stage and the "action potential" pulse is the output of the fourth stage, except for the third stage output for comparison purposes in part A.

A. Propagation Delay

The pulse propagation velocity is proportional to the inverse of the delay t_d per section. As can be seen from Fig. 2(a), for the circuit constructed the total experimentally measured delay is 0.4 μs for four stages. This actually represents a delay of $t_d = 0.060$ μs per section (as also seen by the difference between the 3rd and 4th stage delays in Fig. 2(a)), except for the first section where added delay occurs due to source interaction. Theoretically this delay arises from an intrinsic delay t_i in turning on the MOSFET M_2 ($t_i \approx 40$ ns for our devices) as well as the need to charge up, through R_1, the parasitic capacitance C_p between node 3 and ground ($C_p \approx 10$ pF in our circuit). By adding in an external capacitor C_{ex} at node 3 the delay can be controlled (for

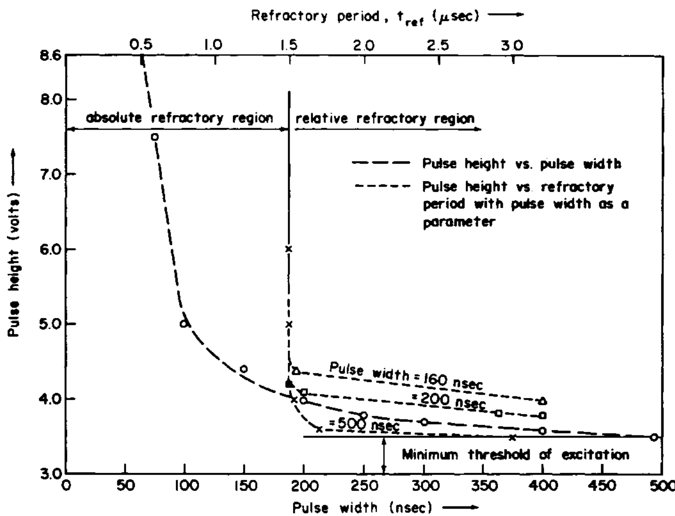

Fig. 3. Refractory period versus pulseheight and threshold voltage versus pulsewidth.

C_{ex} = 50 pF we found t_d = 140 ns). Analytically, using (1), we find

$$t_d = t_i - R_1(C_p + C_{ex}) \ln [1 - V_P\{K(V_{TH} - V_P)^2 R_1\}^{-1}] \quad (2)$$

where V_{TH} is the threshold voltage, that is the voltage at the input to the stage needed to obtain V_{TH} at the output in order to similarly trigger the next stage; for the values of Fig. 1 we measure V_{TH} = 3.5 V. Equation (2) yields t_d = 56.24 ns for Fig. 1.

B. Refractory Period

Fig. 2(b) illustrates the refractory period, t_r, which, as the distance between rectangular pulses in the figure, is 1.5 μs. Basically this is determined by the time after the input pulse vanishes needed for the gate-source voltage of M_1 to fall well below pinch-off. Consequently, t_r is determined by the pulsewidth, t_w, the time constant R_2C, the supply voltage V_B, and the pinch-off voltage V_{Pp} of the p-channel transistor M_2. Essentially, an increase in C, or V_B, will increase the refractory period, the formula we find being

$$t_r = t_w - R_2 C \ln (V_{Pp}/V_B). \quad (3)$$

For t_w = 0.5 μs, as per the action potential pulsewidth measured at 3.5 V = V_{TH} in Fig. 2(b), we calculate from (3), t_r = 1.4 μs.

In physiological experiments performed on the nerve axon, it has been found that the refractory period is sensitive to the height of the input pulse [9, p. 19]. In particular, it decreases with increasing height, until an asymptotic value is obtained, called the "absolute refractory period," during which time absolutely no input can be transmitted regardless of its height. This property has also been observed in the circuit of Fig. 1 and is shown in Fig. 3. The absolute refractory region is to the left of the asymptote of infinite slope and the width of this region is determined by (3). The region to the right of the asymptote is known as the "relative refractory period."

C. Threshold Voltage

To calculate the threshold voltage V_{TH}, we set $v_i = v_o = V_{TH}$ and assume that M_3 is cutoff when the output voltage v_o first just attains V_{TH} so that $v_{gs2} = v_{32} = -R_1 i_1 + R_2 i_2$ is controlled at that instant by transistors M_1 and M_3. This gives, on using (1),

$$V_{TH} = R_3 K[-R_1 K(V_{TH} - V_P)^2 + (R_2/R_3) V_{TH} + V_P]^2. \quad (4)$$

Equation (4), which is polynomial in V_{TH}, can be solved for V_{TH} once the circuit parameters are known. For Fig. 1 this yields V_{TH} = 3.49 V compared to the experimentally measured value of 3.5 V, as seen from Fig. 2(c).

In addition, the threshold voltage is found experimentally to vary with the width of the input pulse. This property has been observed in actual physiological studies on the nerve axon [10], and is commonly referred to as the "strength versus duration curve." This phenomena is shown in Fig. 3 as experimentally determined for the circuit of Fig. 1. The threshold voltage given by (4) is thus the minimum voltage valid for a sufficiently wide pulse.

IV. Discussion

As discussed above, and seen from Fig. 2, the neuristor line discussed here has the pulse shaping and transmission characteristics desired, while the circuit is quite suitable for large scale constructions.

The circuit can be modified in various ways. For example, similar characteristics result even if one removes M_3 from the circuit. Doing this, however, leads to a loss of control on the refractory period. By connecting two of the lines described here back to back, a bidirectional line working on similar principles can also be constructed, though a large increase in the number of elements results. This construction leads to other properties, the details of which are too extensive to cover here.

Finally, the proposed line can be interconnected to obtain neuristor logic elements in a manner as considered in earlier works [1], [11]. As the line is unidirectional, it creates other possibilities [12] for obtaining logic elements, and (further) the use of MOS structures enhances the integrable feature.

Acknowledgment

Helpful discussions with other researchers on the joint Polish-American Program on "Microelectronic Active Systems" are gratefully acknowledged.

References

[1] H. Crane, "Neuristor—A novel device and system concept," *Proc. IRE*, vol. 50, pp. 2048–2060, Oct. 1962.
[2] A. Ambroziak, "Semidistributed neuristor line using unijunction transistors," *Solid-State Electron.*, vol. 7, no. 3, pp. 259–265, Mar. 1964.
[3] A. J. Cote, "Simulating nerve networks," *Tunnel-Diode and Semiconductor Circuits*, J. M. Carroll, Ed. New York: McGraw-Hill, 1963, pp. 294–296.
[4] J. Nagumo, S. Arimoto, and S. Yoshizawa, "An active pulse transmission line simulating a nerve axon," *Proc. IRE*, vol. 50, pp. 2061–2070, Oct. 1962.
[5] A. C. Scott, "Distributed device applications of the superconducting tunnel junction," *Solid-State Electron.*, vol. 7, no. 3, pp. 137–146, Mar. 1964.
[6] B. Wilamowski, Z. Czarnul, and M. Bialko, "Novel inductorless neuristor line," *Electron. Lett.*, vol. 11, no. 15, pp. 355–356, July 24, 1975.
[7] S. A. Reible, A. C. Scott, "Pulse propagation on a superconductive neuristor," *J. Appl. Phy.*, vol. 46, no. 11, pp. 4935–4945, Nov. 1975.
[8] P. Richman, *Characteristics and Operation of MOS Field-Effect Devices*. New York: McGraw-Hill, 1967.
[9] R. Gawronski, Ed., *Bionics—The Nervous System as a Control System*, trans. by E. Lepa. Warsaw: Polish Scientific Publishers, 1971.
[10] B. I. Khodorov, *The Problem of Excitability*, trans. by B. Haigh. New York: Plenum Press, 1974.
[11] B. M. Wilamowski, "A novel concept of neuristor logic," *Int. J. Electron.*, vol. 33, no. 6, pp. 659–663, June 1972.
[12] M. B. Waldron, "Syneuristor: a device and concept," Information Systems Laboratory, Stanford University, Stanford, CA, Technical Report 6560–22, Jan. 1971.

Digital Bandpass and Bandstop Filters with Variable Center Frequency and Bandwidth

M. N. S. SWAMY AND K. S. THYAGARAJAN

***Abstract*—This paper presents a method of designing wave digital bandpass (BP) and bandstop (BS) filters whereby the center frequency and bandwidth can be independently controlled by simply changing the multiplier values. Also given are the canonic realizations for the BP and BS wave digital filters. This method of designing BP and BS wave digital filter results in a saving of coefficient registers.**

I. Introduction

It has been shown that wave digital filters have very low sensitivity with respect to multiplier coefficient changes due to finite word length [1]–[5]. In principle, wave digital filters are derived from doubly terminated LC ladder networks. One way of realizing a wave digital filter is to treat the series and shunt arm elements of the ladder as wave

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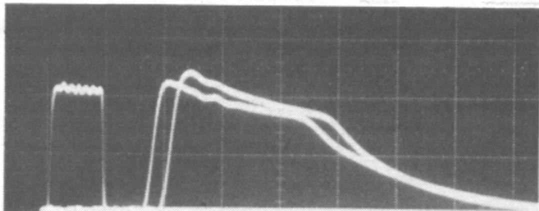

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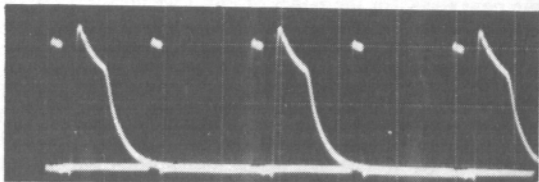

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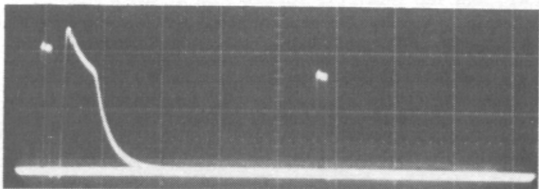

(c)

Fig. 2. Typical Waveforms. Scales: For (a) Horz. = 0.2 μs/div, Vert. = 2.0 V/div. For (b) and (c) Horz. = 1.0 μs/div, Vert. = 2.0 V/div. Input pulses (square) to first stage. Output pulses at fourth stage illustrating: (a) (Top) Delay between third and fourth stages and input. (b) Refractory period. (c) Threshold phenomena.