example, could embody a transistor exhibiting a very large phase change. The requirement for the outer conductor places a restriction on the physical size of any transistor jig, particularly at microwave frequencies where a travelling-wave phase change of 1 deg/GHz occurs over a distance of about 0·8 mm. Because all S parameters are expressed as the complex voltage ratio of two waves travelling in opposite directions, the phase change is then double this value for the same distance. If the port lengths are significant and have, say, an electrical length $\theta = \beta l$, the 2-port and 3-port matrices would be multiplied by $e^{-j2\theta}$, so that the latter

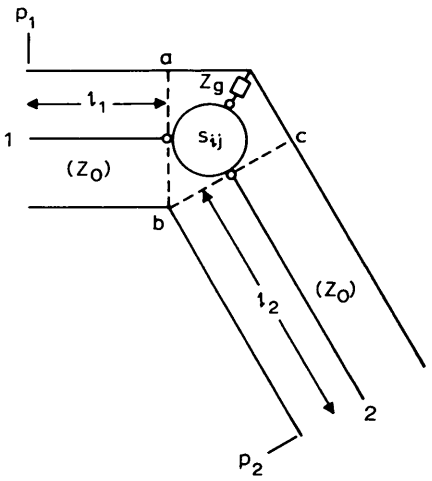

Fig. 4 *2-port jig with finite port lengths*

would then not sum to unity, and neither would the 2-port parameters transform correctly to the equivalent 3-port. Nevertheless, it is possible to derive 3-port parameters when the port lengths are significant, provided that the length and position of the third port is postulated and the junction interface satisfies the criterion previously given. For example, in Fig. 4, we have a 2-port jig with arm lengths l_1 and l_2, where the parameters in the planes p_1 and p_2 are s_{ij}''. We first transform to the planes ab and bc to obtain s_{ij}', including the effect of Z_g: thus

$$[s_{ij}'] = \begin{bmatrix} s_{11}'' e^{j2\theta_1} & s_{12}'' e^{j(\theta_1+\theta_2)} \\ s_{21}'' e^{j(\theta_2+\theta_1)} & s_{22}'' e^{j2\theta_2} \end{bmatrix}$$

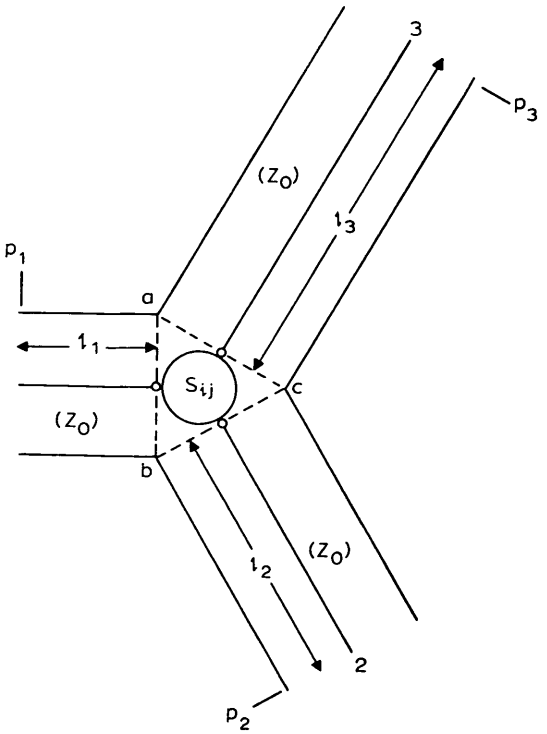

Fig. 5 *3-port jig with finite port lengths*

Provided that the phase difference between points a and c is negligibly small, we can now apply the transforms of eqns. 1*a–d* above, which eliminates the effect of Z_g and gives the equivalent 3-port parameters S_{ij} in the three planes ab, bc and ca of Fig. 5, where a, b and c are substantially equipotential points and all rows and columns of $[S_{ij}]$ sum to unity.[2] S_{ij} can now be transformed to the port reference planes p_1, p_2 and p_3 by multiplying each S parameter by the operator $e^{-j(\theta_i+\theta_j)}$, where θ_i and θ_j are the electrical lengths of the appropriate ports, and the suffix numbers correspond to the S parameter suffixes; for example,

$$S_{32}' = S_{32} e^{-j(\theta_3+\theta_2)}$$

On the other hand, the renormalisation transforms of Reference 2 are general, and the foregoing criterion is not necessary. In consequence of this, the 3-port to 2-port transforms referred to in Reference 2 are also general because the initial 3-port data contain all information relevant to the third port's parameters.

D. WOODS

Department of Chemical Physics
University of Surrey
Guildford, Surrey, England

28th June 1971

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NONLINEAR-CAPACITOR SIMULATION

Indexing terms: Simulation, Capacitors, Nonlinear-network synthesis, State-space methods

An equivalence is shown which allows nonlinear-capacitor dynamics to be placed in linear capacitors, which are then coupled through nonlinear resistive networks to simulate the desired nonlinear capacitors.

Introduction: In order to design general nonlinear circuits, it is useful to have a means of simulating arbitrary charge/voltage characteristics (e.g. capacitors). For single-valued characteristics, we show here how this can be accomplished by loading a nonlinear resistive 2-port by a unit capacitor. The result is also significant for the study of nonlinear circuits through state-space equations and is generalised to coupled capacitors.

Current decomposition: Consider a time-invariant 1-port capacitor of charge q, current i and voltage v. Assuming $q(.)$ to be a single-valued continuously differentiable function of v, we can write

$$i = \frac{dq}{dt} = \frac{dq(v)}{dv}\,\frac{dv}{dt} \quad \ldots\ldots\ldots \quad (1)$$

Physically, we can interpret the right-hand side of eqn. 1

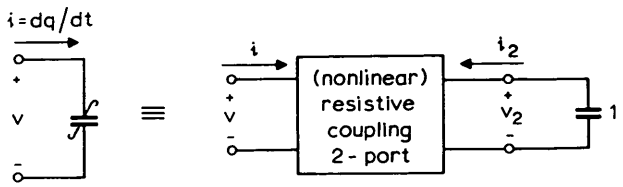

Fig. 1 *Nonlinear-capacitor simulation*

as coupling a unit capacitor, whose current is given by dv/dt, through a current multiplier whose gain is $dq(v)/dv$.

Coupling circuit: A coupling device of the type just described can be made more precise by considering it as a 2-port with the current gain just described, but also with its input and output voltages equal. Mathematically, such a 2-port is described by the general description

$$\begin{bmatrix} 0 & 0 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} v \\ v_2 \end{bmatrix} = \begin{bmatrix} 1 & \dfrac{dq(v)}{dv} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i \\ i_2 \end{bmatrix} \quad . \quad . \quad . \quad (2)$$

Since no time derivatives occur in eqn. 2, it describes a resistive 2-port which is nonlinear with $q(.)$. If we load this resistive 2-port at port 2 in a unit capacitor, for which $i_2 = -dv_2/dt$, as shown in Fig. 1, we find from eqn. 2 that the capacitor law of eqn. 1 results.

As a consequence, we have simulated a nonlinear capacitor by a linear capacitor loading a nonlinear resistive-coupling 2-port.

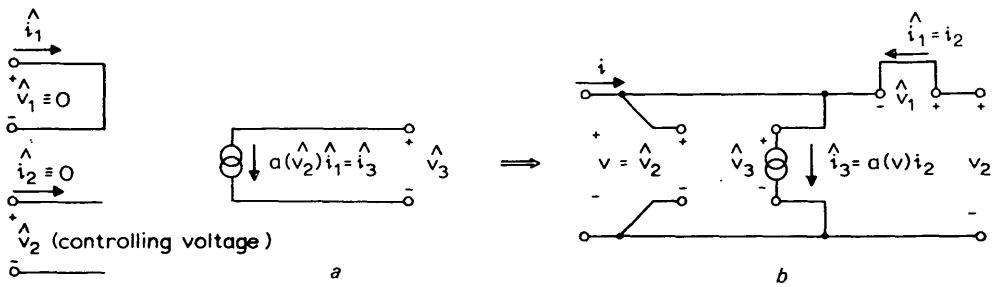

Fig. 2 *V.A.C.C.C.S. and its use*
a V.A.C.C.C.S.
b V.A.C.C.C.S. realisation of resistive coupling 2-port (eqns. 2 and 5). $a(v) = 1 - dq(v)/dv$

V.A.C.C.C.S. realisation: By introducing a voltage-adjustable current-controlled current source (v.a.c.c.c.s.), we can obtain a convenient realisation of the coupling 2-port of eqn. 2 by a more basic device. The v.a.c.c.c.s. is a (nonlinear) 3-port represented as in Fig. 2*a* and defined by the general description

$$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_1 \\ \hat{v}_2 \\ \hat{v}_3 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ a(\hat{v}_2) & 0 & -1 \end{bmatrix} \begin{bmatrix} \hat{i}_1 \\ \hat{i}_2 \\ \hat{i}_3 \end{bmatrix} \quad (3)$$

To realise the coupling 2-port of eqn. 2, we note that the change of variables

$$\begin{bmatrix} \hat{v}_1 \\ \hat{v}_2 \\ \hat{v}_3 \end{bmatrix} = \begin{bmatrix} -1 & 1 \\ 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} v \\ v_2 \end{bmatrix} \qquad \begin{bmatrix} \hat{i}_1 \\ \hat{i}_2 \\ \hat{i}_3 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 0 & 0 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} i \\ i_2 \end{bmatrix} \quad (4)$$

when substituted in eqn. 3, and after premultiplication by

$$\begin{bmatrix} 0 & 0 & -1 \\ -1 & 0 & 0 \end{bmatrix}$$

yields

$$\begin{bmatrix} 0 & 0 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} v \\ v_2 \end{bmatrix} = \begin{bmatrix} 1 & 1-a(v) \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i \\ i_2 \end{bmatrix} \quad . \quad . \quad . \quad (5)$$

which is eqn. 2 with $1-a(v) = dq(v)/dv$. Physically, the change of variables of eqn. 4 is realised by the connection of Fig. 2*b*, where the premultiplication mentioned above eqn. 5 has also been used to remove an extraneous port.

In summary, a nonlinear capacitor described by a single-valued $q(.)$ can be simulated by the v.a.c.c.c.s.-realised 2-port of Fig. 2*b*, loaded in a (linear) unit capacitor.

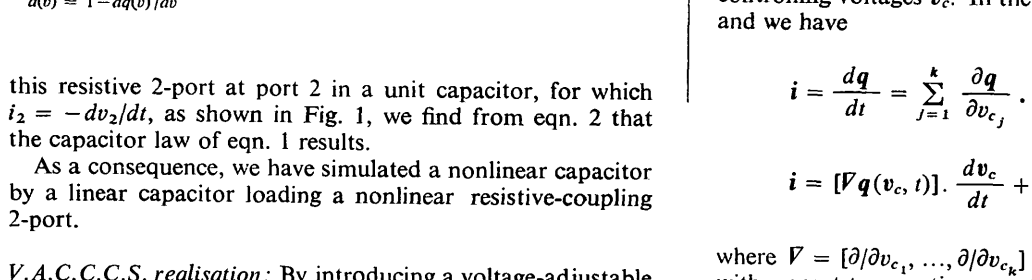

Fig. 3 *Diode capacitor simulation*

Generalisation: The above result can be generalised to n coupled capacitors whose n vector $\boldsymbol{q}$ of charges depends on k controlling voltages $\boldsymbol{v}_c$. In the time-varying case, $\boldsymbol{q} = \boldsymbol{q}(\boldsymbol{v}_c, t)$, and we have

$$\boldsymbol{i} = \frac{d\boldsymbol{q}}{dt} = \sum_{j=1}^{k} \frac{\partial \boldsymbol{q}}{\partial v_{c_j}} \cdot \frac{dv_{c_j}}{dt} + \frac{\partial \boldsymbol{q}}{\partial t} \quad . \quad . \quad . \quad . \quad (6a)$$

$$\boldsymbol{i} = [\nabla \boldsymbol{q}(\boldsymbol{v}_c, t)] . \frac{d\boldsymbol{v}_c}{dt} + \frac{\partial \boldsymbol{q}}{\partial t} \quad . \quad . \quad . \quad . \quad . \quad . \quad (6b)$$

where $\nabla = [\partial/\partial v_{c_1}, \ldots, \partial/\partial v_{c_k}]$ is the gradient (row-k vector) with respect to $\boldsymbol{v}_c$ acting on $\boldsymbol{q}(\boldsymbol{v}_c, .)$, and where we have also used $\boldsymbol{v}_c$ rather than $\boldsymbol{v}$ to indicate that the controlling voltages might be at other ports than the capacitor terminals in which $\boldsymbol{i}$ flows. Taking this into account and realising that $\partial \boldsymbol{q}/\partial t$ is an additional current source, the general description for a resistive-coupling $(n+2k)$-port network, analogous to eqn. 2, becomes

$$\begin{bmatrix} \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0}_k & \mathbf{0} \\ \mathbf{0} & \mathbf{1}_k & -\mathbf{1}_k \end{bmatrix} \begin{bmatrix} \boldsymbol{v} \\ \boldsymbol{v}_c \\ \boldsymbol{v}_2 \end{bmatrix} = \begin{bmatrix} \mathbf{1}_n & \mathbf{0} & \nabla \boldsymbol{q}(\boldsymbol{v}_c, t) & \mathbf{1}_n \\ \mathbf{0} & \mathbf{1}_k & \mathbf{0}_k & \mathbf{0} \\ \mathbf{0} & \mathbf{0}_k & \mathbf{0}_k & \mathbf{0} \end{bmatrix} \begin{bmatrix} \boldsymbol{i} \\ \boldsymbol{i}_c \\ \boldsymbol{i}_2 \\ \dfrac{\partial \boldsymbol{q}}{\partial t} \end{bmatrix} \quad (7a)$$

(here $\mathbf{1}_k$ is the $k \times k$ identity and $\mathbf{0}_k$ the $k \times k$ zero matrix). When loaded in k unit capacitors, $\boldsymbol{i}_2 = -d\boldsymbol{v}_2/dt$, and tapped into the k controlling voltages $\boldsymbol{v}_c$, eqn. 6*a* results. In the most practical case, where controlling voltages are port voltages, $\boldsymbol{v}_c = \boldsymbol{v}$ (hence $k = n$), eqn. 7*a* simplifies to

$$\begin{bmatrix} \mathbf{0}_n & \mathbf{0}_n \\ \mathbf{1}_n & -\mathbf{1}_n \end{bmatrix} \begin{bmatrix} \boldsymbol{v} \\ \boldsymbol{v}_2 \end{bmatrix} = \begin{bmatrix} \mathbf{1}_n & \nabla \boldsymbol{q} & \mathbf{1}_n \\ \mathbf{0}_n & \mathbf{0}_n & \mathbf{0}_n \end{bmatrix} \begin{bmatrix} \boldsymbol{i} \\ \boldsymbol{i}_2 \\ \dfrac{\partial \boldsymbol{q}}{\partial t} \end{bmatrix} \quad . \quad (7b)$$

which reduces to eqn. 2 in the time-invariant ($\partial \boldsymbol{q}/\partial t = \mathbf{0}_n$) 1-port-capacitor case ($n = 1$).

Eqns. 7 are realisable by v.a.c.c.c.s.s and a voltage-adjustable current for $\partial \boldsymbol{q}/\partial t$, in a similar manner as before; however, the current gains may now each depend on up to k voltages.

Example: As an illustration, let

$$q(v) = Kv/[V - v]^N \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (8a)$$

as for a tunnel diode, where K, V and N are constants.

Then

$$\frac{dq}{dv} = K\frac{V+[N-1]v}{(V-v)^{N+1}} \quad \ldots\ldots\ldots \quad (8b)$$

and Fig. 3 results.

Discussion: By making a derivative expansion, we have shown how nonlinear capacitors can be simulated by using voltage-adjustable current-controlled current sources loaded in unit capacitors. The result allows for extension to coupled and time-variable capacitors whose charges are controlled by arbitrary voltages not necessarily located across the capacitors, as shown by eqns. 6 and 7.

The interest in such a simulation is rather broad. First, one expects that, through appropriate electronic circuitry, a large class of voltage-controlled gains can be realised, giving a convenient means of obtaining useful nonlinear capacitors. The class of electronically realisable v.a.c.c.c.s. gains, and hence nonlinear capacitors, is presently under investigation. Secondly, isolation of the dynamics of a nonlinear capacitor into a unit capacitor is extremely useful for state-variable analysis and design. When the equivalences set up here are used, it is a relatively easy matter to set up the state-variable equations $\dot{x} = f(x, u)$ and $y = g(x, u)$ for nonlinear networks. This is of special interest for computer-aided analysis and will be reported soon.

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R. W. NEWCOMB* *1st July 1971*
O. A. SERIKI

Electrical Engineering Department
University of Lagos, Lagos, Nigeria

* R. W. Newcomb is on leave from the University of Maryland, College Park, Md. 20742, USA

THE MIXED DOUBLE: A NEW BALANCED INPUT STAGE

Indexing term: D.C. amplifiers

A new circuit has been developed for use as the input stage in low-level d.c. amplifiers.

In low-level d.c. amplifiers, it is virtually essential to use a pair of transistors in the input stage to balance out the relatively large and temperature-sensitive base–emitter offset voltage. The well known long-tailed pair[1] is commonly used, but, in amplifiers with single-ended inputs, it has certain disadvantages, notably that the input is not at earth potential unless a split supply is used, and that the gain is half that of the equivalent single transistor.

A new circuit has been developed in which both these disadvantages have been overcome. The circuit, the 'mixed double', is shown in Fig. 1A.

The input transistor Tr_1 is connected as a common-collector stage with $V_{cb} = 0$, and drives Tr_2, which operates as a common-emitter stage. The voltage gain of Tr_1 is slightly less than 1. Its frequency response is not important (if necessary it could be bypassed completely by a capacitor), but it should have a high current gain to minimise the input offset current. Conversely, the current gain of Tr_2 is not very important, since it is voltage-fed, but its high-frequency current gain determines the overall frequency response. Optimum temperature compensation will nominally be obtained when the base–emitter voltages of the two transistors are equal. For similar transistors, the collector currents would then be equal, but Tr_2 may, with advantage, be chosen to operate at a higher current than Tr_1.

With arbitrarily chosen pairs of transistors, types 2N4250 and 2N3565, temperature coefficients of 70–100 μV/deg C were obtained over the 20–50°C range. This is markedly worse than the performance of a conventional input stage

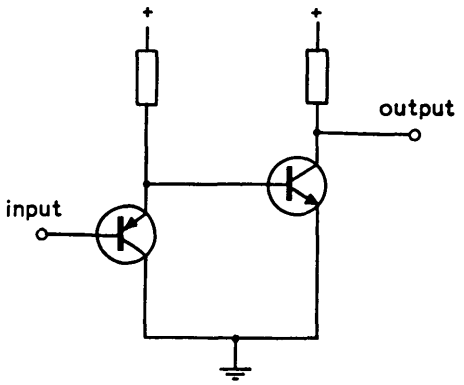

Fig. 1A *Basic circuit*

using a matched pair of transistors, but is adequate for many laboratory applications. Much better results would be expected if the design of the transistors were optimised for this application.

The advantages of this connection are demonstrated by the circuit shown in Fig. 1B. This is a simple d.c. millivoltmeter operating from a 2·7 V battery, and giving full output for 10 mV input. It has a loop gain of about 25 dB, an input impedance of about 100 MΩ and an input offset current of about 5 nA. Linearity is better than 99% of full-scale deflection. The meter pointer is offset as far as possible to the left, so that a significant current is flowing in Tr_4 when the meter reads zero. Resistor R_6 provides a relatively

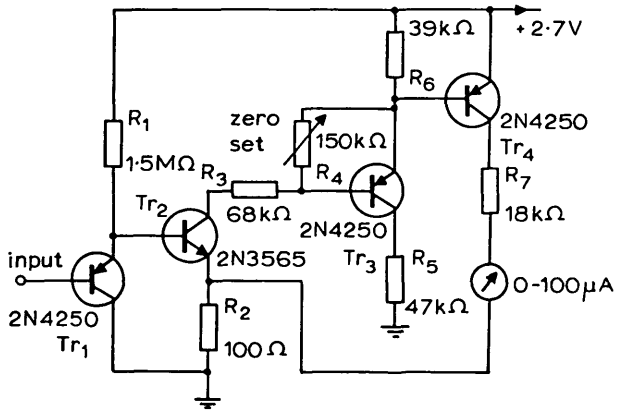

Fig. 1B *Simple d.c. millivoltmeter*

constant operating current for Tr_3, while resistors R_3, R_5 and R_7 prevent excessive currents flowing under overload conditions. The temperature coefficient is about 200 μV/deg C and is due mainly to the uncompensated second stage.

R. H. S. RIORDAN *5th July 1971*

Division of Mechanical Engineering
Commonwealth Scientific & Industrial Research Organisation
Highett, Victoria, Australia

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