

# A Computer-Oriented Technique for Determining the State-Variable Equations for Admittance Descriptions

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J. A. Miller and R. W. Newcomb

## INTRODUCTION

After a study of existing computer routines for obtaining the state-space equations from a given network,<sup>(1),(2)</sup> it was apparent that such routines were rather complicated for many applications.

Presently, a simple, general method for determining the state equations for a network is available<sup>(3)</sup>—a method that does not have the restriction that the admittance description exist. However, this procedure can be simplified for the very large percentage of practical circuits where an admittance description does exist. This latter can easily be found by computer routines<sup>(4)</sup> that form an indefinite admittance matrix for the whole system and reduce it to a definite admittance matrix for

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the  $n$ -port network. Knowing this, we can profitably develop a simple algorithm based on the admittance description for determining the state-space equations.

### THE ADMITTANCE DESCRIPTION

The problem we consider is to find state equations of the form

$$\dot{\mathbf{x}} = \mathbf{F}\mathbf{x} + \mathbf{G}\mathbf{u} \quad (1a)$$

$$\mathbf{y} = \mathbf{H}\mathbf{x} + \mathbf{J}\mathbf{u} \quad (1b)$$

for a linear  $n$ -port network (given in schematic form) that contains a finite number of resistors, capacitors, inductors, transformers, gyrators, and active devices. Since we are working with the admittance, we choose  $\mathbf{u} = \mathbf{v}$  and  $\mathbf{y} = \mathbf{i}$ . Through the use of the inductor equivalent network shown in Fig. 1A, the original  $n$ -port network can be transformed to an  $(n + c)$ -port network from which all the dynamic elements have been extracted as capacitors to leave a network with only algebraic constraints. In order to analyze networks including transformers using an indefinite admittance program, the transformer equivalent of Fig. 1B is used. It is also understood that all the active devices (such as transistors) are replaced by their equivalent circuits (for example, hybrid- $\pi$ , as described in Ref. [5], p. 259) and the dynamic elements removed from them in the manner just described. This resultant  $(n + c)$ -port network is as shown in Fig. 2.

This  $(n + c)$ -port network can now be described in an  $\mathbf{AV} = \mathbf{BI}$  manner (see Ref. [6], p. 47) such that  $\mathbf{Y}_r\mathbf{V} = \mathbf{I}$ , where  $\mathbf{Y}_r$  is an  $(n + c) \times (n + c)$  admittance matrix describing only the resistive network, and  $\mathbf{V}$  and  $\mathbf{I}$  are (time-domain) column matrices with  $n + c$  elements. An example problem will be worked out subsequent to the presentation of the algorithm to demonstrate the following steps in detail.

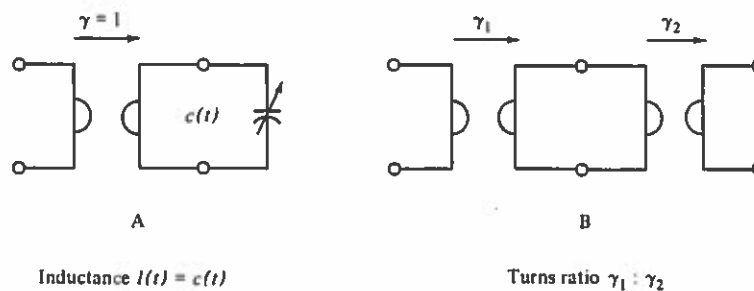


FIG. 1. Equivalents using gyrators. A—Inductor equivalent. B—Transformer equivalent.

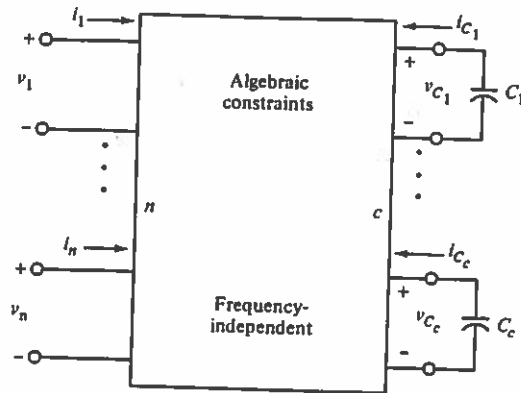


FIG. 2. Dynamic element extraction.

Let us arrange  $V$  and  $I$  as follows:

$$\begin{bmatrix} Y_{nn} & Y_{nc} \\ Y_{cn} & Y_{cc} \end{bmatrix} \begin{bmatrix} v \\ V_c \end{bmatrix} = \begin{bmatrix} i \\ I_c \end{bmatrix} \quad (2)$$

such that  $v$  and  $i$  refer to the original terminal ports and  $V_c$  and  $I_c$  refer to the dynamic element ports. Then by simple rearrangement,  $YV = I$  can be brought into the following form (where  $1_n$  is the  $n \times n$  identity matrix):

$$\begin{matrix} n \{ \\ c \{ \end{matrix} \begin{bmatrix} Y_{nn} & Y_{nc} & -1_n & 0 \\ Y_{cn} & Y_{cc} & 0 & -1_c \end{bmatrix} \begin{bmatrix} v \\ V_c \\ i \\ I_c \end{bmatrix} = 0 \quad (3)$$

Carrying out the multiplication of equation (3) and rearranging gives

$$\begin{matrix} n \{ \\ c \{ \end{matrix} \begin{bmatrix} 0 \\ -I_c \end{bmatrix} = - \begin{bmatrix} Y_{nc} \\ Y_{cc} \end{bmatrix} V_c - \begin{bmatrix} Y_{nn} \\ Y_{cn} \end{bmatrix} v + \begin{bmatrix} i \\ 0 \end{bmatrix} \quad (4)$$

To form the state variables, we use the general approach of considering charges on capacitors and fluxes in inductors (Ref. [7], p. 391); since we have removed all the inductors, we need only consider the capacitor charges. That is, let

$$x = CV_c \quad (5)$$

where  $C$  is the  $c \times c$  diagonal matrix of capacitances (note the extraction numbering in Fig. 2 where  $c_1 = n + 1$ ). Assuming  $C$  is nonsingular (which will be true for all  $t$  in the time-invariant case), equation (5) can be solved

for  $V_c$  as follows:

$$V_c = C^{-1}x \quad (6)$$

Having already chosen  $x$  as the state variable matrix defined by (5), we then notice that

$$\dot{x} = -i_c = \frac{dCv_c}{dt}$$

for all the dynamic elements; or in matrix form,

$$\dot{x} = -I_c \quad (7)$$

Using the definitions of (5) and (7), we can go to (4) and make the appropriate substitution to give us the final form

$$\begin{matrix} n \\ c \end{matrix} \left\{ \begin{matrix} 0 \\ \dot{x} \end{matrix} \right\} = - \begin{matrix} Y_{nc} \\ Y_{cc} \end{matrix} [C]^{-1}x - \begin{matrix} Y_{nn} \\ Y_{cn} \end{matrix} v + \begin{matrix} i \\ 0 \end{matrix} \quad (8)$$

Recalling our previous definition of input and output variables, the equivalence for equation (1) is, by simple rearrangement of (8),

$$\dot{x} = Fx + Gu \equiv \dot{x} = -[Y_{cc}][C]^{-1}x - [Y_{cn}]v \quad (9a)$$

$$y = Hx + Ju \equiv i = [Y_{nc}][C]^{-1}x + [Y_{nn}]v \quad (9b)$$

If currents are desired as input variables, the first  $n$  rows of equation (8) can be solved for the voltages in terms of the currents and the state variables and then substituted back into the last  $c$  rows of (8), such that the impedance matrix is determined.

### AN EXAMPLE

As a preliminary we remark that the gyrator of Fig. 3 is assumed to have, by definition, the two-port admittance matrix

$$Y = \begin{bmatrix} 0 & 1/\gamma \\ -1/\gamma & 0 \end{bmatrix} \quad (10a)$$

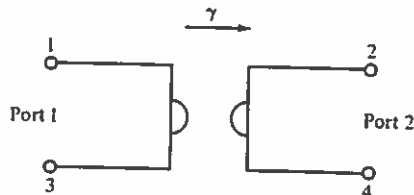


FIG. 3. Floating gyrator.

(where  $\gamma = \text{gyration resistance}$ ), from which the indefinite admittance

$$Y_{\text{ind}} = \begin{bmatrix} 0 & 1/\gamma & 0 & -1/\gamma \\ -1/\gamma & 0 & 1/\gamma & 0 \\ 0 & -1/\gamma & 0 & 1/\gamma \\ 1/\gamma & 0 & -1/\gamma & 0 \end{bmatrix} \quad (10b)$$

where the terminal numbering is that of Fig. 3. In a similar manner the indefinite admittance matrix for a voltage-controlled current source is found.

Now consider the time-invariant circuit of Fig. 4A. After the appropriate equivalence substitution for the inductor and the extraction of the capacitor, the  $(n + c)$ -port resistance network is as in Fig. 4B (in this case,  $n = c = 2$ ).

For this four-port network with two capacitors the general form of equation (8) is

$$\begin{bmatrix} 0 \\ 0 \\ \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = - \begin{bmatrix} Y_{13} & Y_{14} \\ Y_{23} & Y_{24} \\ Y_{33} & Y_{34} \\ Y_{43} & Y_{44} \end{bmatrix} \begin{bmatrix} 1/C_1 & 0 \\ 0 & 1/C_2 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} - \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \\ Y_{31} & Y_{32} \\ Y_{41} & Y_{42} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} i_1 \\ i_2 \\ 0 \\ 0 \end{bmatrix} \quad (11)$$

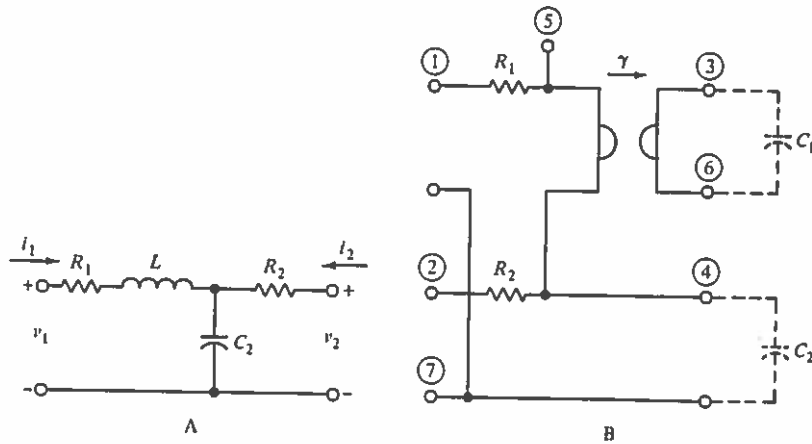


FIG. 4. A—Time-invariant circuit. B—Equivalent circuit.

The indefinite admittance matrix for the network of Fig. 4B, using  $\gamma^2 C_1 = L$  and ignoring the zeros from node 7, becomes

$$Y_7 = \begin{bmatrix} 1/R_1 & 0 & 0 & 0 & -1/R_1 & 0 \\ 0 & 1/R_2 & 0 & -1/R_2 & 0 & 0 \\ 0 & 0 & 0 & 1/\gamma & -1/\gamma & 0 \\ 0 & -1/R_2 & -1/\gamma & 1/R_2 & 0 & 1/\gamma \\ -1/R_1 & 0 & 1/\gamma & 0 & 1/R_1 & -1/\gamma \\ 0 & 0 & 0 & -1/\gamma & 1/\gamma & 0 \end{bmatrix} \quad (12)$$

which can easily be found by adding indefinite matrices for each separate component and then grounding node 7. For example, the gyrator indefinite matrix of (10b) occurs, after an interchange of row and column 1 with rows and columns 2 and 3, in the lower right of (12); that is,  $Y_{ind}$  can simply be inserted into the indefinite  $Y$  for the complete  $(n + c)$ -port, which has been calculated with all the inductor ports open-circuited. Further, since only the voltage difference on  $C_1$  is of importance, we are free to set  $V_6 = 0$ , in which case the last row and column of  $Y_7$  can be deleted. Since node 5 is an internal node, it is to be eliminated. We then have

$$\begin{bmatrix} Y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V \\ v_5 \end{bmatrix} = \begin{bmatrix} I \\ 0 \end{bmatrix} \quad (13)$$

where

$$y_{12} = \begin{bmatrix} -1/R_1 \\ 0 \\ -1/\gamma \\ 0 \end{bmatrix} \quad y_{21} = [-1/R_1, 0, 1/\gamma, 0] \quad y_{22} = [1/R_1]$$

$V$  and  $I$  are the voltage and current variables of the four-port network.

Solving (13) to obtain the form of  $Y_r V = I$  gives

$$[Y_{11} - y_{12}y_{22}^{-1}y_{21}] V = I \quad (14)$$

The definite admittance  $Y_r$  for this four-port network is then

$$Y_r = \begin{bmatrix} 0 & 0 & 1/\gamma & 0 \\ 0 & 1/R_2 & 0 & -1/R_2 \\ -1/\gamma & 0 & R_1/\gamma^2 & 1/\gamma \\ 0 & -1/R_2 & -1/\gamma & 1/R_2 \end{bmatrix} \quad (15)$$

From (15) and the last  $c = 2$  rows of (11), equation (1a) is found immediately to be

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} -R_1/\gamma^2 C_1 & -1/\gamma C_2 \\ 1/\gamma C_1 & -1/R_2 C_2 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 1/\gamma & 0 \\ 0 & 1/R_2 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \quad (16a)$$

and equation (1b) to be

$$\begin{bmatrix} \dot{i}_1 \\ \dot{i}_2 \end{bmatrix} = \begin{bmatrix} 1/\gamma C_1 & 0 \\ 0 & -1/R_2 C_2 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 1/R_2 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \quad (16b)$$

If it is desired to consider the output as the voltage across the resistor  $R_2$ , when  $v_2 = 0$ , we can find the output from the last row of (16b) multiplied by  $R_2$  (when  $v_2 = 0$ ). Consequently, the method can be used to calculate desired transfer functions by proper insertion of ports in a given structure.

It should be clear that the method just described is extremely simple and very easily programmed for computer operation. The main characteristic of this method's simplicity is that no transformations are necessary to bring the state matrices to proper form, and only simple matrix operations are needed. The method always works if the admittance matrix  $Y$ , exists. The restriction that the nondynamic admittance description exists generally means that no capacitor loops or inductor wyes are allowed, nor poles at infinity.<sup>(8)</sup> The situation with regard to capacitor loops can often be handled by the use of the equivalents of Fig. 5. Note that to be useful this equivalence requires the presence of resistive components associated with the original delta, as would occur for example in transistor hybrid-pi models [no admittance matrix exists for the algebraic coupling portion of Fig. 5C]. Similarly, inductor wyes can be treated as in Fig. 6. The restriction of no poles at infinity means the absence of capacitive paths across any of the original  $n$  ports, but it can easily be relaxed by

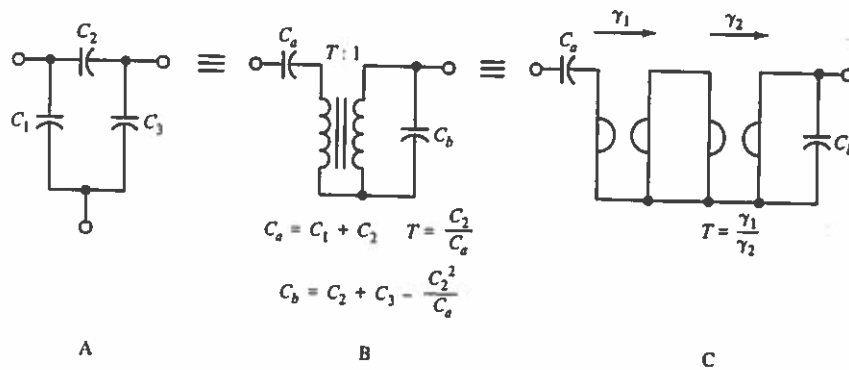


FIG. 5. Capacitor delta equivalent.

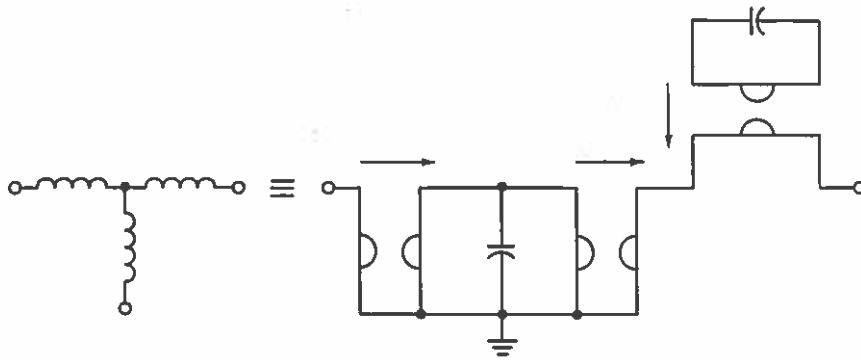


FIG. 6. Inductor wye equivalent.

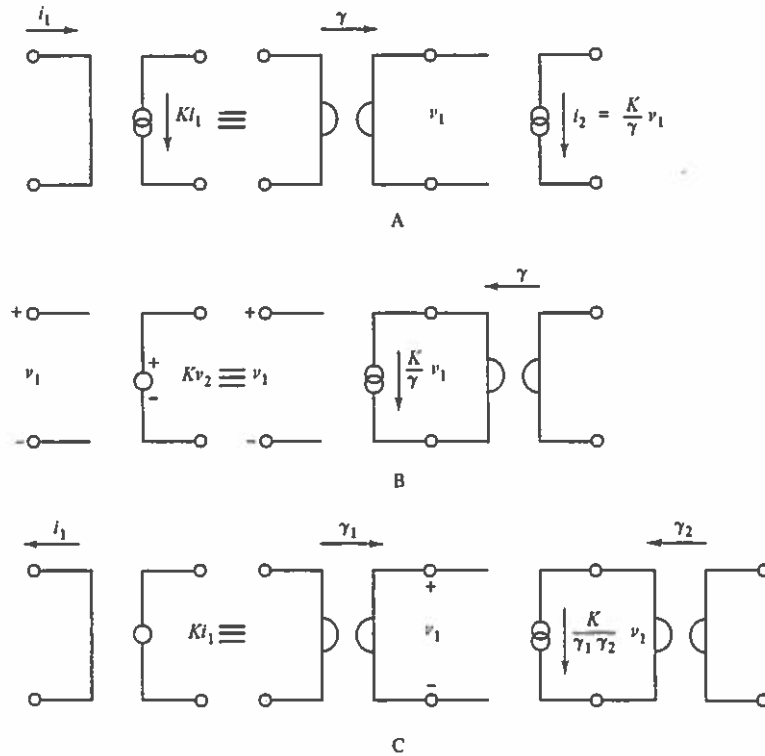


FIG. 7. Controlled-source equivalents. A—Current-controlled current source. B—Voltage-controlled voltage source. C—Current-controlled voltage source.



adding a term  $K\dot{u}$  to equation (1b).<sup>[9]</sup> Alternatively, if only numerical values for transfer functions, and so forth, are desired, a series variable resistor may be inserted at the ports of interest and then reduced to some limiting value that does not affect the impedance level in the original network but allows for an admittance description.

One should, of course, insure that the proper resistive network matrix  $Y_r$  is used. Thus, if  $Y_r$  is formed from the indefinite matrix, the capacitor voltages may be differences of node-to-datum voltages, in which case differences of columns from the indefinite matrix will be required along with the deletion of appropriate rows and columns needed to isolate the ports. If all capacitors are grounded these extra steps are not required.

It is to be noted that voltage-controlled current sources are easily handled in a straightforward manner, and therefore, we suggest that the hybrid- $\pi$  model be used for transistor equivalent circuits. Other controlled sources can be handled by the use of gyrators to convert to the dual and/or by cascade connections, as shown in Fig. 7. Independent current sources can be handled by the addition of a term  $i_s$  to the right of equation (1b), with  $i_s$  found through superposition and Norton's theorem. Independent voltage sources are simply brought out as input ports (or converted to  $i_s$  with gyrators). A program written using the algorithmic structure described here has satisfactorily performed on the simple circuits analyzed thus far. Furthermore, this procedure is now being implemented in a symbolic manner using a combination of the symbolic languages Snobol and Altran to give the state-variable matrices in terms of the explicit element names of the network under consideration.

#### CONCLUDING REMARK

*It is not enough to cover the rock with leaves.  
We must be cured of it by a cure of the ground  
Or a cure of ourselves, that is equal to a cure  
Of the ground, a cure beyond forgetfulness.  
And yet the leaves, if they broke into bud,  
If they broke into bloom, if they bore fruit,  
And if we ate the incipient colorings  
Of their fresh culls might be a cure of the ground.*  
—Stevens<sup>[10]</sup>

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