ON THE TRANSFER FUNCTION TEMPERATURE INSENSITIVITY OF LINEAR INTEGRATED CIRCUITS*

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Abstract. Using the general result of Blostein that the sum of the sensitivities with respect to element values add to a constant it is shown that the temperature sensitivity of a transfer function realized by a linear completely integrated circuit is essentially independent of the circuit configuration; it depends only upon the transfer function and the material used. From the developed theory one can determine possible means of investigation for any improvements in temperature sensitivity.

"In a field of inquiry in which some measure of understanding has already been achieved by the establishment of empirical laws, a good theory will deepen as well as broaden that understanding." [1, p.75]

I. INTRODUCTION

Many active synthesis techniques are becoming available for the design of linear integrated circuits to realize a given transfer function [2] - [9]. In many cases of interest the results are judged and compared upon their sensitivity performance with, in fact, a sensitivity analysis almost always performed before practically considering a given design. When such sensitivity analyses are actually performed they are generally with respect to an active element gain or passive element values. However, for completely integrated circuits probably the most significant parameter with respect to which sensitivity seems important is temperature. Since a theoretical study of the overall temperature sensitivity is rarely carried out, one could claim that as yet the various studies so far made give inadequate information for use of the circuits in completely integrated structures. Here, however, we show that such is not generally the case; to a high degree of accuracy the temperature sensitivity of a given transfer function H(p) depends primarily upon the material used in the fabrication and H(p) itself and not upon the circuit used. Although the result is not completely exact, it is true to a good degree of accuracy, that is, to what one might refer to as first order. Consequently, for the synthesis of linear integrated circuits the sensitivities already evaluated in the literature appear to be the most valuable in that they show the designer where he has freedom to improve the circuit performance. For example, though to first order the effects of temperature can not be compensated without external components, the effects of mask misalignment and non-optimum layout can be minimized by a proper choice of circuit configuration. The result is also such that it generally shows how second order effects, with regard to the temperature sensitivity of transfer functions, can be minimized. To obtain the final conclusion we first develop some theory.

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II. GENERAL RESULT

Consider as given a specific voltage (or current) transfer function H(p). This transfer function is dependent upon all capacitances in the circuit as well as upon all conductances, including gyration conductances and transconductances of active elements. Because we are interested in integrated circuits we can ignore inductances, while for transistors we need consider only conductances and capacitances, for example through the use of pi or hybrid-pi models. If we denote the dependence by $H = H(G_1,\ldots,G_g,C_1,\ldots C_c,p)$, where G_i and C_j are the ith conductance (possibly a transconductance) and jth capacitance, respectively, then following Blostein [10, p.22] we can admittance scale through a scale factor a to obtain

$$H(aG_1,\ldots,aG_g,aC_1,\ldots,aC_c,p) = H(G_1,\ldots,G_g,C_1,\ldots,C_c,p) \tag{1}$$

If we define the sensitivity S_x^X of the quantity X to a parameter x through

$$S_x^X = \frac{x}{X}\frac{\partial X}{\partial x} \tag{2}$$

we find, by differentiating with respect to a, setting a = 1, and dividing by H

$$\sum_{i=1}^{g} S_{G_i}^H + \sum_{j=1}^{c} S_{C_j}^H = 0 \tag{3}$$

Identical reasoning applies to the magnitude yielding

$$\sum_{i=1}^{g} S_{G_i}^{|H|} + \sum_{j=1}^{c} S_{C_j}^{|H|} = 0 \tag{4}$$

At this point we comment that if an admittance H(p) is considered, rather than a voltage or current transfer function, then the results are the same except the right hand zeros are replaced by ones in (3) and (4). To continue, let us perform a frequency scaling by a factor b

$$H(G_1,\ldots,G_g,bC_1,\ldots,bC_c,p) = H(G_1,\ldots,G_g,C_1,\ldots,C_c,bp) \tag{5}$$

Differentiating with respect to b, setting b = 1, and dividing by H gives [6, p.23]

$$\sum_{j=1}^{c} S_{C_j}^{H} = p\,\frac{d \ln H}{dp} = S_p^{H(p)} \qquad (6)$$

with the same results holding if H is replaced by $|H|$. Combining this last result with (3) yields

$$\sum_{i=1}^{g} S_{G_i}^{H} = -S_p^{H} \qquad (7)$$

Let us next evaluate the sensitivity of H with respect to (absolute) temperature T; we find

$$S_T^H = \sum_{i=1}^{g} S_{G_i}^{H} S_T^{G_i} + \sum_{j=1}^{c} S_{C_j}^{H} S_T^{C_j} \qquad (8)$$

Again an identical expression holds when H is replaced by $|H|$. If it is true that

$$S_T^{C_j} = S_T^{C_k} = S_T^C \text{ and } S_T^{G_j} = S_T^{G_k} = S_T^G \quad \text{for all } j, k \qquad (9)$$

then, by simply combining the above equations, we arrive at

$$S_T^H = S_p^{H(p)}[S_T^C - S_T^G] \qquad (10a)$$

$$S_T^{|H|} = S_p^{|H(p)|}[S_T^C - S_T^G] \qquad (10b)$$

For immittance transfer functions the results are simply modified by the addition or subtraction of S_T^G. We will see that (9) is valid to a reasonable degree of approximation for normal operation of most completely integrated circuits, in which case (10), our approximate but main result, says that the transfer function temperature sensitivity depends primarily upon the transfer function and the material from which the components are constructed. We next evaluate the temperature sensitivities for these latter.

III. CAPACITANCE AND CONDUCTANCE SENSITIVITIES

Let us first consider a completely monolithic device. In this case the capacitance sensitivity can be calculated to a good degree of approximation as follows. For an abrupt junction the capacitance is given by [11, pp.8 and 61] [12, p.97]

$$C = \frac{\epsilon A}{d} = KA[V+v_{bi}(T)]^{-1/2} \qquad (11a)$$

$$v_{bi}(T) = \frac{kT}{q} \ln \frac{N_a N_d e^{qV_g/kT}}{\textcircled{k} T^3} \qquad (11b)$$

where the parameters are: ϵ = dielectric constant, A = junction area, d = junction width, K = constant, V = applied voltage, v_{bi} = built in voltage, k = Boltzman's constant, q = electron charge, $\textcircled{k}$ = proportionality constant, N_a = acceptor level, N_d = donor level, V_g = gap voltage (which has a slight temperature dependence here ignored). Directly using (2) gives for the capacitance sensitivity

$$S_T^C = \frac{T}{C}\frac{\partial C}{\partial T} = \frac{1}{2}\,\frac{kT}{q}\,\frac{[3+\ln \textcircled{k} T^3 / N_a N_d]}{[V+v_{bi}(T)]} \qquad (12)$$

A typical value for silicon is $S_T^C \approx 0.2$ [for $\textcircled{k} T^3 \approx 10^{40}$, $N_a N_d \approx 10^{30}$, $kT/q \approx 0.026$, V = 1, $v_{bi} \approx 0.6$]. Note that S_T^C is quite small and independent of the layout configuration. It does depend somewhat on the material used and there is a voltage dependence which shows that parasitics enter slightly differently than the primary capacitors. In any event the first of (9) is reasonably well satisfied, and as we next see, $|S_T^C| < |S_T^G|$.

Consider now a diffused resistor. Over the range of -100° C to +100° C the conductance is reasonably accurately given by [13, p.28] [14, p.70] [15, pp.67 and 74]

$$G = \frac{\sigma A}{\ell} = \frac{qNA}{\ell}\mu, \quad \mu \approx KT^{-m} \qquad (13)$$

where: σ = conductivity, A = cross sectional area, ℓ = length, q = electron charge, N = acceptor or donor level, μ = mobility of impurity carriers, K = proportionality constant, m = temperature exponent (dependent upon the material considered, m = 2.5±0.1 for n type silicon and m = 2.7±0.1 for p type silicon [16, p.667]). Then the conductance sensitivity of diffused resistors is given by

$$S_T^G = \frac{T}{G}\frac{\partial G}{\partial T} \approx -m \qquad (14)$$

Again the sensitivity is independent of the structure used, verifying (9) for resistors, and we note that $|S_T^G| > |S_T^C|$.

Next let us investigate monolithic transistors. Here one does not yet have a complete theory of how to proceed, but it appears to us that the Ebers-Moll model [17, p.1763] coupled with the appropriate junction diode capacitances is physically the most basic for determination of temperature behavior.

As seen at (12) the junction capacitances are relatively small, so we can restrict our attention to the more important Ebers-Moll model quantities. We have [18, p.407]

$$i_E = a_{11}(e^{qv_{EB}/kT} - 1) + a_{12}(e^{qv_{CB}/kT} - 1) \qquad (15a)$$

$$i_C = a_{12}(e^{qv_{EB}/kT} - 1) + a_{22}(e^{qv_{CB}/kT} - 1) \qquad (15b)$$

For our purposes the terms determined by v_{CB} are negligible while exp $(qv_{EB}/kT) \gg 1$. Since we are interested in signal variations for the transfer function we let $i_E = I_E + \Delta i_E$, etc., thus

$$I_E \approx a_{11}\, e^{qV_{EB}/kT}\,,\quad I_C \approx a_{12}\, e^{qV_{EB}/kT} \qquad (16a)$$

$$\Delta i_E \approx I_E\, q\, \Delta V_{EB}/kT\,,\quad \Delta i_C \approx I_C\, q\, \Delta V_{EB}/kT \qquad (16b)$$

Further [18, pp.742, 746]

$$\Delta i_C \approx \left(\frac{I_C}{I_E}\right) \Delta i_E = -\frac{H_d}{H_d+H_c}\,\Delta i_E = \frac{-1}{1+1/\beta_o}\,\Delta i_E \qquad (16c)$$

Therefore if we define g_E and g_m by

$$\Delta i_E = g_E\ \Delta v_{EB},\ \Delta i_c = -g_m\, \Delta v_{EB} \qquad (16d)$$

we have for the conductances of interest

$$g_E = \frac{q}{kT}\, I_E\,,\ g_m = \left(\frac{1}{1+1/\beta_o}\right)\frac{q}{kT}\, I_E \qquad (16e)$$

Now generally I_E, the emitter bias current, is fixed by a bias voltage and a set of resistors "external" to the transistor. In such a case I_E varies with temperature as T^{-m} as (13) shows. To finish the calculation we need the sensitivity of β_o to temperature.

The sensitivity of current gain β_o seems theoretically unavailable nor does it seem to have been studied much; an investigation of available graphical data shows

$$S_T^{\beta_o} \approx +1 \qquad (17)$$

over a wide range of temperature and current gains (for example, the planar silicon epitaxial passivated npn transistors 2N3402 and 2N3417's yield the result of (17) for $70 < \beta_o < 550$ over the range -30^o C to $+80^o$ C; analysis of another available β_o versus T characteristic [19, p.143] gives a range of 1.7 to 2.6 for the right side of (17), but use of these latter larger numbers yield results inconsistent with another (g_π) sensitivity available from the same curves [19, p.143]). For some diffused configurations operating near room temperature the temperature sensitivity of β_o can be analytically determined from [20, p.605]

$$\alpha_o = 1-[(0.005)(\frac{T}{300})^{1.6} + (2.3\times10^{-5})(\frac{T}{300})^{0.8} I_C^{-1/2}]\exp[3.86(\frac{300}{T}-1)] \qquad (18a)$$

At $T = 300^o$ K and $I_C = 1$ ma we find

$$\frac{\partial \alpha_o}{\partial T} = 4.17\times10^{-5} \qquad (18b)$$

Now, using $\beta_o = \alpha_o/(1-\alpha_o)$ we get

$$S_T^{\beta_o} = \frac{\beta_o}{\alpha_o}\, 2\, S_T^{\alpha_o} \qquad (18c)$$

Using a reasonable integrated $\beta_o \approx 50$ and assuming (18b) to still hold gives $S_T^{\beta_o} \approx 0.66$, while doubling β_o approximately doubles this number. Consequently, (17) seems reasonable on experimental and theoretical grounds though the justification for the latter is rather hazy.

Finally then (16e) yield

$$S_T^{g_E} = -(m + 1) \qquad (19a)$$

$$S_T^{g_m} = S_T^{g_E} - \frac{1}{1+\beta_o}\, S_T^{\beta_o} \approx S_T^{g_E} = -(m+1) \qquad (19b)$$

Our conclusion is that the sensitivity behavior of transistors is slightly worse than that of resistors but still roughly the same. Note however that [18, p.742][21, p.16][17, p.70, for $V_g = 1.1$]

$$I_E(T) \approx K_o\, T^{-m+4}\, e^{[V_{EB}(T) - 1.1]q/kT} \qquad (20)$$

where K_o is independent of temperature. If the temperature variation of I_E is not fixed by bias resistors (in which case $V_{EB}(T)$ adjusts) then much larger sensitivities can result for g_E and g_m.

Similar results [22, p.223] can be obtained using the hybrid-pi model [23, p.259] but their derivation is lengthy and avoided here.

We conclude that the equalities of (9) are reasonably well satisfied in normal designs for completely integrated monolithic circuits over normal temperature ranges of operation (0^o C to 100^o C). Since MOS capacitors also have $S_T^C << S_T^G$ we conclude that a reasonable result for the temperature sensitivities of most monolithic or hybrid completely integrated circuits realizing a given voltage or current transfer function H(p) is

$$S_T^H \approx -2.8\, S_p^{H(p)} \qquad (21)$$

where 2.8 is an "average" conductance sensitivity. For an admittance H(p) we add about 2.8 to this. If the construction is completely in terms of MOS devices (transistors, capacitors, and resistors) it appears that $S_T^C \approx S_T^G < 0.02$ and much smaller temperature sensitivities can be obtained with (9) even holding to a higher degree than in the monolithic situation.

IV. DISCUSSION

In the cases where all capacitance and all conductance sensitivities are identical we have rigorously shown that the temperature sensitivity of a transfer function is independent of the circuit configuration used. In particular the result is reasonably valid for completely integrated circuits constructed from monolithic resistors and bipolar transistors using either monolithic or metal oxide capacitors; in these cases customarily $S_T^H \approx -2.8pd \ln H(p)/dp$. The result is of course not exact since rigorously (9) will not exactly hold. But, as the last section has shown, in the temperature range 0^o C to 100^o C it is reasonably accurate, that is, accurate enough such that for first order temperature effects designs can be based upon other than the temperature sensitivity of the configuration. Even though the improvements of one configuration over another will be slight, these are often worthwhile pursuing; the result shows in general how such improvements can be accomplished. Thus, we see that it is the presence of transistors which raises the overall sensitivity over its minimum possible value. Consequently one desires to keep the ratio of number of transistors small or to minimize the effect of the temperature variation of the transistors by some means, such as external resistive feedback. Looked at in this manner we see from (14) that the "smallest" possible sensitivity would be about $S_T^H \approx -2.5pd \ln H(p)/dp$, corresponding to the absence of transistors, at least for monolithic circuits.

We also see that realizations completely in terms of MOS devices seem to have considerable advantages in terms of temperature sensitivity of the transfer functions. In fact the result shows the nature of the overall improvement in going from monolithic to MOS devices. Thus, experimental results seem to indicate variations of 1000 to 5000 ppm/^{o}C for monolithic silicon components and of 50 to 100 ppm/^{o}C for MOS components. The above formulation then shows that an improvement by a multiplicative factor near 30 for the temperature sensitivity of the transfer function can result by changing the material while a factor of under 2 results by changing the circuit.

An example to illustrate further the nature of the result, we comment that a complete integration of a gyrator synthesis [4] will yield, to a high degree of accuracy, identical temperature sensitivity results as will be obtained for a complete integration using the same material via a state-variable synthesis [2] of a given transfer function. Consequently, comparison of various circuit configurations might best be made, at least in the first instance of design, in terms of other quantities, such as sensitivities to gain variations through mask misalignment, etc., in place of temperature sensitivity.

It should be pointed out that it is sensitivity, a normalized quantity, which has been treated and not absolute variations. Because, for example, one configuration might operate at a higher temperature than another one, the absolute temperature variations might differ and are consequently well worth investigation in individual cases. Also local variations in temperature due, for example, to high resistivities or high packing densities can cause one layout to be superior in temperature behavior over another. Likewise we should reiterate that only transfer functions have been treated here. The result does not hold for sensitivity with respect to temperature of the quality factor, Q, or undamped natural frequency, ω_n; in fact it appears that a change in circuit configuration can significantly change these latter two sensitivities (but more research is needed to solidify results). We mention too that the result is limited to linear input-output relationships. The presence of non-linearities and particularly independent sources, as for example from photodiodes, greatly alters the result.

At reasonable temperatures and for reasonable configurations the result is valid. However, for temperature environments greater than 150^o C, for example, the approximations of (9) appear to further break down, in which case there is a need for a theory of high temperature minimum temperature sensitivity designs. Further, by force of design specifications or by desire to deliberately violate (9) one can apparently meet situations where the difference between $S_T^{g_m}$ of (19) and S_T^G of (9) is critical, in which case further investigation seems needed, as it is for $S_T^{\beta_o}$ anyway.

Here we have assumed that in each portion of a chip there is located a component which for temperature behavior can adequately be modeled by its Ebers-Moll equivalent. Such an assumption seems in many ways inappropriate though about all one can presently do to obtain quantitative results. Still the approach presented seems more accurate than the previous one [22, p.223] where the hybrid-pi model was used since the temperature behavior rests upon absolute variations for which bias quantities can not be ignored. In any event we see that a more accurate method seems needed. One such method of attack would be to consider a chip as a blend of material which continuously varies from point to point (though in some portions this variation may be rather sharp). Taking this viewpoint and working with differential volume elements which can be described in terms of conductance and capacitance seems to give a more accurate demonstration of the validity of (9).

Of course it is well recognized that external feedback can be used to decrease sensitivity—the presented result does not change the situation. Thus, if external components having differ-

ent temperature characteristics are employed considerable sensitivity change can occur by a change in circuit configuration; a study of such configurations is then of profit. To reiterate, the result is for a completely integrated structure constructed of somewhat homogeneous material.

"A favorable outcome of even very extensive and exacting tests cannot provide conclusive proof for a hypothesis, but only more or less strong evidential support or confirmation" [1, p.33].

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