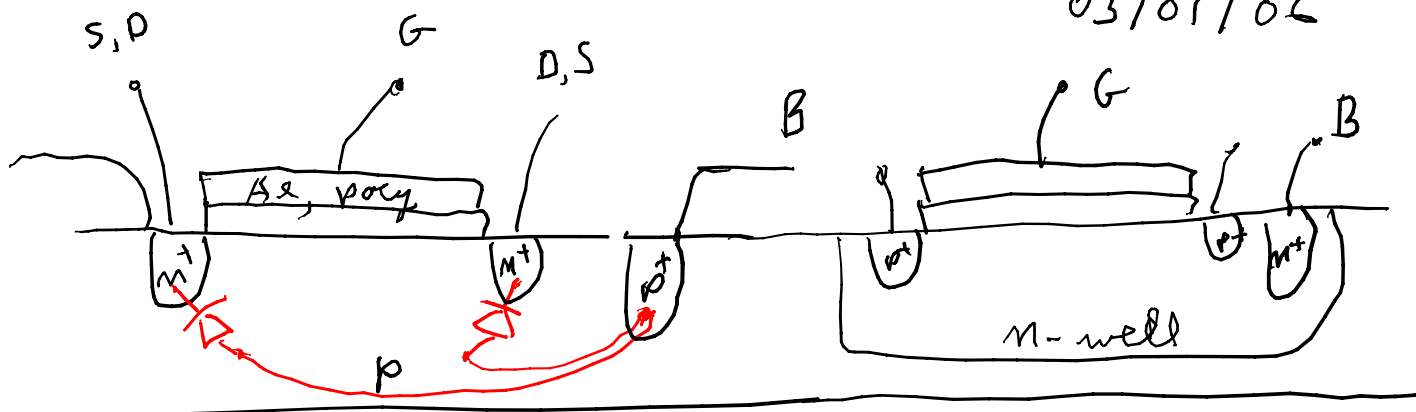


EEH17
03/01/06



NMOS

PMOS

To back bias the bulk diode, for NMOS tie B to lowest potential (pin 7 of 4007)

for PMOS tie B to highest potential (pin 14 of 4007)

$$i_D = f(v_{GS}, v_{DS})$$

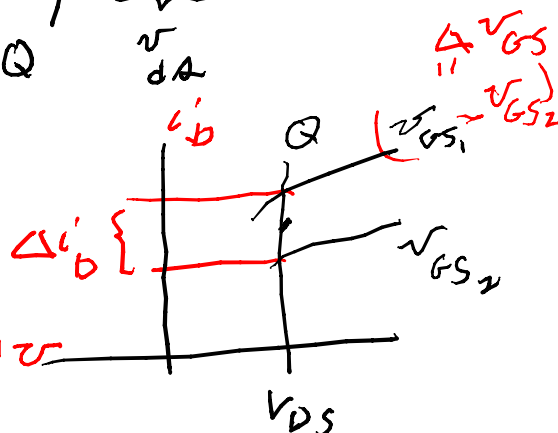
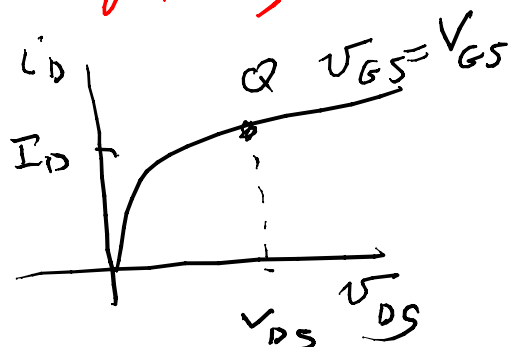
Taylor series

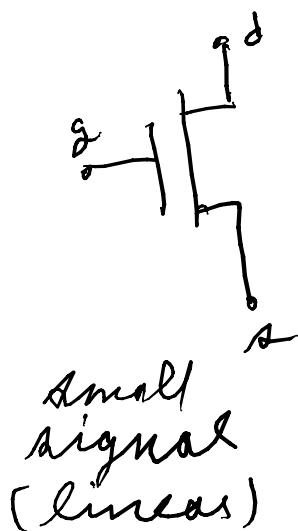
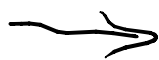
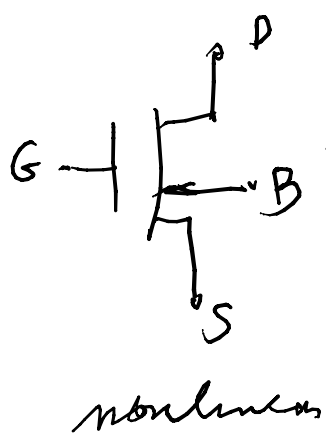
$$i_D = I_D + \left. \frac{\partial i_D}{\partial v_{GS}} \right|_Q (v_{GS} - V_{GS}) + \left. \frac{\partial i_D}{\partial v_{DS}} \right|_Q (v_{DS} - V_{DS}) + \dots$$

Q v_{gs} Q v_{ds}

$$i_d = i_D - I_D = g_m v_{gs} + g_o v_{ds}$$

$$g_m = \left. \frac{\Delta i_D}{\Delta v_{GS}} \right|_Q \approx \frac{2.2 \times 10^{-3}}{2} = 1.1 \text{ mS}$$





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