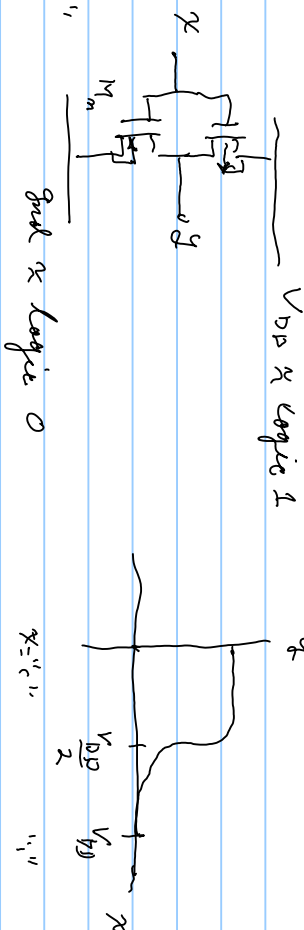
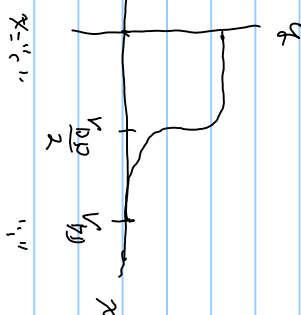


P. 1093 logic gates CMOS

inverters



But x logic 0



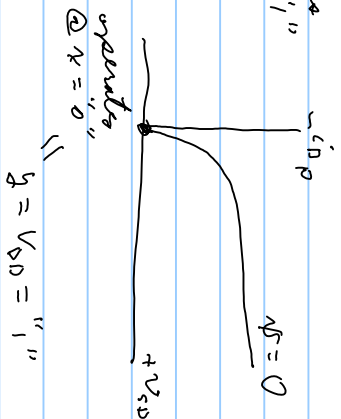
$x = 0$ "1"



$\Rightarrow$ if $x = 1$ force the $V_{DS} = 0 = y = 0$ pull output down

$\Rightarrow M_n =$ a pull down Transistor

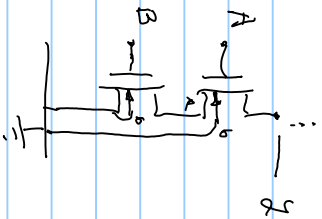
operates if $x = 1$



operates @ $x = 0$

$y = V_{DD} = 1$

$\Rightarrow$ if $x = 0 \Rightarrow y = 1 \Rightarrow M_p =$ a pull up transistor

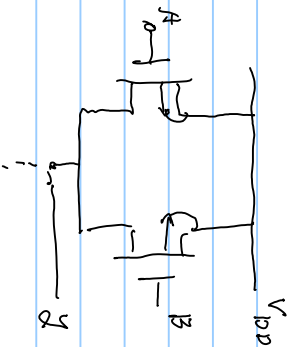


two pull down transistors

$$y = \overline{A \cdot B}$$

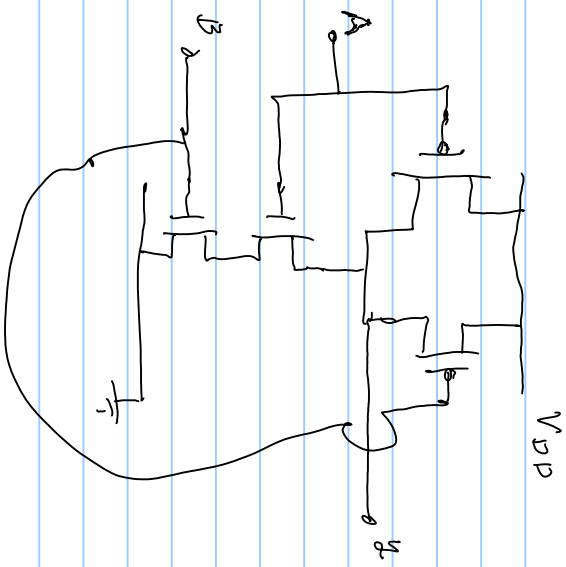
= not and

+ = logic or
 • = logic and
 upper bar = logic complement

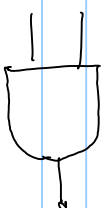


$$y = \overline{A + B} \Rightarrow A, B = \overline{y} \Rightarrow \text{non connect to above}$$

nand = buffer stroke



→ gives the NAND



Logic table

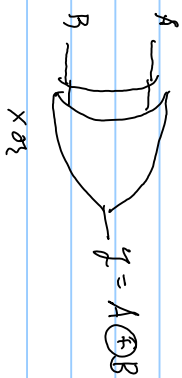
A	B	Y
1	1	0
1	0	1
0	1	1
0	0	1

Logic OR

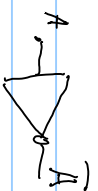
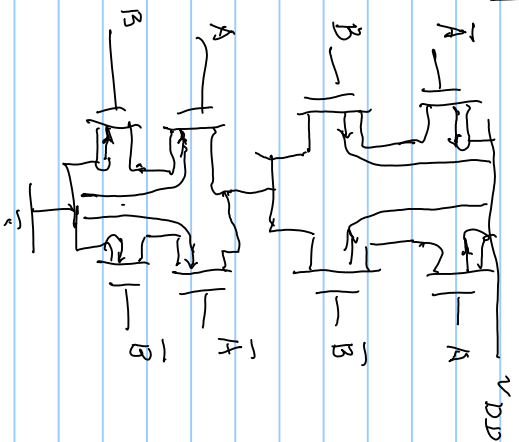
A	B	y
1	1	1
1	0	1
0	1	1
0	0	0

A	B	y
1	1	0
1	0	1
0	1	1
0	0	0

2nd case in mod 2



P.1078



Effect of the bulk, p. 288

$$V_{th} = V_{TO} + \gamma \left(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f} \right) = V_{TO} \text{ if } V_{SB} = 0$$

(tie source to bulk)

can use V_{SB} for small signals but not $V_{SB} < -2\phi_f$
important to be sure bulk diodes don't get too far forward biased

another way to make logic is with pass transistors (CMOS variants) p. 1193