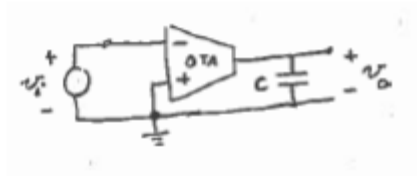


HW5

1. (60 points; OTA integrator design)

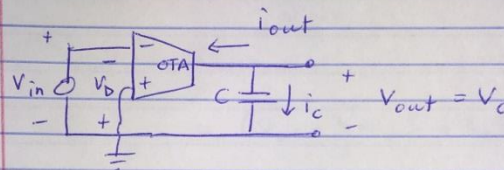


a) For the above connection give the nonlinear differential equation for the voltage output versus the voltage input using an MOS OTA.

② Part A Differential Equation

You do not need to solve it!

Just find an expression where V_{in} and V_{out} are the only variables.



Note the direction of i_{out} !

The MOS OTA is just the MOS differential pair given in lecture on 10/01/15.

i_{out} is a function of V_D

See the lecture notes for a full derivation of $i_o(V_D)$

$$\text{Let } A = \sqrt{2I_T/k_n}$$

I_T = tail current

k_n = property of the NMOS used in the MOS OTA circuit.

$$i_o = 2I_T \left[\frac{V_D}{A} \sqrt{1 - (V_D/A)^2} \right]$$

$$V_i = -V_D, \text{ and } i_c = -i_{out}$$

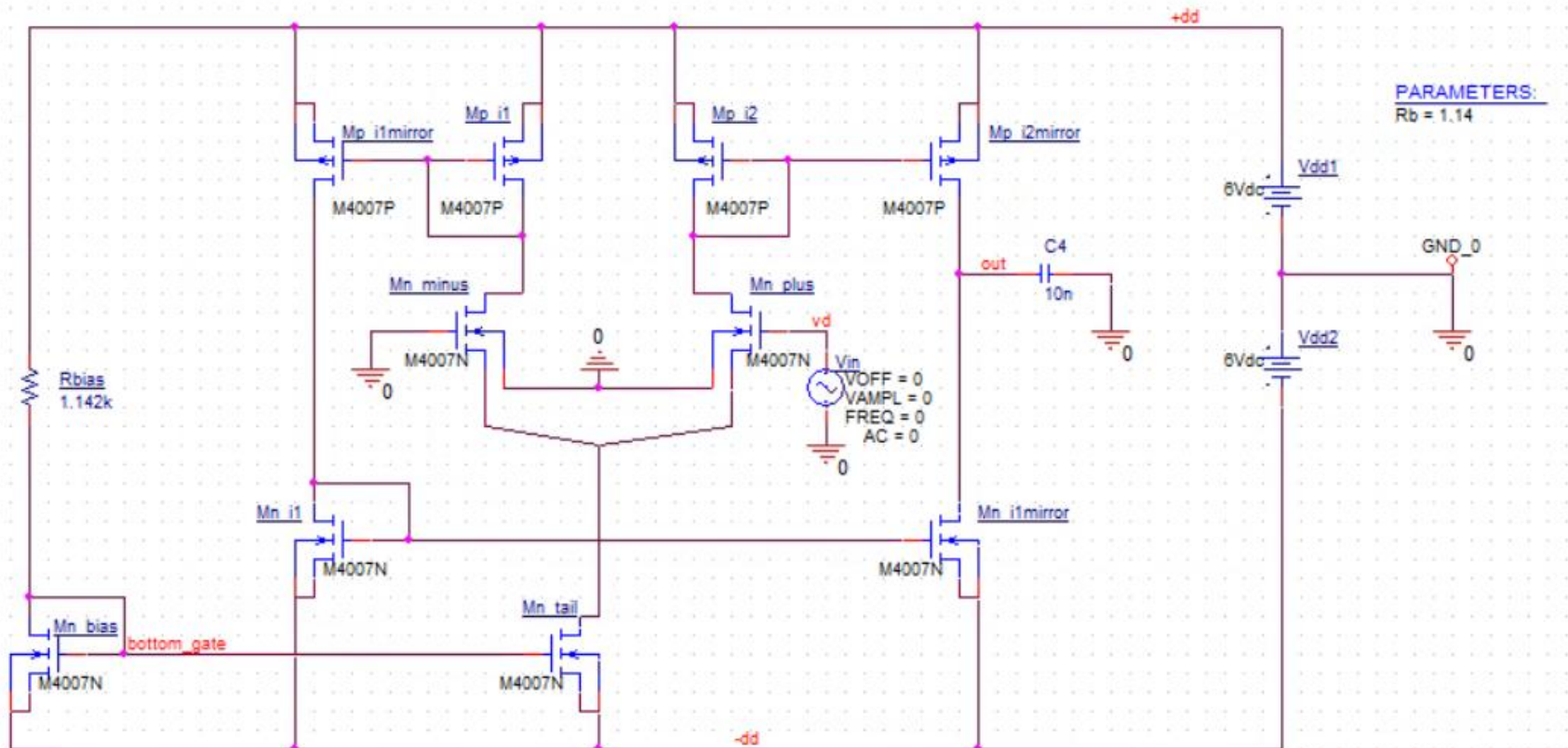
$$i_c = 2I_T \left[\frac{V_i}{A} \sqrt{1 - (V_i/A)^2} \right]$$

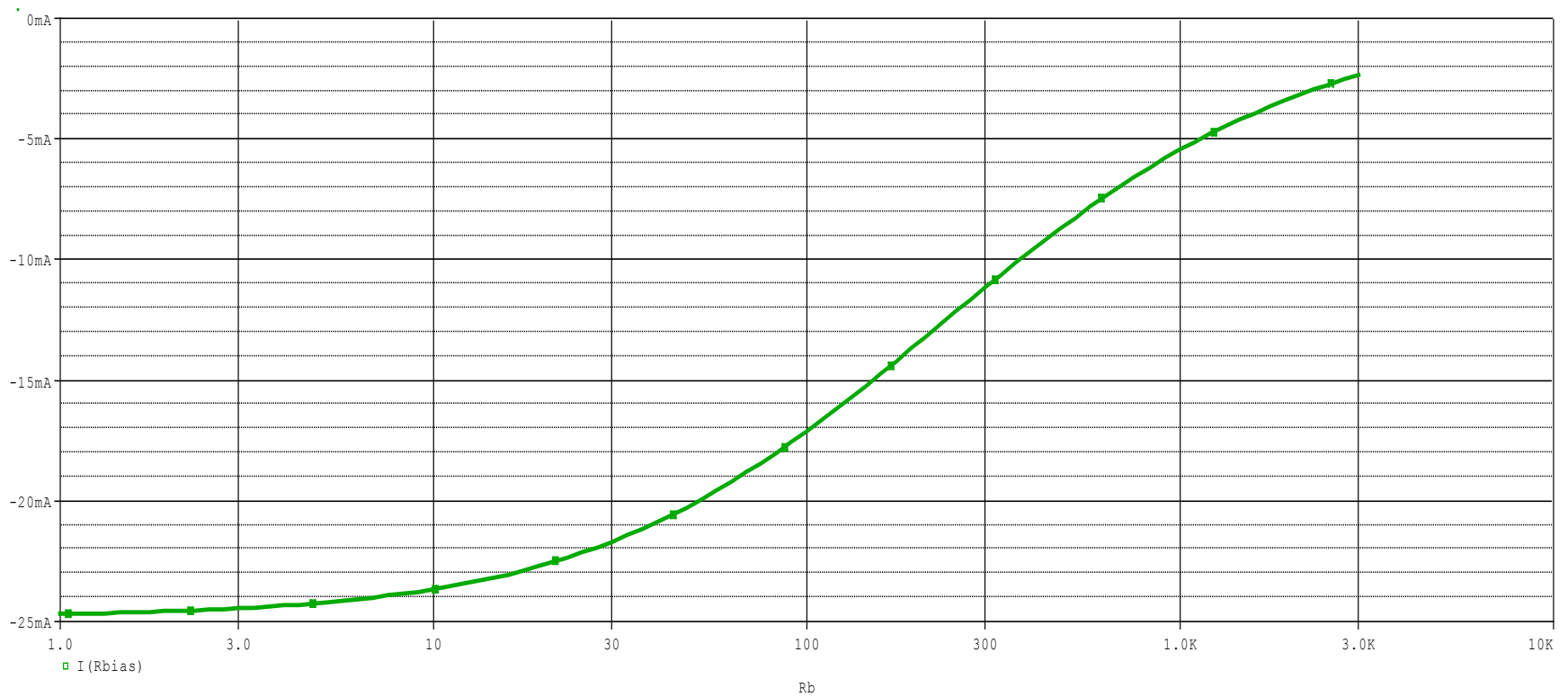
$$i_c = C \frac{dV_c}{dt} \rightarrow V_c - V_{c, \text{initial}} = \frac{1}{C} \int_0^t i_c dt$$

$$V_c(t) = V_{out}(t) = \frac{1}{C} \int_0^t 2I_T \left[\frac{V_i}{A} \sqrt{1 - (V_i/A)^2} \right] dt + V_{c, \text{initial}}$$

initial charge on capacitor

Design an OTAC circuit to give this differential equation using a MOS OTA made of 4007 transistors (with one tail current setting resistor). Use two 6V power supply batteries, set the tail current at 5mA, and use a 10nFd capacitor.





I ran a sweep for $\{R_b\}$, the value of the bias resistor. The sweep intersects 5mA (the desired current) at about 1.142 k Ω .

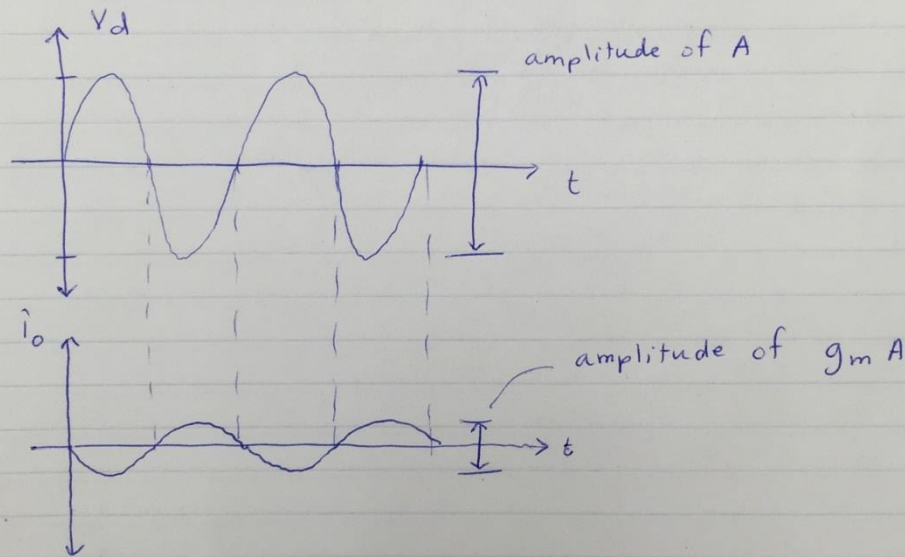
b) Sketch (by hand) the low frequency output current versus input differential voltage that you expect for this integrator with small signal sine wave inputs.

Low-frequency means that capacitive behavior inside the OTA will not be significant.

Small-signal means: $\hat{i}_o \approx g_m V_d$

~~I've labeled my output such that it should have the opposite sign of V_d (g_m is negative).~~

I've labeled my output current such that it is going into the OTA, so i_o will be negative when V_d is positive.

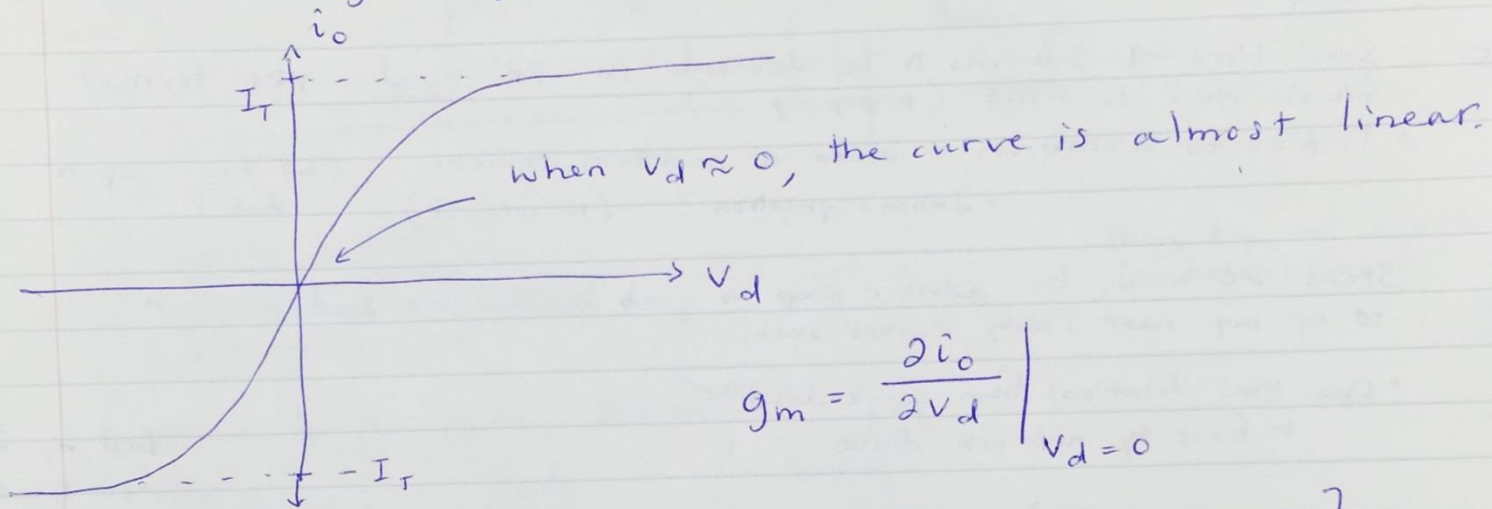


V_o on the other hand would be the integration of i_o ~~V_d~~ . So if V_d is a sine wave, i_o is a negative sine wave, V_o is a ~~positive~~ cosine wave.

Correction: v_o would be a negative cosine wave, because it is the integration of i_c , and $i_c = -i_o$

Determine the small signal gm and run Spice to check the integrator operation.

Small-signal gm:



$$g_m = \left. \frac{2i_o}{2V_d} \right|_{V_d=0}$$

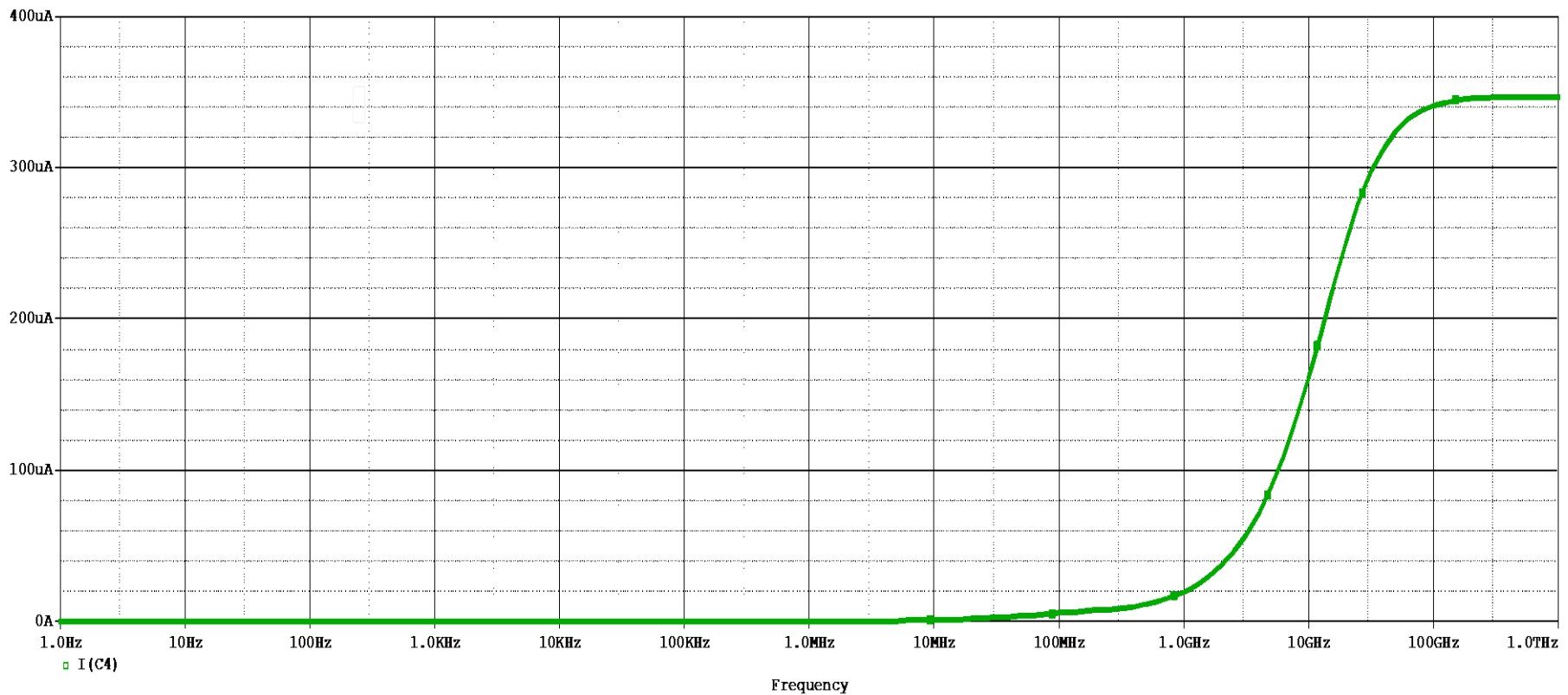
$$i_o = 2I_T \left[\frac{V_d}{A} \sqrt{1 - (V_d/A)^2} \right]$$

$$\text{where } A = \sqrt{2I_T/k_n}$$

$$g_m \approx \left. \frac{i_o}{V_d} \right|_{V_d=0} \quad \text{because the curve is approximately linear at that region.}$$

$$g_m = \frac{2I_T \left[\frac{V_d}{A} \sqrt{1 - (V_d/A)^2} \right]}{V_d}$$

Do a frequency response to determine over what frequency range it will work.



Frequency plot of the current amplitude through the output capacitor. No significant current goes through the transistor until around 1GHz, this seems really high...

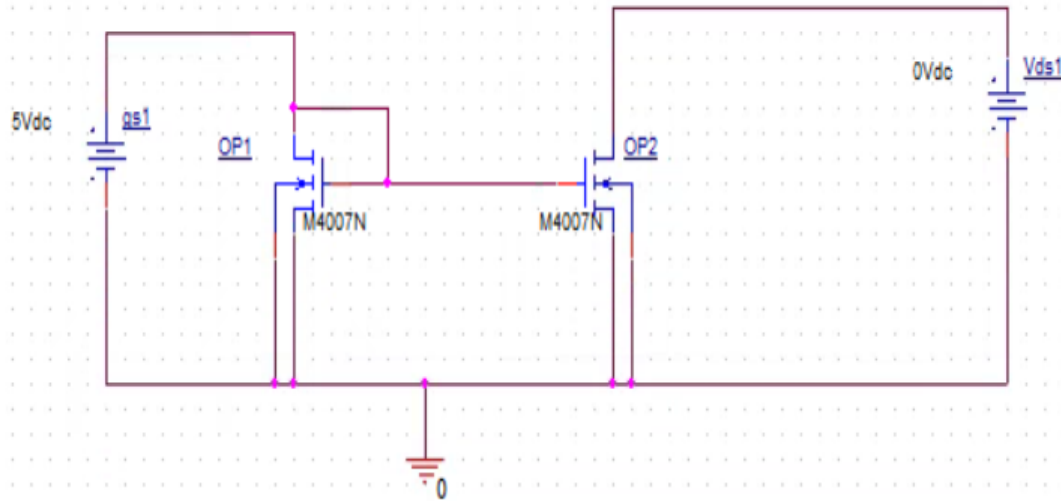
2. (40 points; current sources, mirrors)

a) Compare NMOS current sources made with one input/output pair of transistors versus a circuit using a cascode of two input/output pairs.

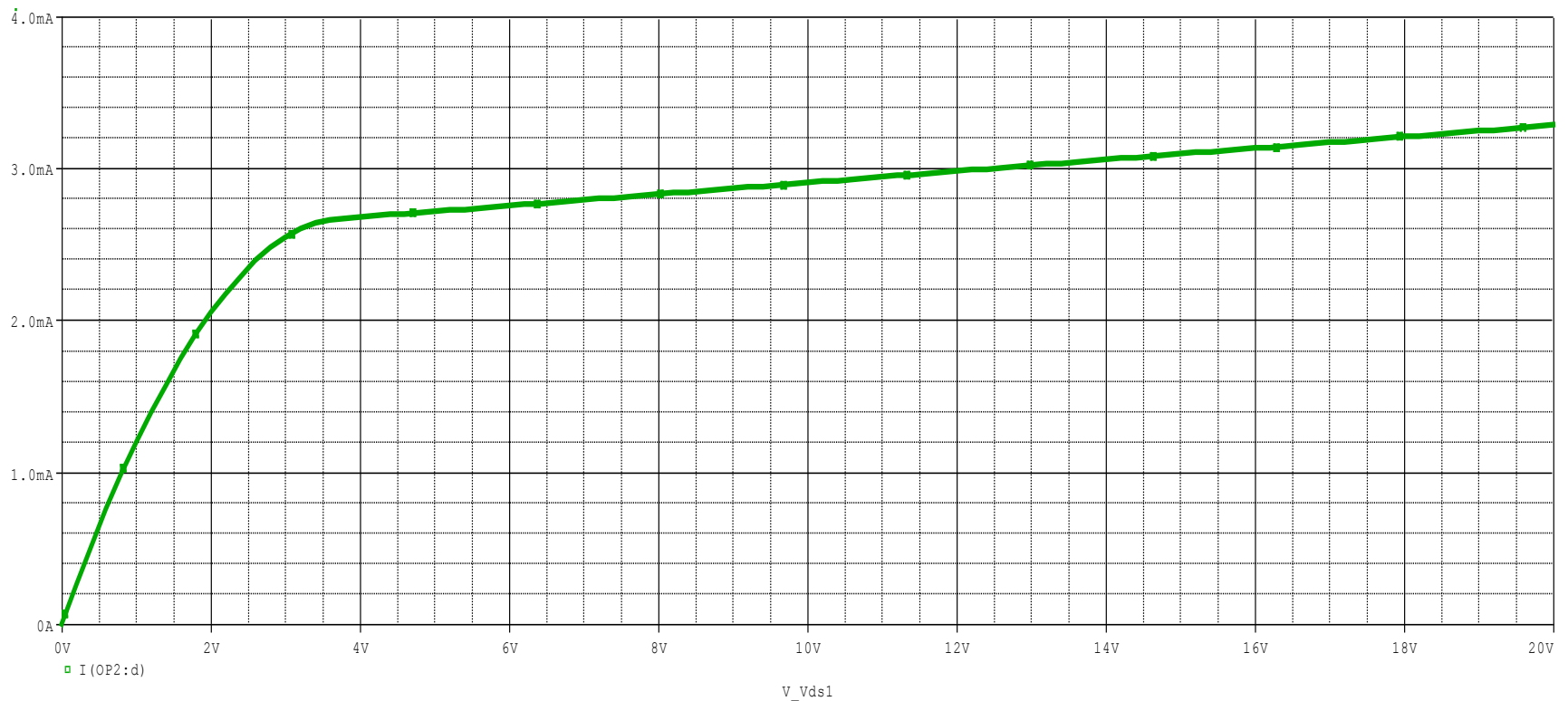
One-pair:

Voltage sweep on {Vds1}.

Measure the current into the
drain of OP2.

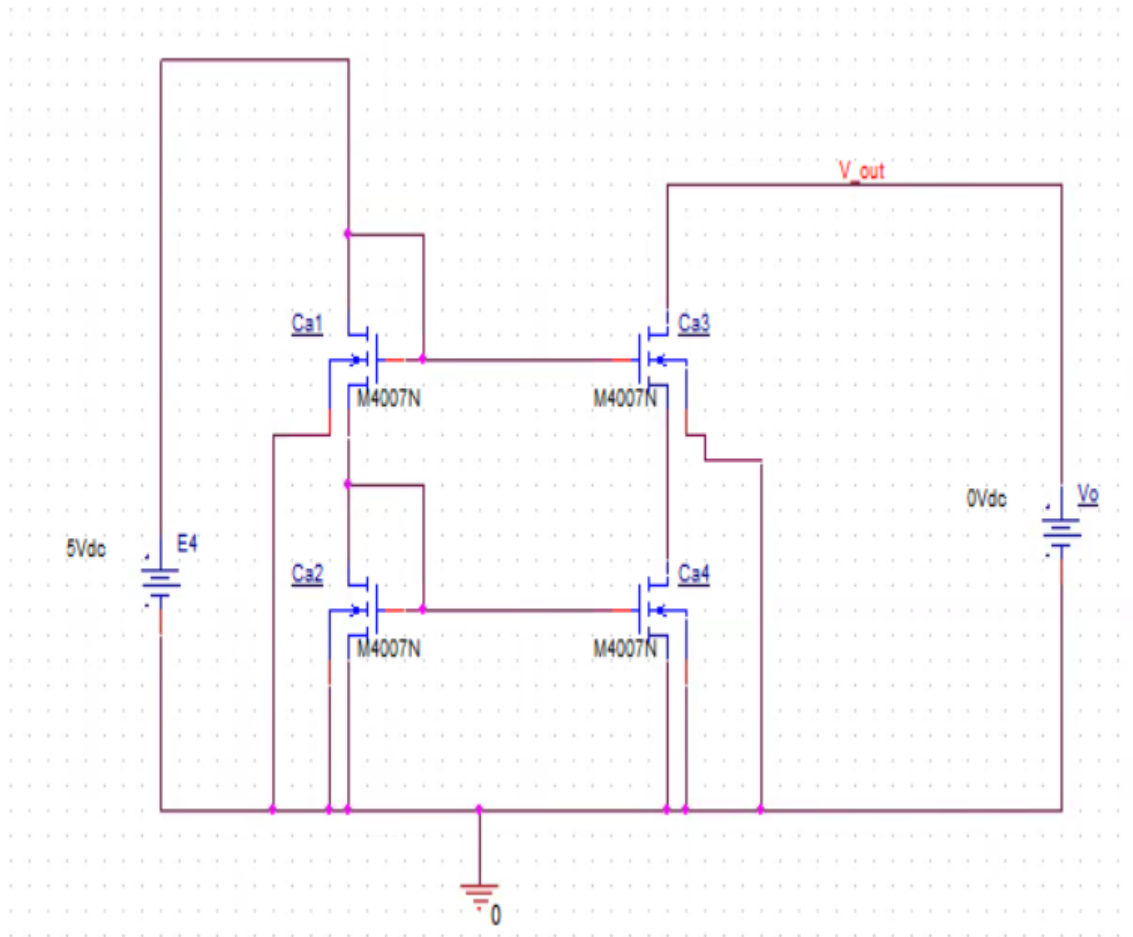


One-pair plot of V_{DS} across the mirror NMOS, vs the current through its drain.
The saturation region still has a rising slope, which is undesirable.

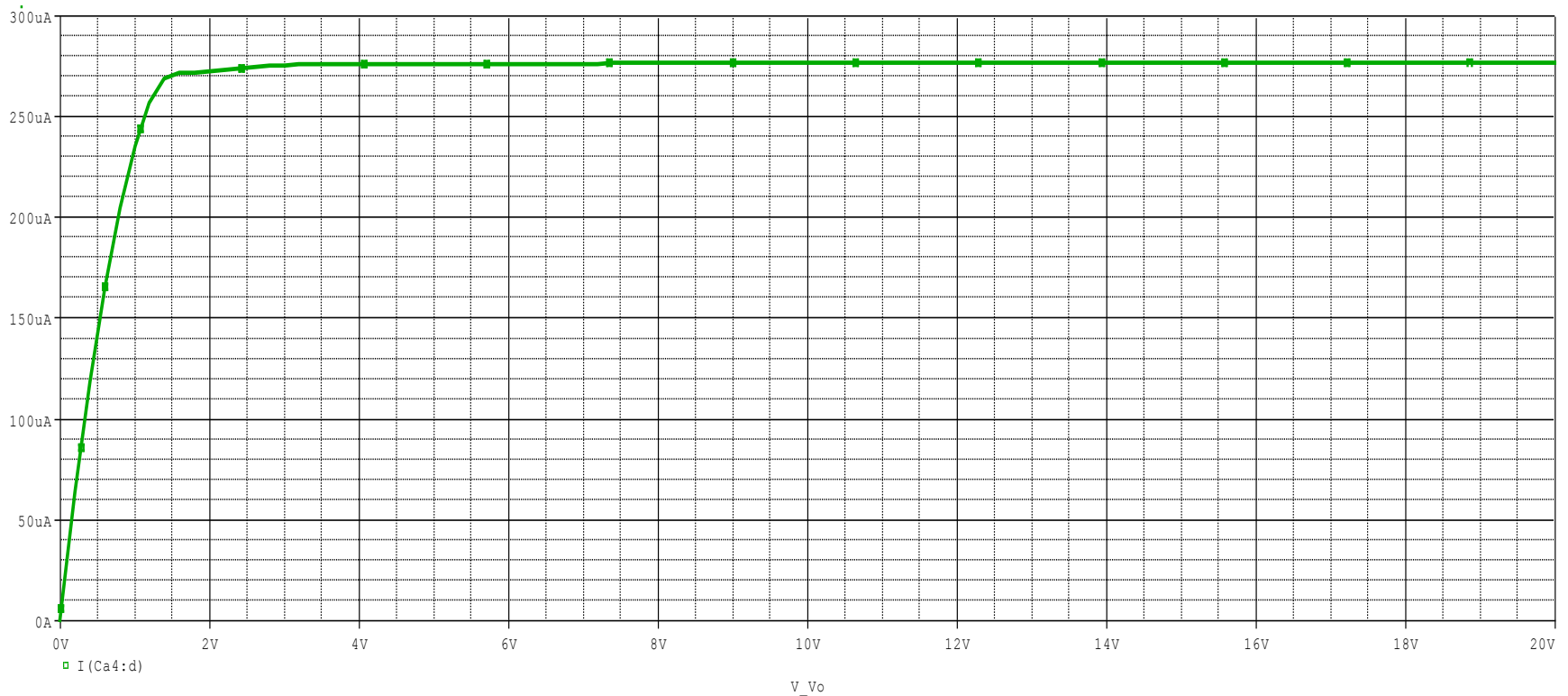


Two-pair (cascode):

Voltage sweep on $\{V_o\}$,
measure current
through the transistors
(same through both)
on the mirrored side).

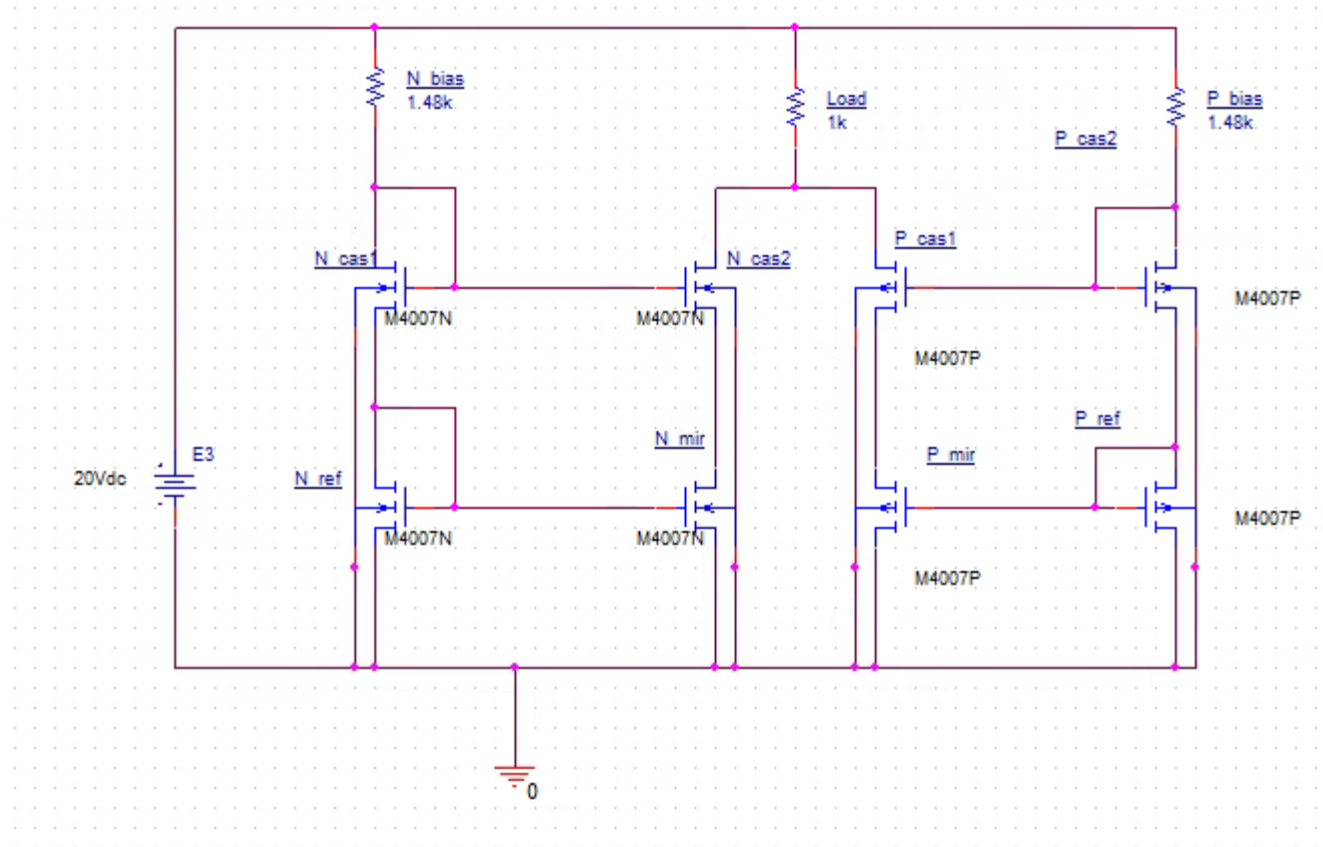


Two-pair cascode plot of V_{out} across the both mirror transistors, vs the current through those mirror transistors. The saturation is now flat with a constant current, but that current is much lower than the one-pair.



b) Design a 4 transistor CMOS bidirectional current mirror (that is, one which will work with input currents of any sign). Note that this will require a bias offset current. Check your design in Spice.

For the bidirectional mirror, I could not figure out how to get the proper behavior in pspice with just 4 transistors. I used an NMOS cascode sink and a PMOS cascode source in parallel, both of which connect to the load resistor (in the middle).



I did a bias-point simulation with a positive 20V source, which should have let current run through the NMOS cascode, but not through the PMOS cascode. But the bulk terminal on P_cas1 was drawing -18.34mA. I don't know why this happened.

