

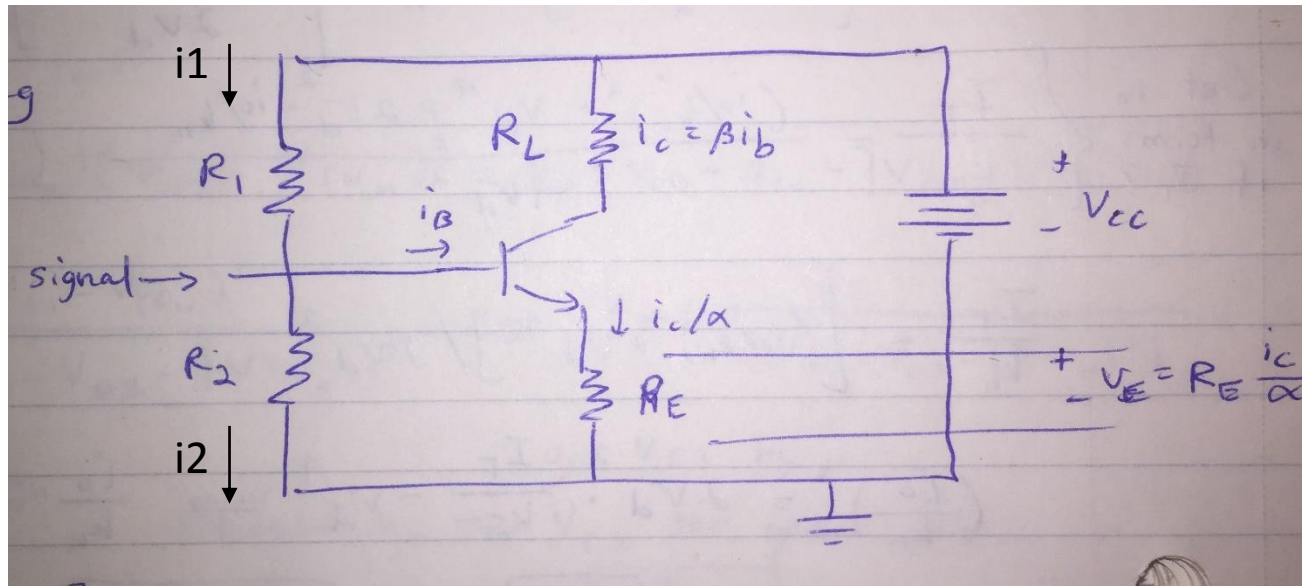
HW 4

For the following problems assume a 9Volt battery available.

1. (50 points, BJT CE design)

a) Design a common emitter amplifier using a 2N3904 transistor for a voltage gain of $A_v = -10$ with the collector current near 10mA.

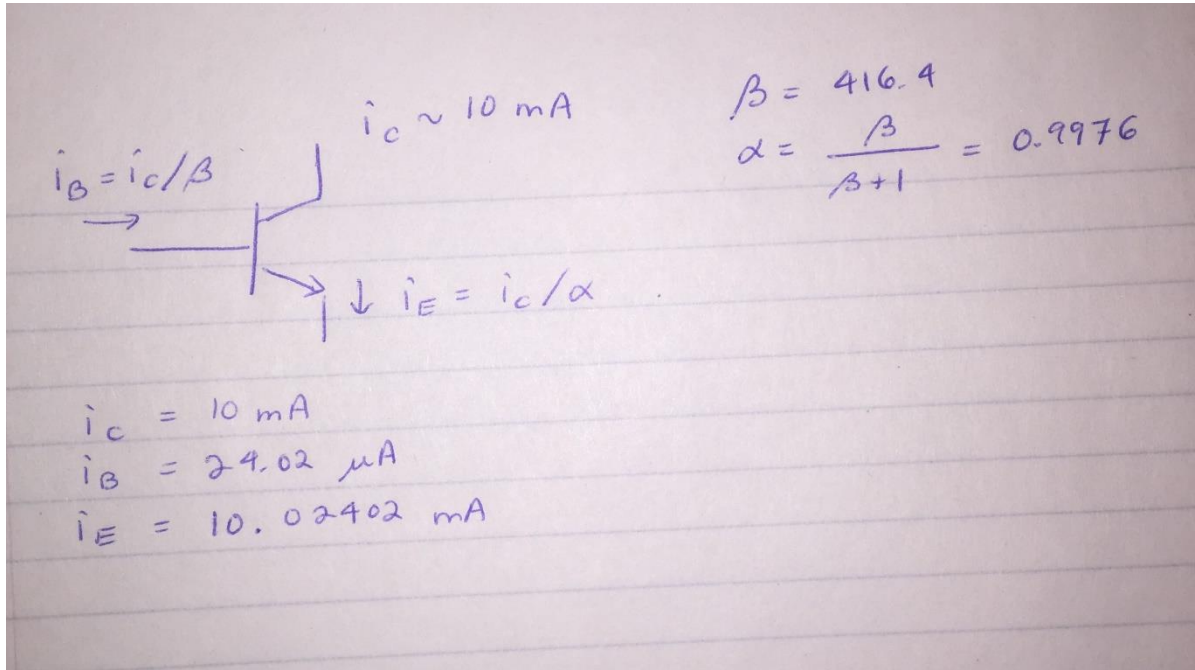
First, we must bias the transistor appropriately, with the two desired values we are given. This means we decide on the resistor values and battery voltage for the following diagram:



Well we know that the battery V_{CC} must be 9V, so that is taken care of.

To decide on the resistors, let's find each desired current at the transistor terminals, because we know that $I_C \sim 10 \text{ mA}$ (See next slide)

From the Pspice model for the 2N3904, we get that $\beta = 416.4$, and $\alpha = \frac{\beta}{(\beta+1)} = 0.9976$



The desired gain A_v is $-10 = v_o/v_{in}$. It is negative because the voltage potential increases across the signal component v_{in} , and decreases across the load component v_o .

We know this about the performance of the BJT:

$$g_m \approx \frac{I_C}{V_T} = \frac{10 \text{ mA}}{26 \text{ mV}} = 0.385 \text{ S}$$
$$g_m = \frac{\partial i_C}{\partial v_{BE}}$$

$\partial v_{BE} = \partial v_{in}$ when the battery voltage doesn't change.

The voltage across the load: $v_{load} = v_o = -i_C R_{load}$, $i_C = \frac{-v_o}{R_{load}} \rightarrow \partial i_C = -\partial v_o / R_{load}$

Using the last equation in the line above, we get:

$$g_m = \frac{-\partial v_o}{\partial v_{in}} \cdot \frac{1}{R_{load}} = 0.385 \text{ S}$$

We want to select the value of R_{load} to get $v_o/v_{in} = -10$.

$$R_{load} = -\frac{10}{0.385} \approx 26 \Omega$$

From KCL between the R1 and R2, we get:

$$I_1 = I_B + I_2$$

And the voltage across R2: $V_{R2} = V_{BE} + V_E$

Let's set $V_E = 1V$ (This is what was done in lecture)

And we can approximate $V_{BE} = 0.65 V$ (This is its typical value)

So $V_{R2} = 1.65 V$

Let's say R2 is 500 k Ω , then $I_2 = \frac{1.65}{500 \text{ k}\Omega} = 3.30 \mu A$

Whatever you pick for R2, make sure at the end that the voltage at the base is less than the voltage at the collector! ($V_{CB} \geq 0$)

Then $I_1 = 3.30 \mu A + 24.02 \mu A = 27.32 \mu A$

$$V_{R1} = V_{CC} - V_{R2} = 9V - 1.65 V = 7.35 V$$

$$R_1 = \frac{V_{R1}}{I_1} = \frac{7.35}{27.32 \cdot 10^{-6}} \approx 269.0 \text{ k}\Omega$$

$$\text{Finally, } R_E = \frac{1 V}{10.024 \cdot 10^{-3} A} \approx 99.8 \Omega$$

All together:

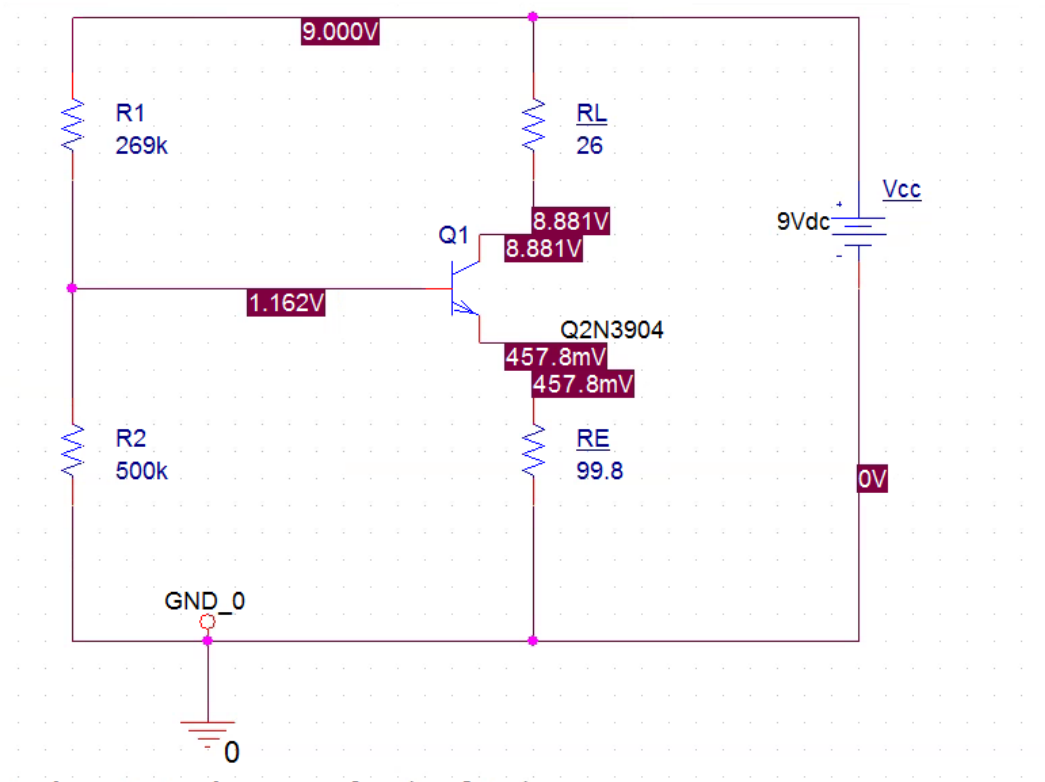
R1 = 269k

R2 = 500k

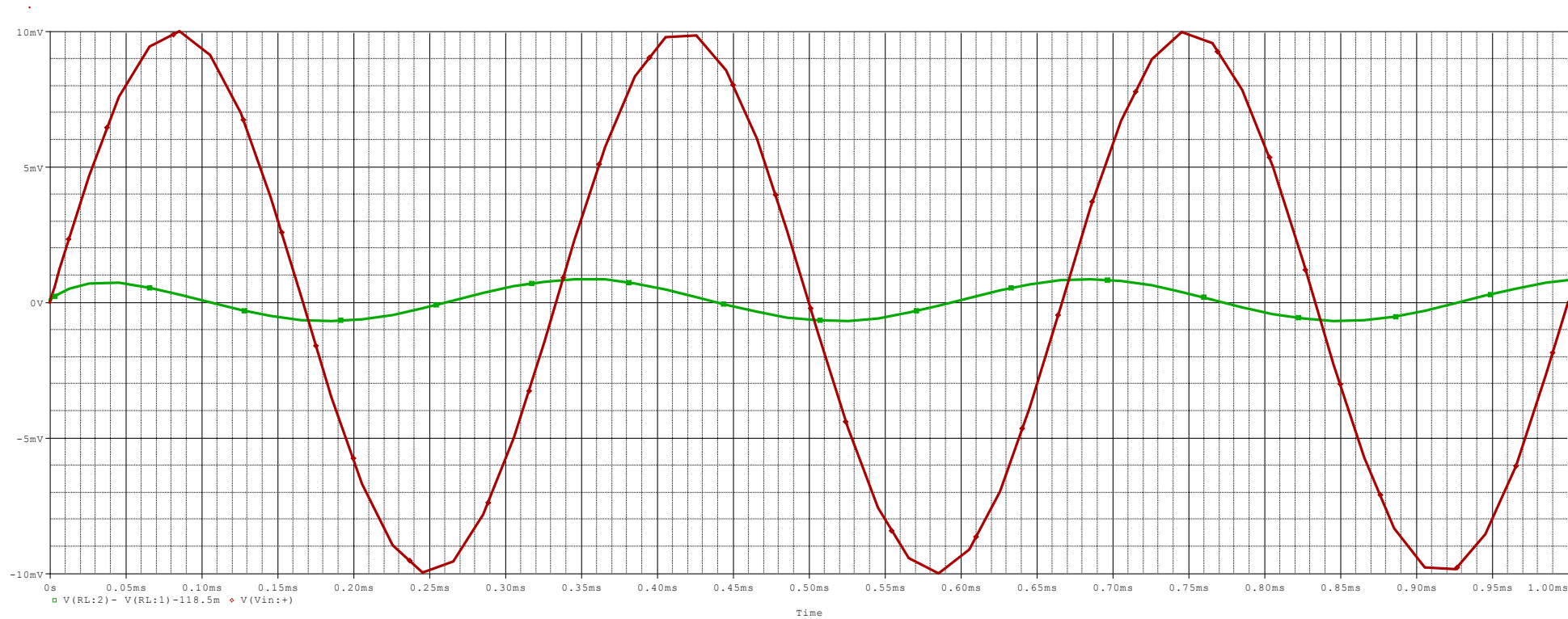
Rload = 26

$R_E = 99.8$

b) Check your design by running Spice with sinusoidal input signals at a frequency near 3KHerz. .

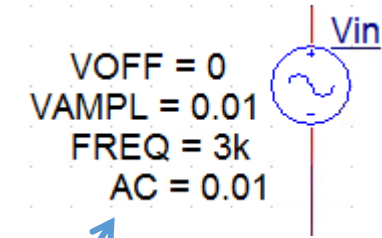
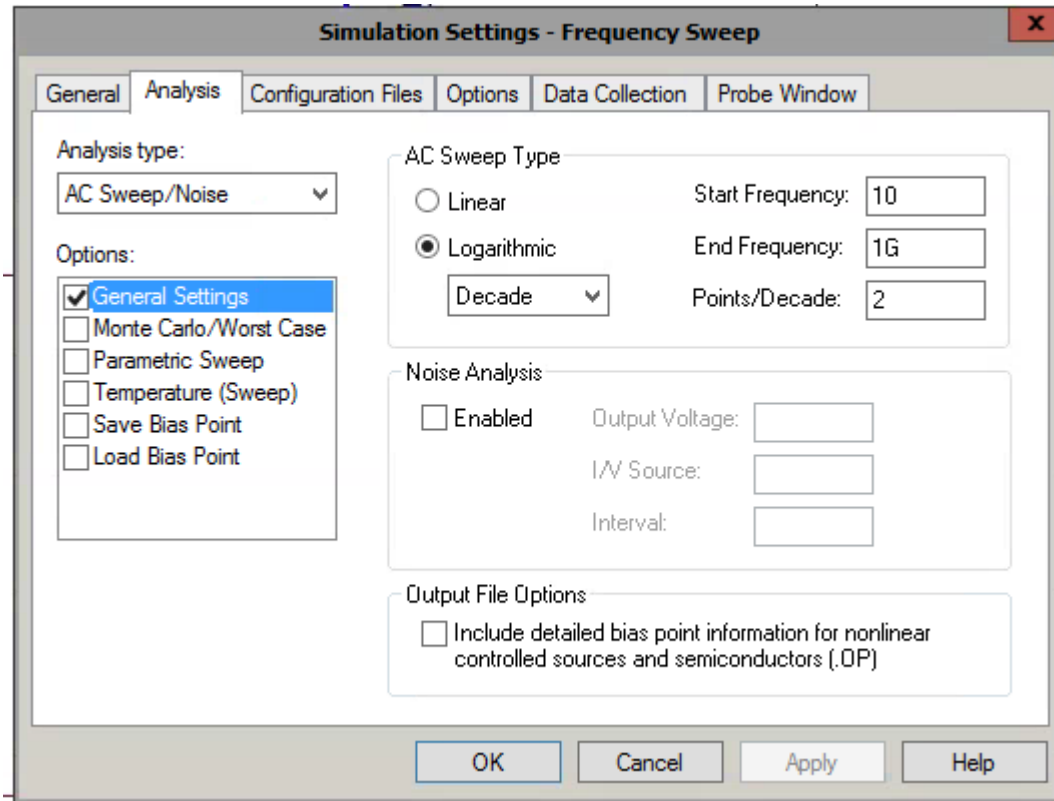


Here is my DC bias. It is not exactly the same as the theoretical, but that's ok. Notice that the DC bias of the load is about 0.119 V.

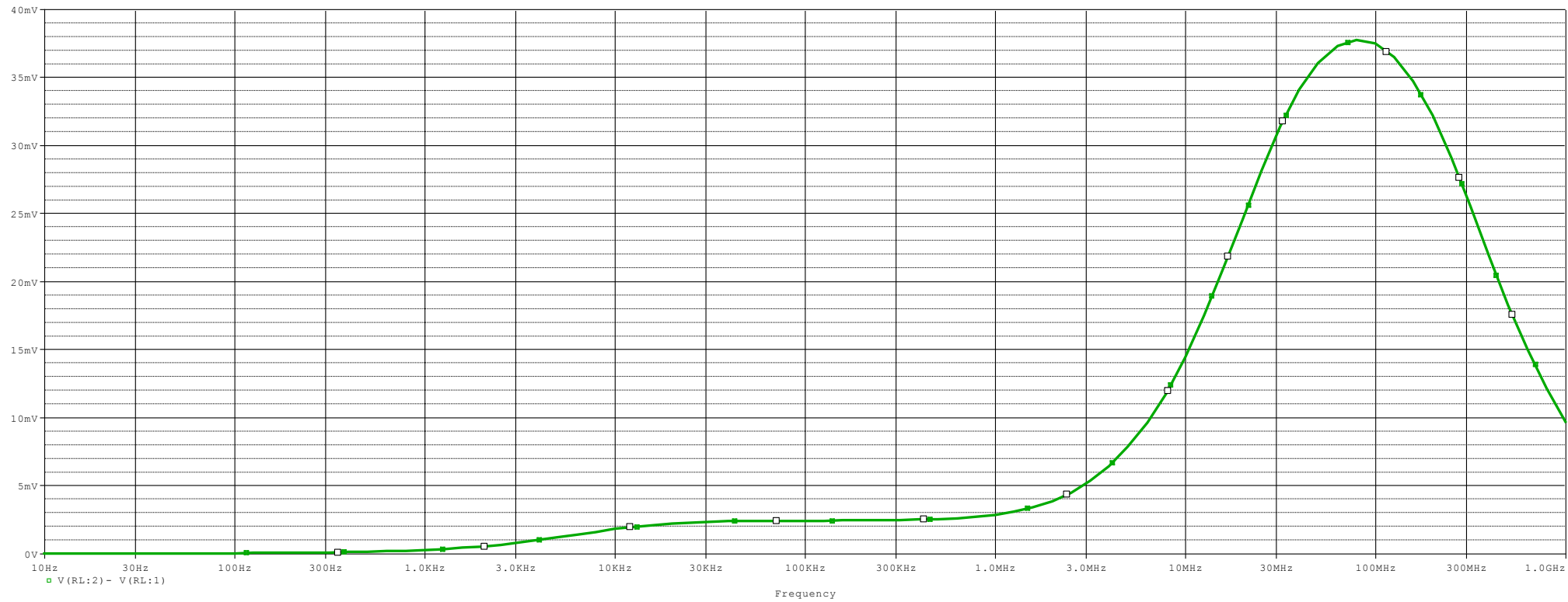


Clearly not the desired gain... green is V_{out} and red is V_{in} . But the gain depends on the frequency, so let's move on to the next step.

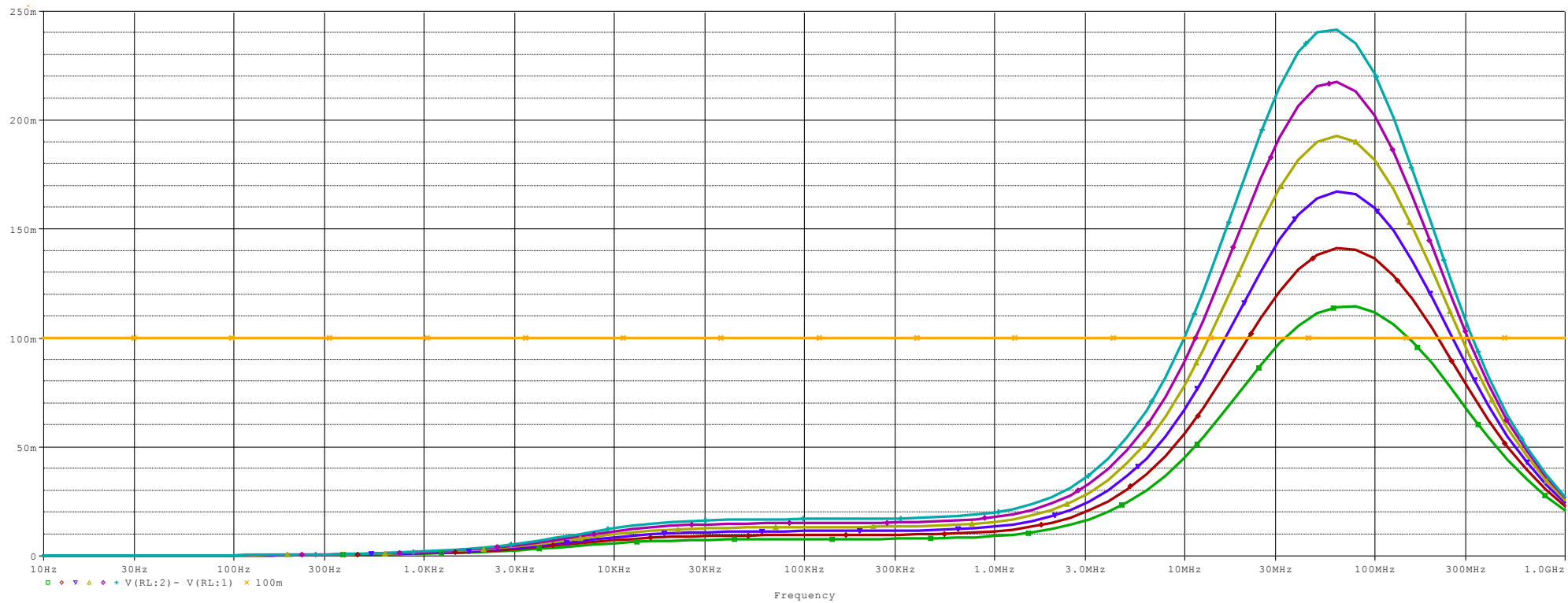
c) Do a frequency response from 10Hz to 1GHerz and comment on the results.



“AC” is the voltage amplitude that will apply for this sweep



This plots the amplitude of the voltage across the load. We can't get the gain we want... the max is about $37/10 = 3.7$. So let's do a parametric sweep of Rload and pick a new value.



The horizontal line shows the V_{out} we need to get gain = 10 ($V_{out} = 100$ mV). The minimum resistance I chose here is 80 ohms, so this means you could use any load resistance above 80, and you will get the desired gain somewhere between 10MHz and 300MHz.

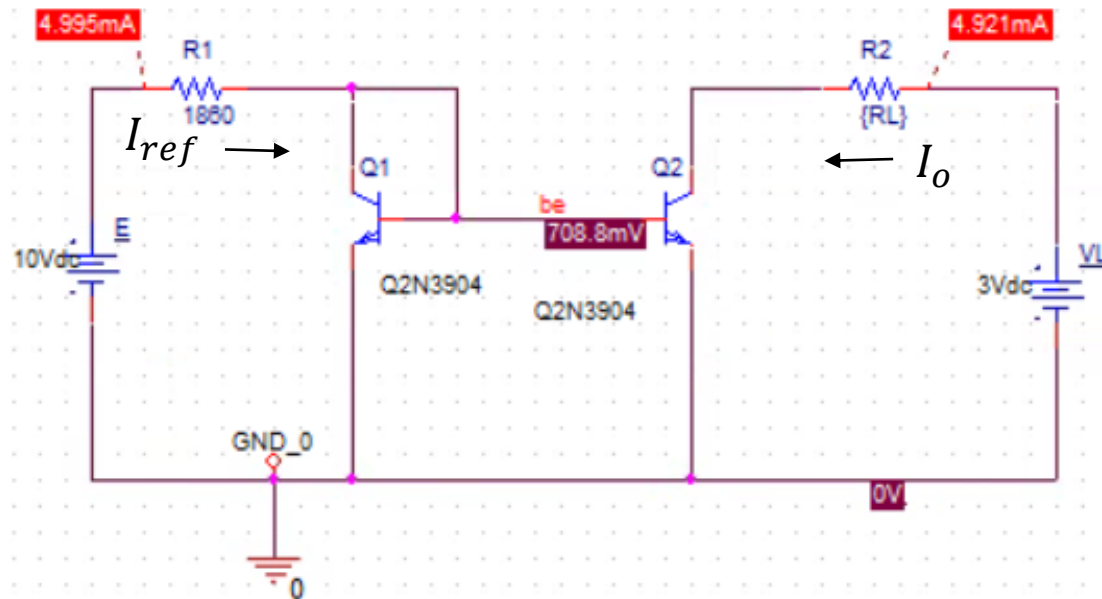
2. (50 points, current mirrors)

For transistors use 2N3904, 2N3906, and 4007-CMOS

- a. Using resistors and transistors design four current mirrors to mirror 5mA, two for sinking and two for sourcing, one of each of these two using BJTs and one each of them using MOS.

Note that your designs may vary a bit, but here are the schematics that I drew:

Current-sinking BJT: Uses NPN transistors



$$E - V_{R1} - V_{be} = 0$$

Let's say $E = 10V$, and $V_{be} \approx 0.7$

$$10 \approx i_{R1} R_1 + 0.7$$

Want $i_{R1} = 5mA$

$$R_1 = \frac{9.3V}{5 \cdot 10^{-3}A} = 1860\Omega$$

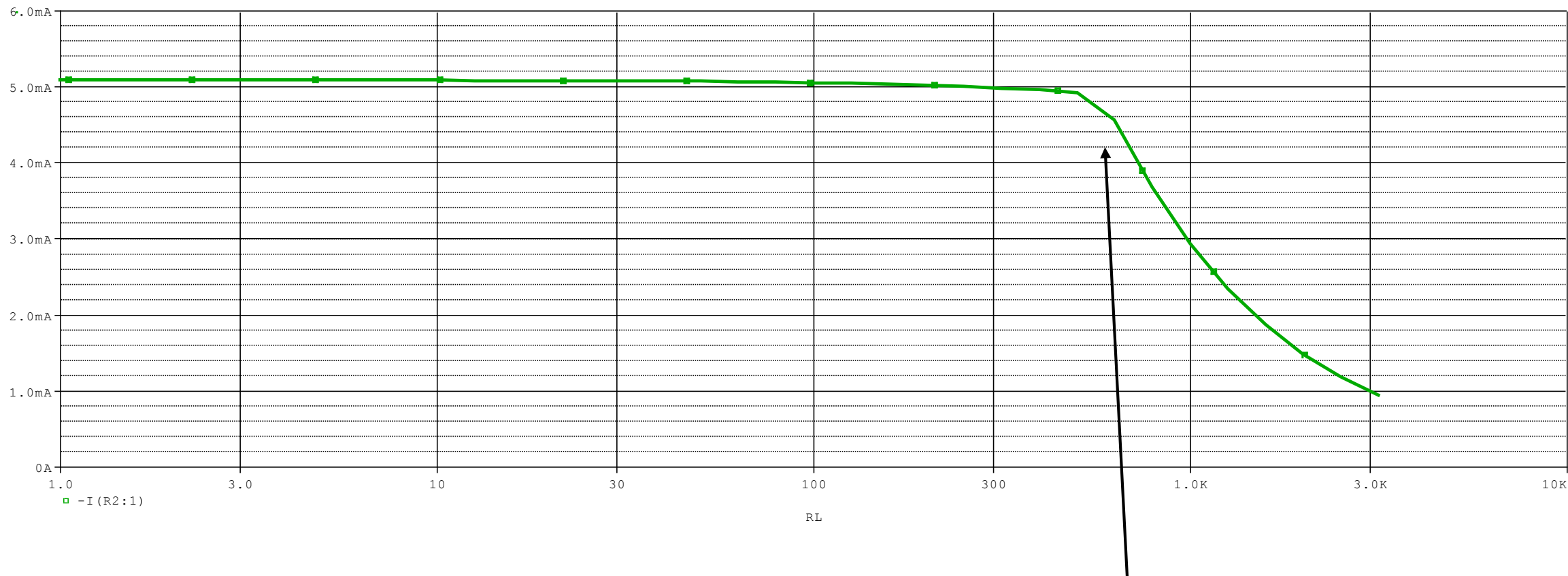
PARAMETERS:

RL = 500

R3 = 100

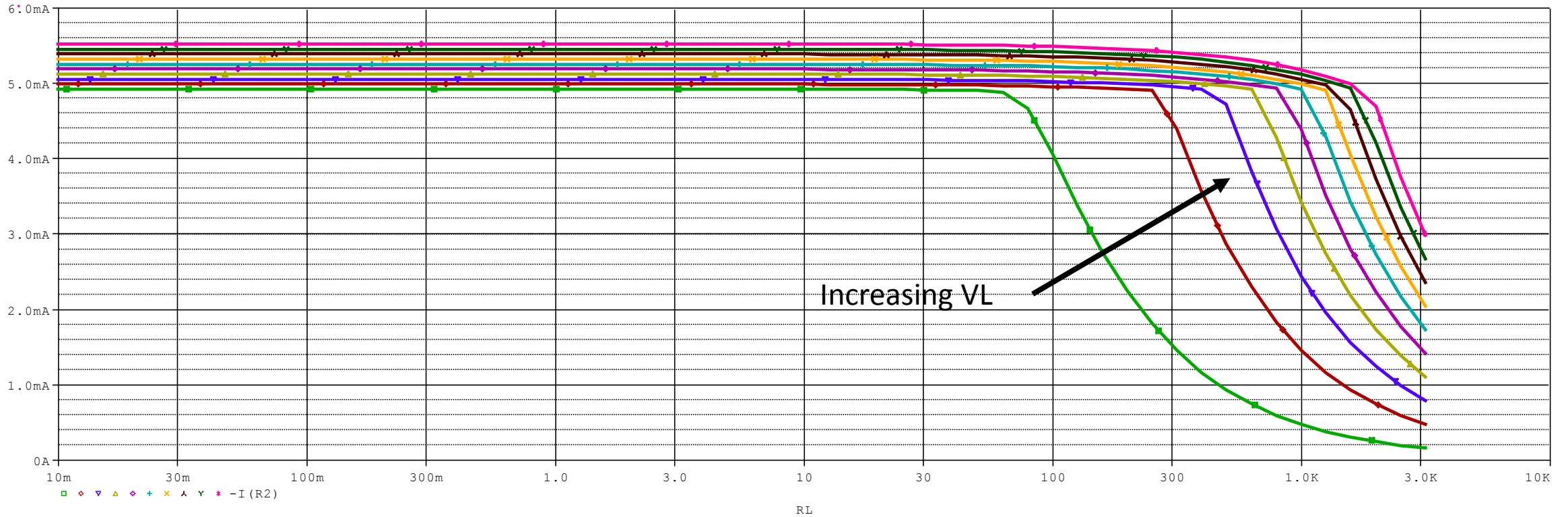
Not a perfect current mirror, as you can see from the bias point simulation, but close enough.

Parametric sweep on RL on the next slide



The current mirror works for a load resistance up to about 516 Ω .

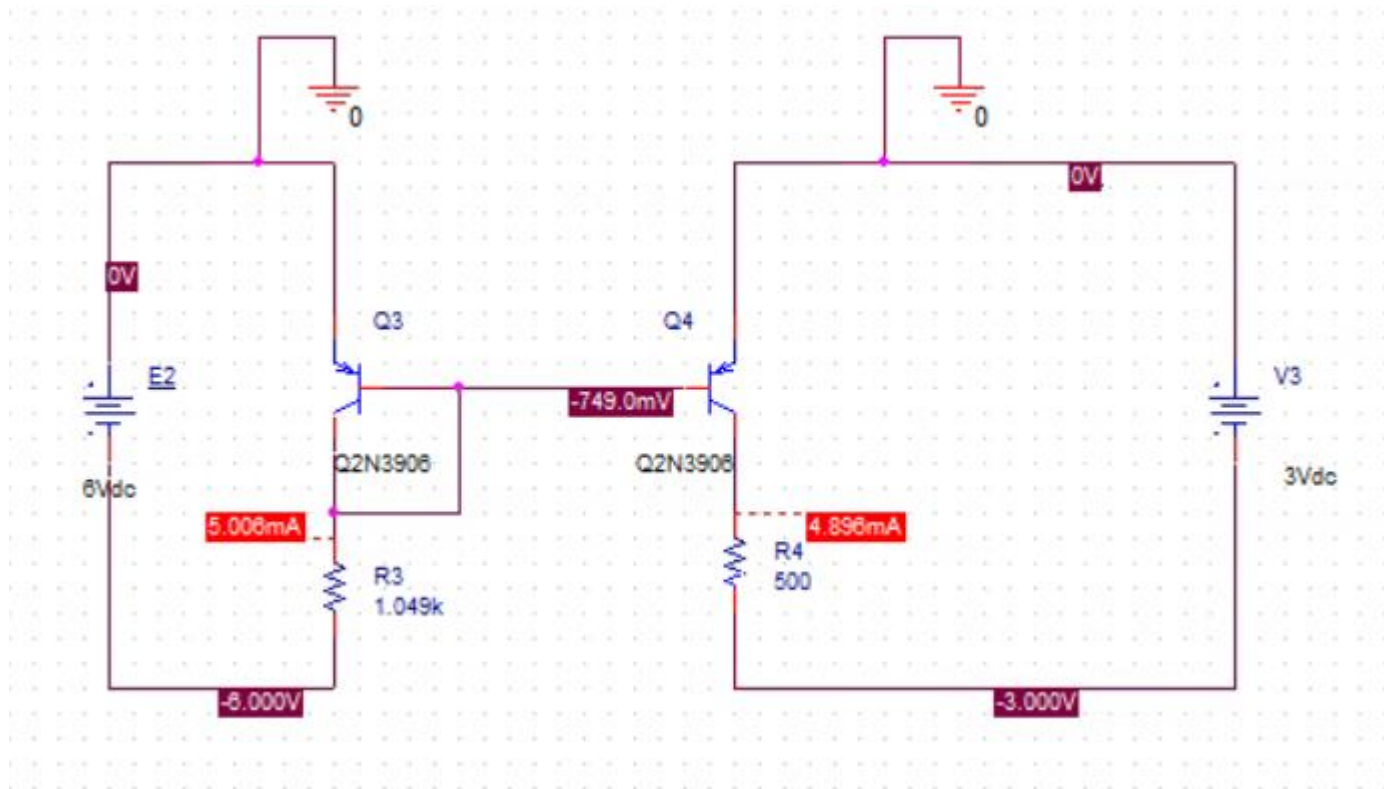
I just arbitrary chose 3V for the load-side battery. What happens if I vary the voltage of that battery? (Next slide)



The different curves are load batteries ranging from 0.5 V to 10V. As you can see, increasing the load voltage will increase the range of R_L for which the mirror can work, but it also slightly increases the mirrored current. If the load battery is too high, the mirrored current goes up to about 5.5mA. It looks like the best choice for the load battery voltage would be the red or blue curves, which are 1.5V and 2.5V respectively.

The pspice approach is the same for the rest of the current mirrors. I will just give some example schematics.

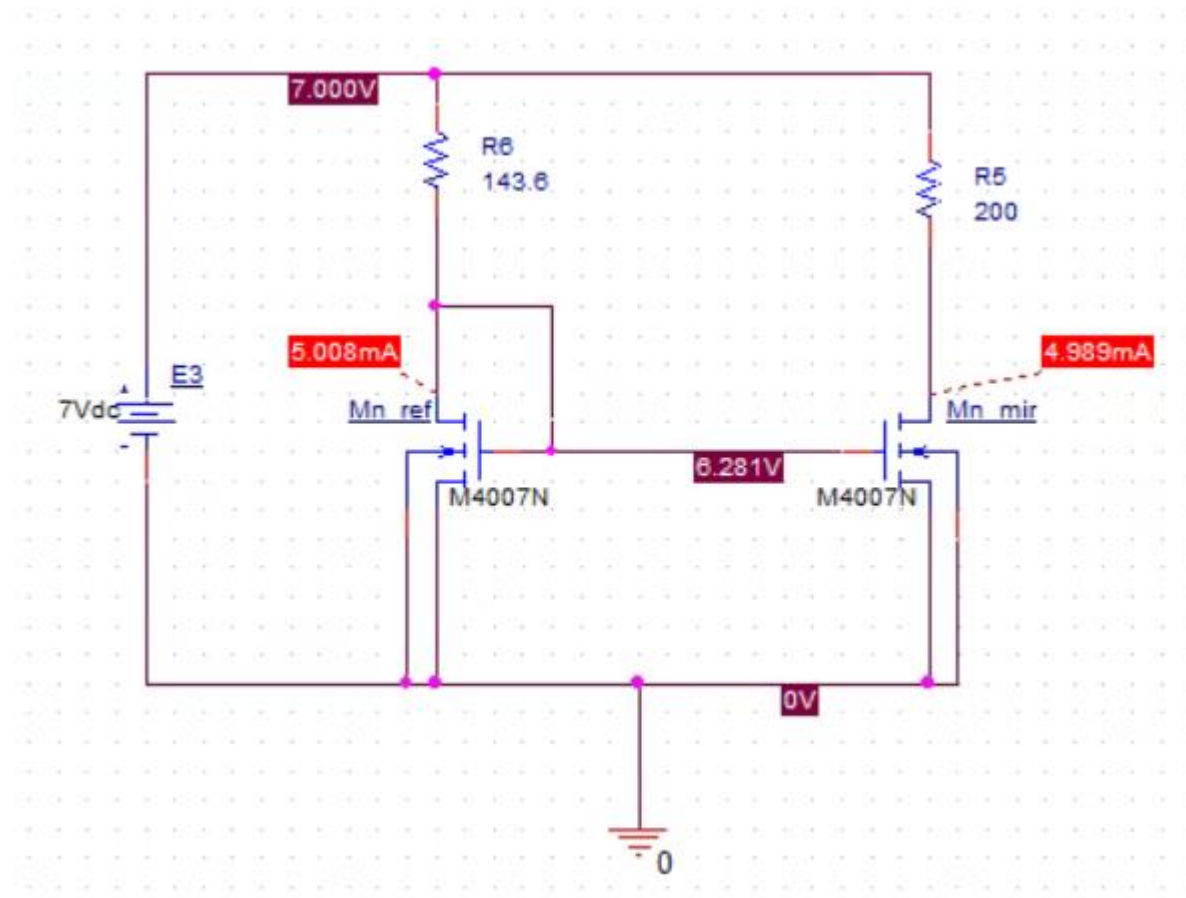
Current-sourcing BJT: Uses PNP transistors



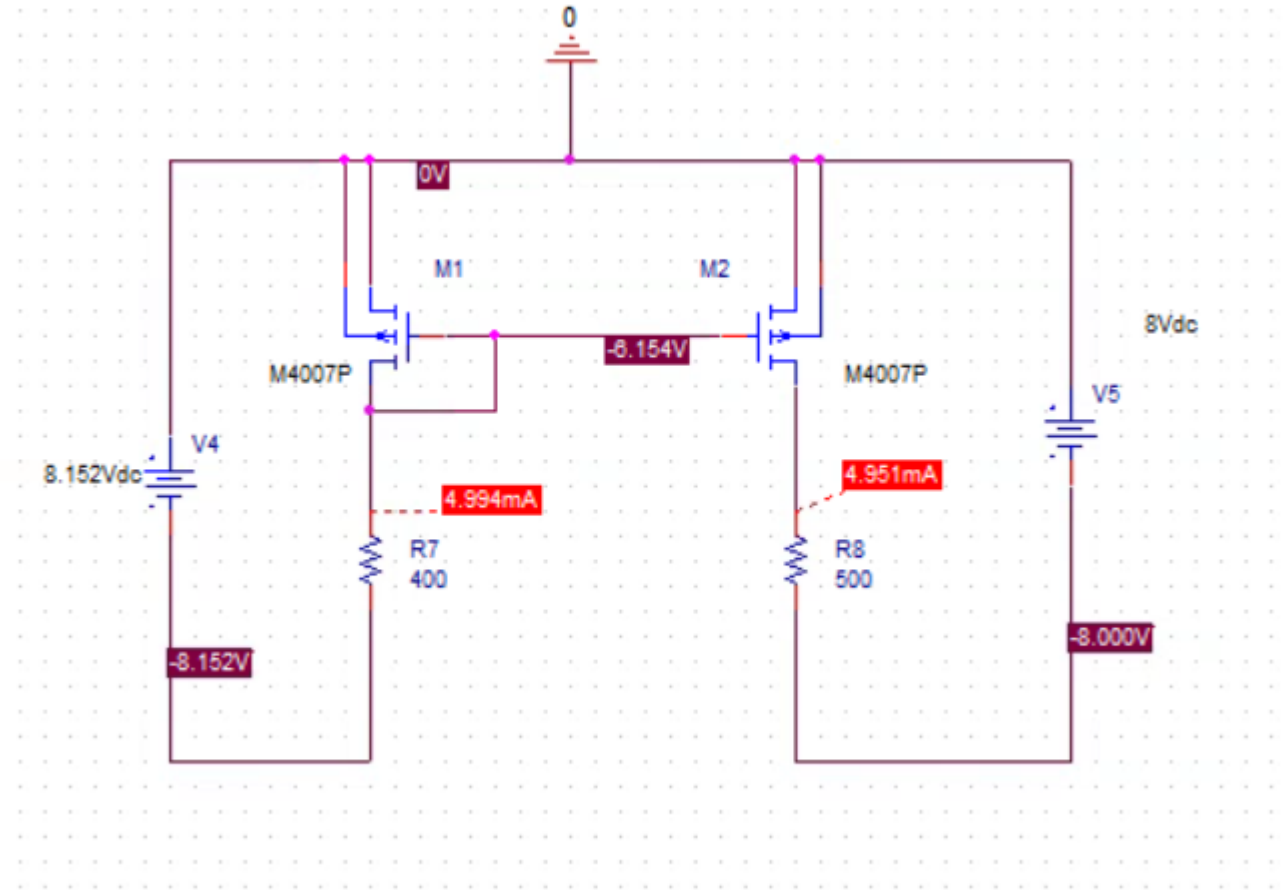
Notice that I placed ground up top now, so that the two transistors can get the same voltage from base to emitter(ground) V_{be} . In my simulation that voltage was about -0.75V.

The bottom nodes of the schematic have negative voltages.

Current-sinking MOS: Uses NMOS transistors



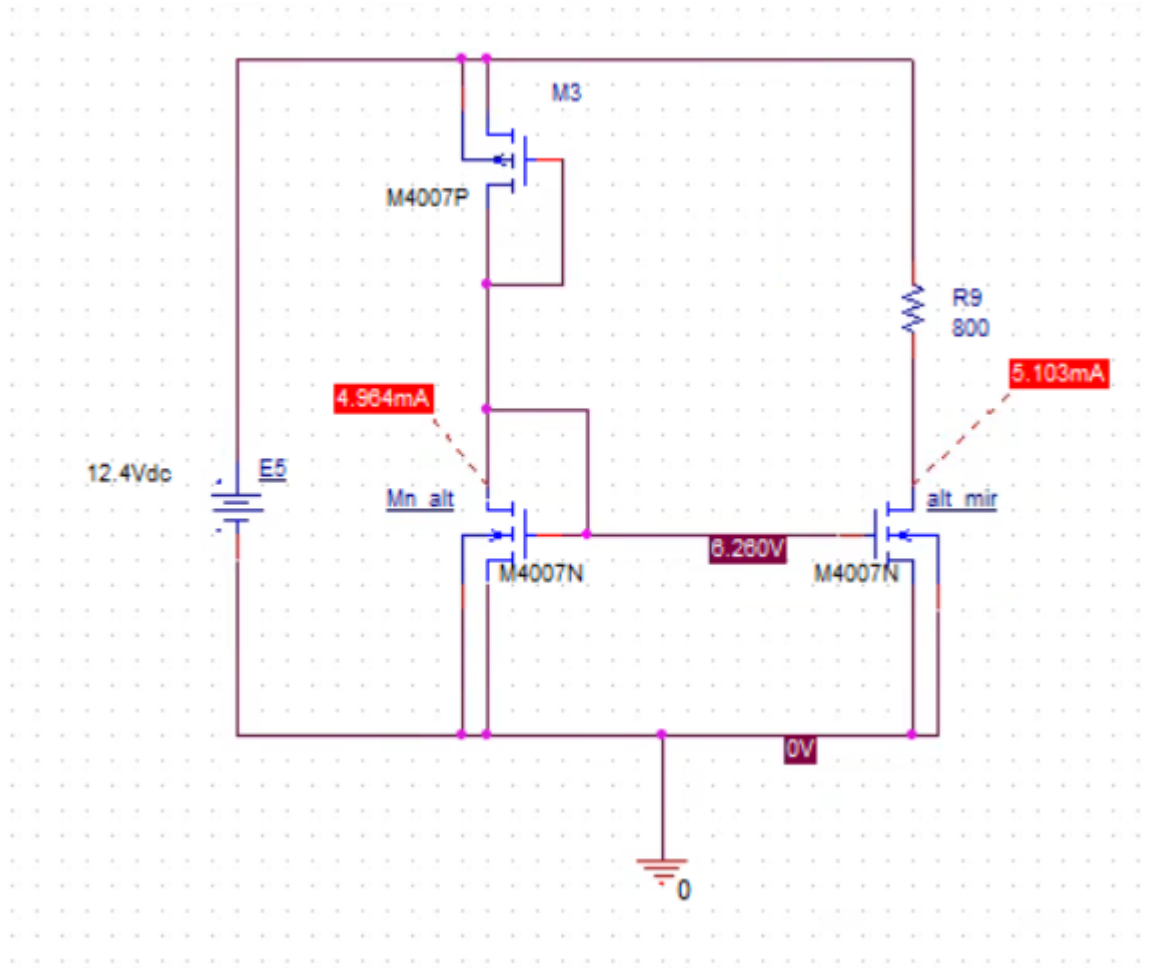
Current-sourcing MOS: Uses PMOS transistors



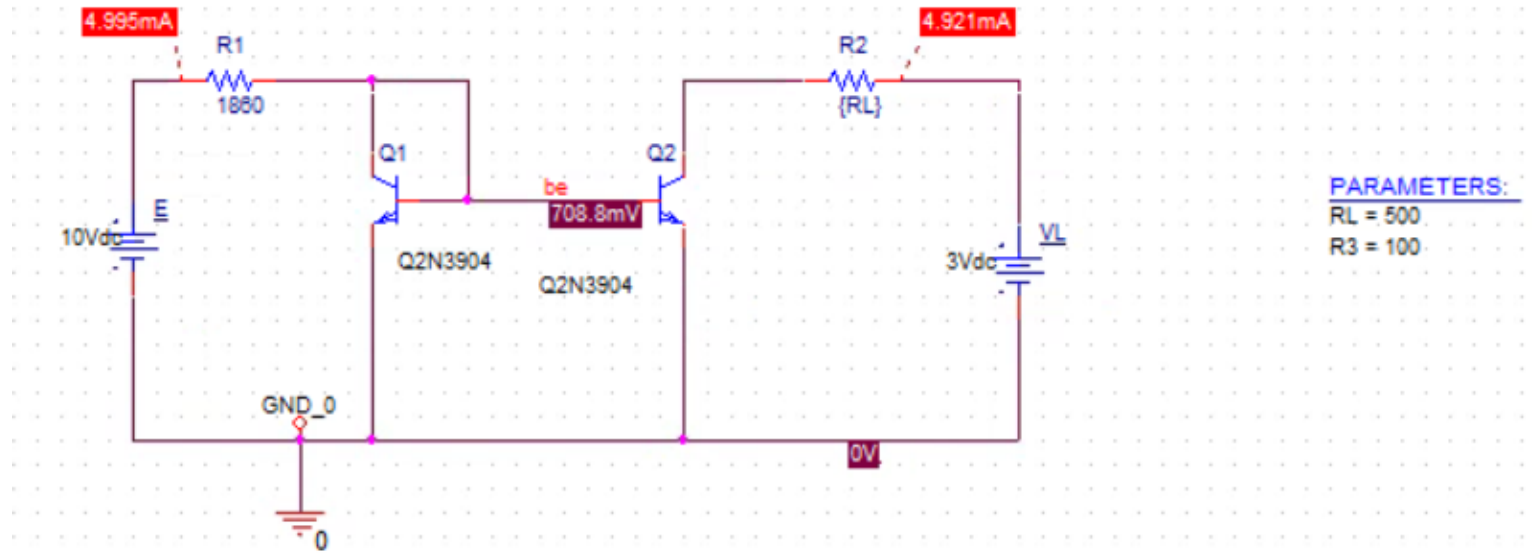
b. Check your designs in Spice by placing a resistor load on an output transistor and comment upon what values of the load the circuit acts as a valid mirror.

I gave an example of this for the NPN sink. It's pretty straight-forward to do a parametric sweep on the load resistance and see the range for which you can get a mirror current close to 5 mA.

c. By replacing the current determining resistor by a PMOS transistor, repeat the above two parts for the current sinking MOS mirror.



d. For any one of the four circuits of part a, discuss what happens if only 10% resistors of commercially standard sizes are available.



Consider the NPN source:

$$V_{R1} = E - V_{be}$$

$$i_{R1} R_1 = (E - V_{be})$$

$$i_{R1} = \frac{E - V_{be}}{R_1}$$

What if R_1 is 10% greater than the value you desire?

$$i_{R1} = \frac{E - V_{be}}{11R_1/10} = \frac{10(E - V_{be})}{11R_1}$$

The current would be $(10/11)$ of its desired value $\sim 91\%$. Similarly, if R_1 was 10% less than the expected value, R_1 would be $9/10$ of its desired value, and the current would be $10/9$ the desired value $\sim 111\%$. So the current could vary by $(111\% - 91\%) = 20\%$ total.

This could be really bad if you are trying to operate a device with a very specific current range.