

HW 3

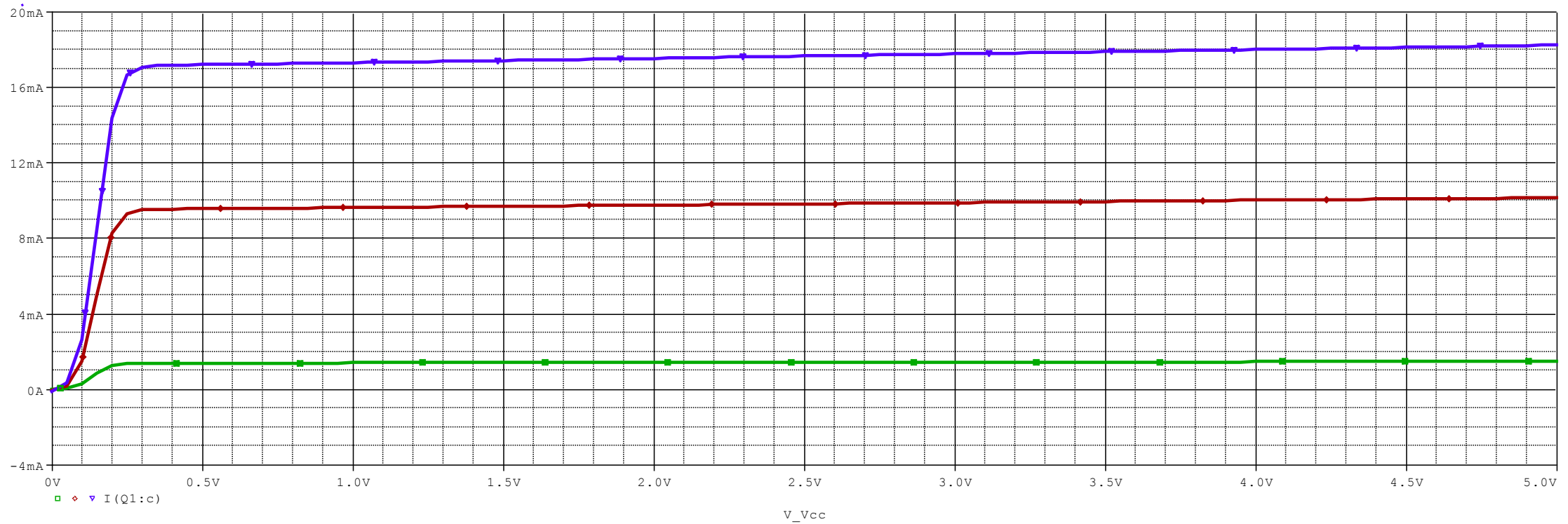
1. (50 points, BJT curves & equivalent) For the 2N3904 =(nnp) and the 2N3906 =(pnp)
 - a) Obtain in Spice the transistor curves given on the course web page except do in separate plots, one for the npn in the first quadrant and one for the pnp in the third quadrant.

The example curves and the pspice schematic can be found here:

http://www.ece.umd.edu/~newcomb/courses/fall2013/303H/BJT_curves.pdf

NOTE: you don't need to include the last transistor.

3904 (NPN)



If you plotted these three curves together or separately, either is fine.

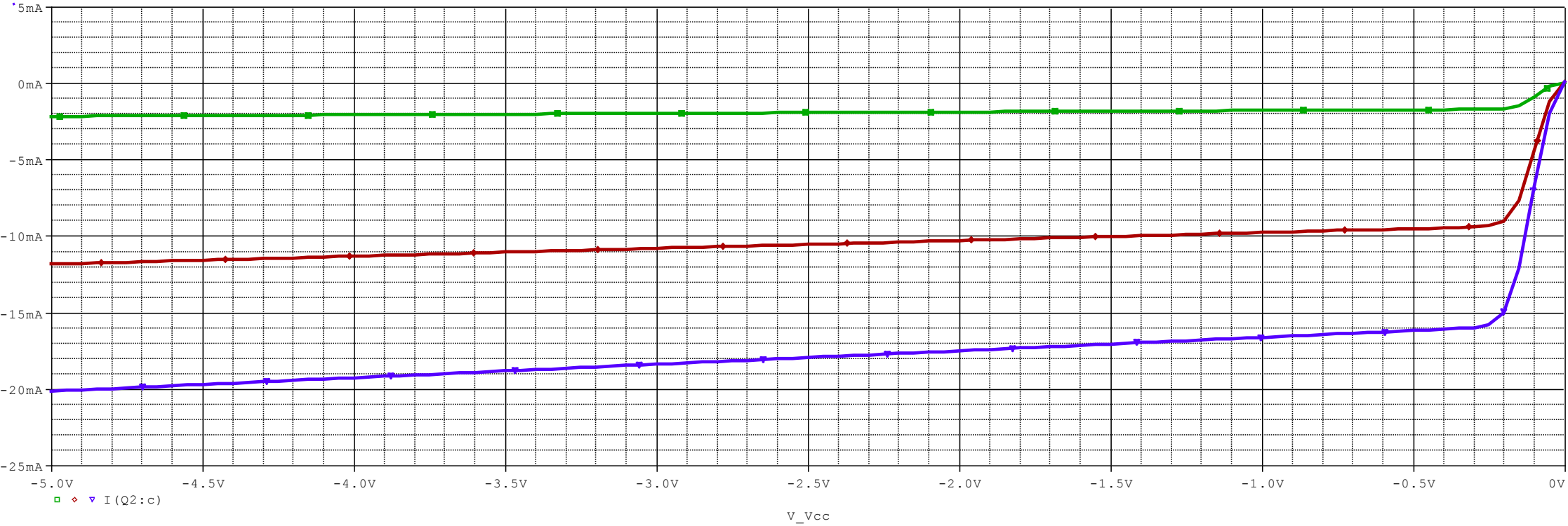
For each plot, the separate curves are separate I_B values:

Green – 10mA

Red – 60 mA

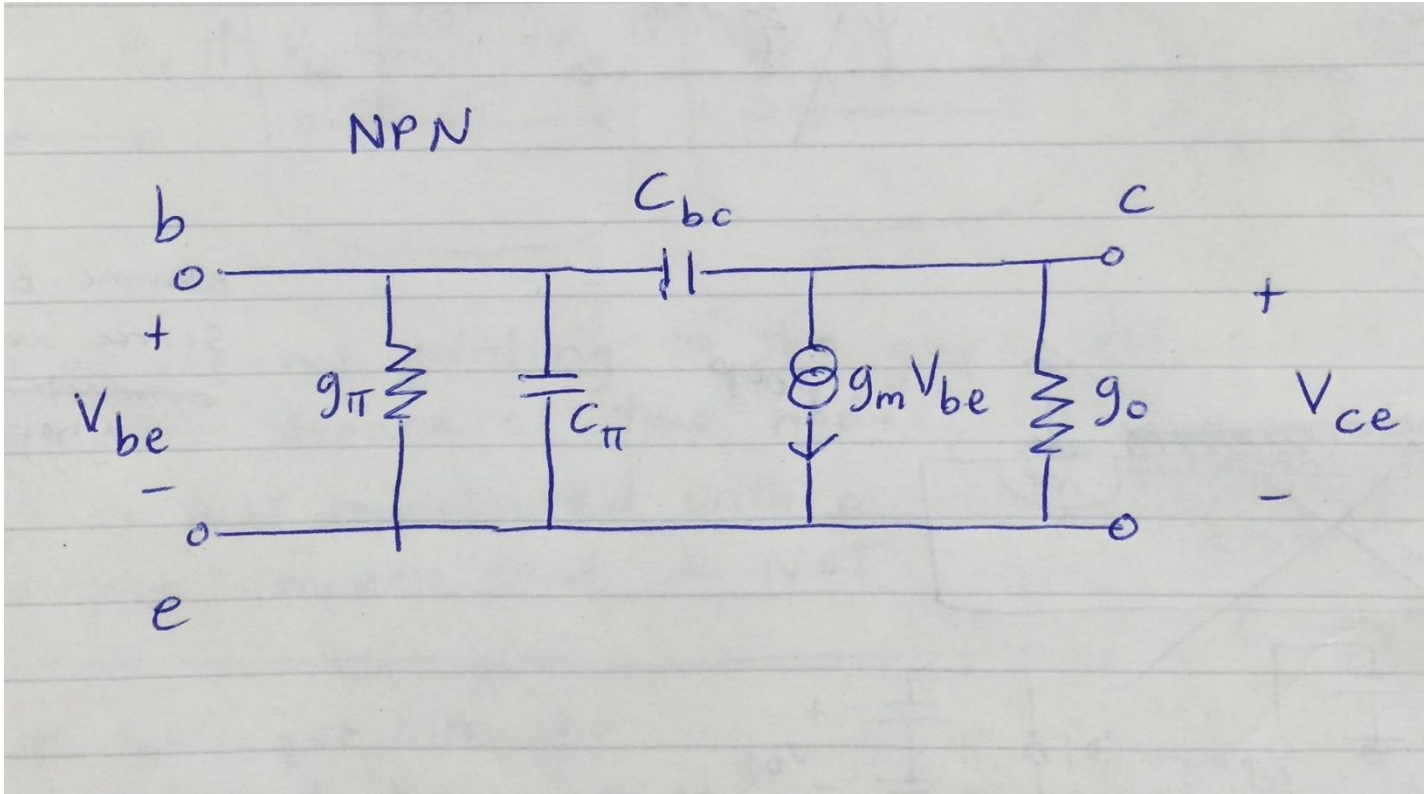
Blue – 110 mA

3906 (PNP)



b) Give for each transistor the hybrid-pi equivalent circuit when operating at $I_C=5\text{mA}$ and $V_{CE}=3\text{V}$. Do this analytically (using equations) and discuss how you could use the Spice curves to check the analytic results

3904 npn



$$V_T \sim 26\text{mV}$$

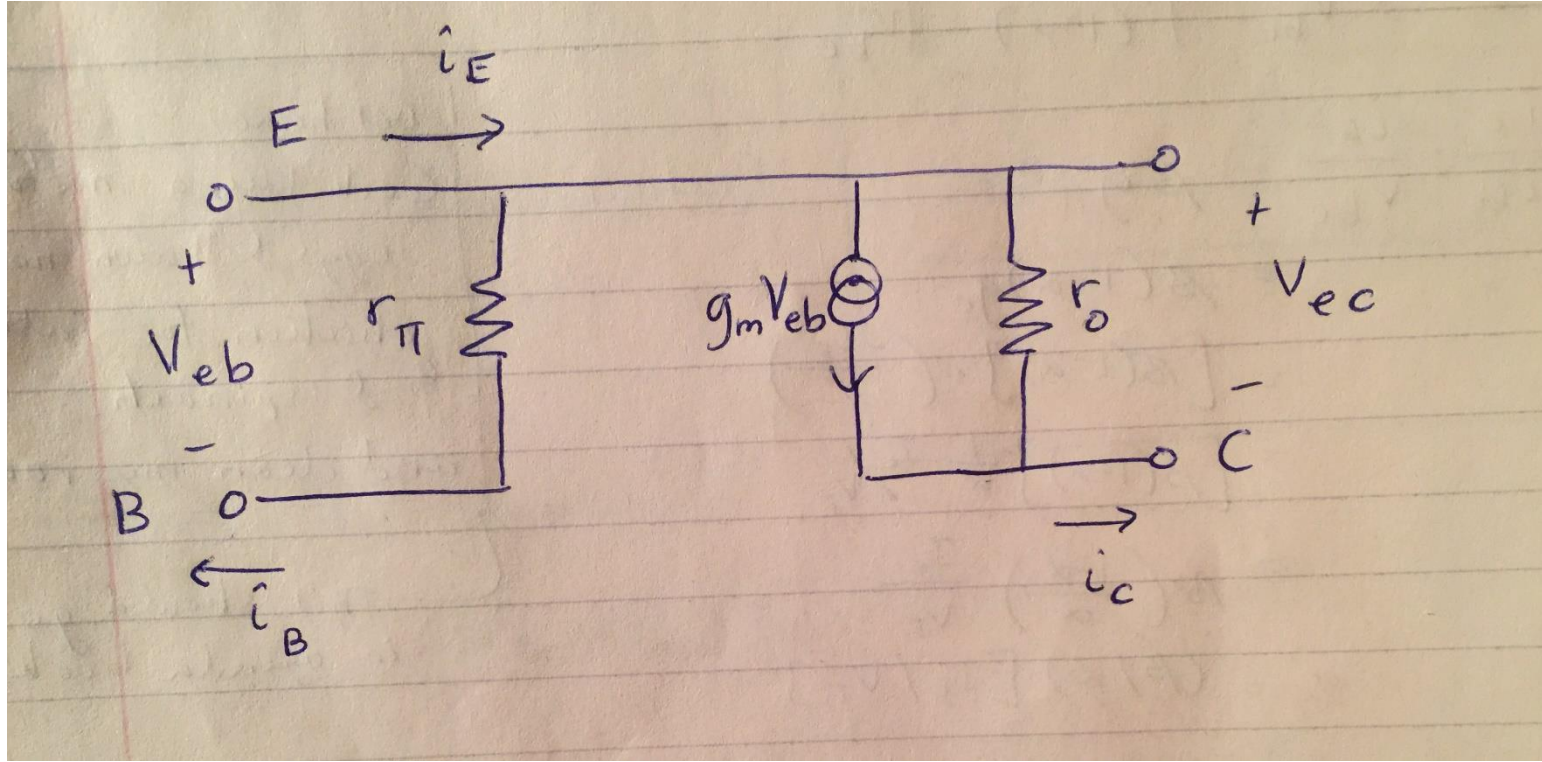
$$g_\pi = \frac{I_C}{\beta V_T} \approx 4.61 \cdot 10^{-4}$$

$$g_o = \frac{I_C}{V_A} \approx 6.76 \cdot 10^{-5}$$

$$g_m = \frac{I_C}{V_T} = 0.192$$

All "g" in units of Siemens (Ω^{-1})

β and V_A can be found in the pspice model ($B_f \sim 416$, $V_{af} \sim 74$). The capacitors drop out of the model because this is a dc circuit, so their admittance ($j\omega C$) goes to zero.



In this diagram, I wrote r_π and r_o but they are just the reciprocals of g_π and g_o .

$$V_T \sim 26mV$$

$$\beta = 180.7$$

$$V_A = 18.7 V$$

$$g_\pi = \frac{I_C}{\beta V_T} \approx 0.0011$$

$$g_o = \frac{I_C}{V_A} \approx 2.67 \cdot 10^{-4}$$

$$g_m = \frac{I_C}{V_T} = 0.192$$

All "g" in units of Siemens (Ω^{-1})

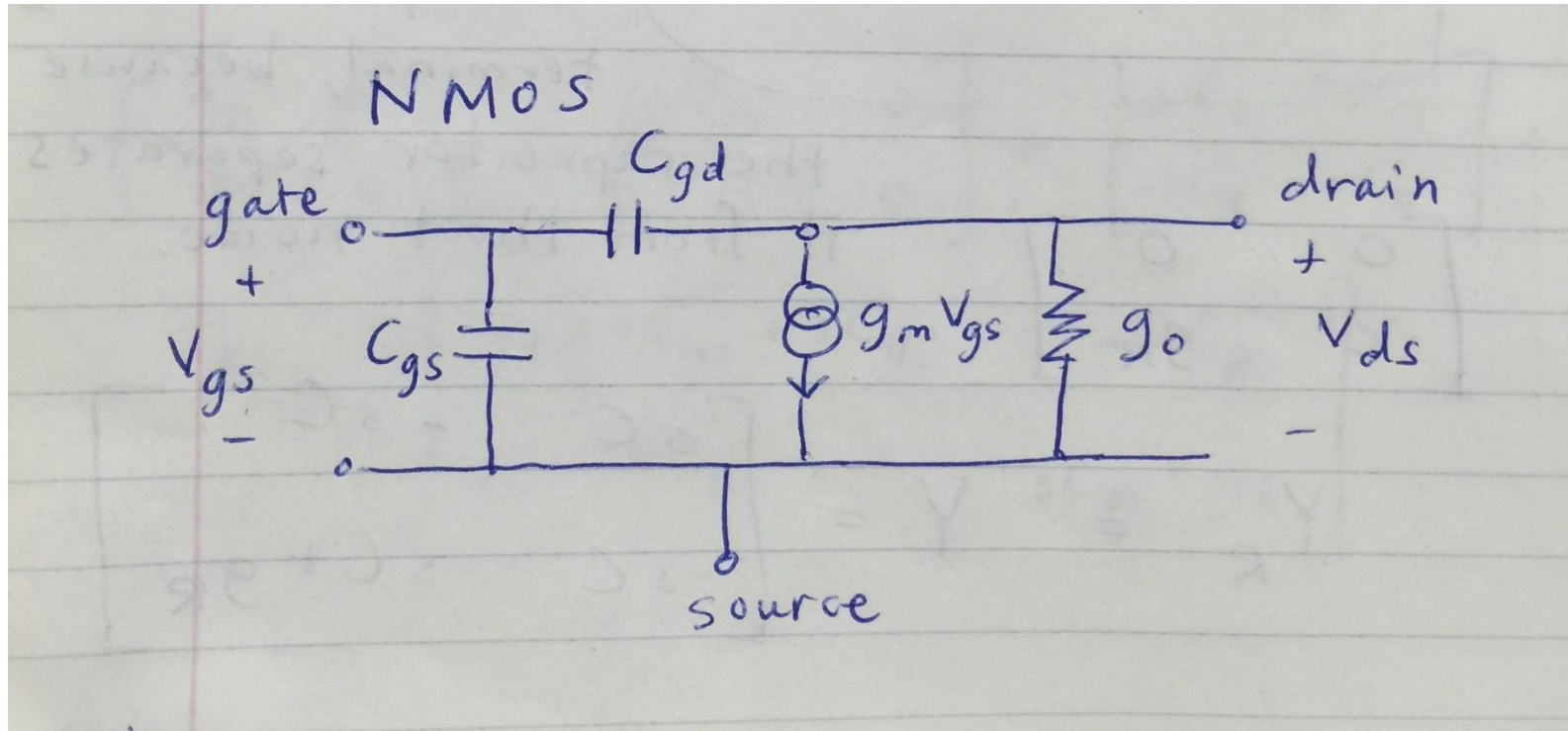
Notice that the model is functionally the same as the NPN, except the voltages and currents have switched signs. You can find g_π , g_o , and g_m in the exact same way (but using the β and V_A in the 3906 model).

You can verify that your hybrid- π equivalent performs the same as your transistor by replacing the transistor with this network of components, connecting to the same base, collector, and emitter terminals. When you run the same DC sweep with the same I_B currents, your results should look almost the same.

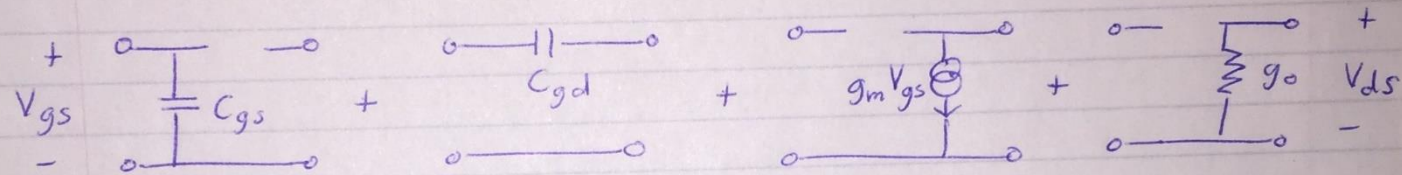
2. (25 points, Y matrix)

a. For the NMOS (common source) give the low frequency admittance matrix

NMOS



NMOS



$$\begin{bmatrix} sC_{gs} & 0 \\ 0 & 0 \end{bmatrix} + \begin{bmatrix} sC_{gd} & -sC_{gd} \\ -sC_{gd} & sC_{gd} \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ g_m & 0 \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & g_o \end{bmatrix}$$

$$= \begin{bmatrix} sC_{gs} + sC_{gd} & -sC_{gd} \\ g_m - sC_{gd} & g_o + sC_{gd} \end{bmatrix}$$

For DC-circuits and low frequency,

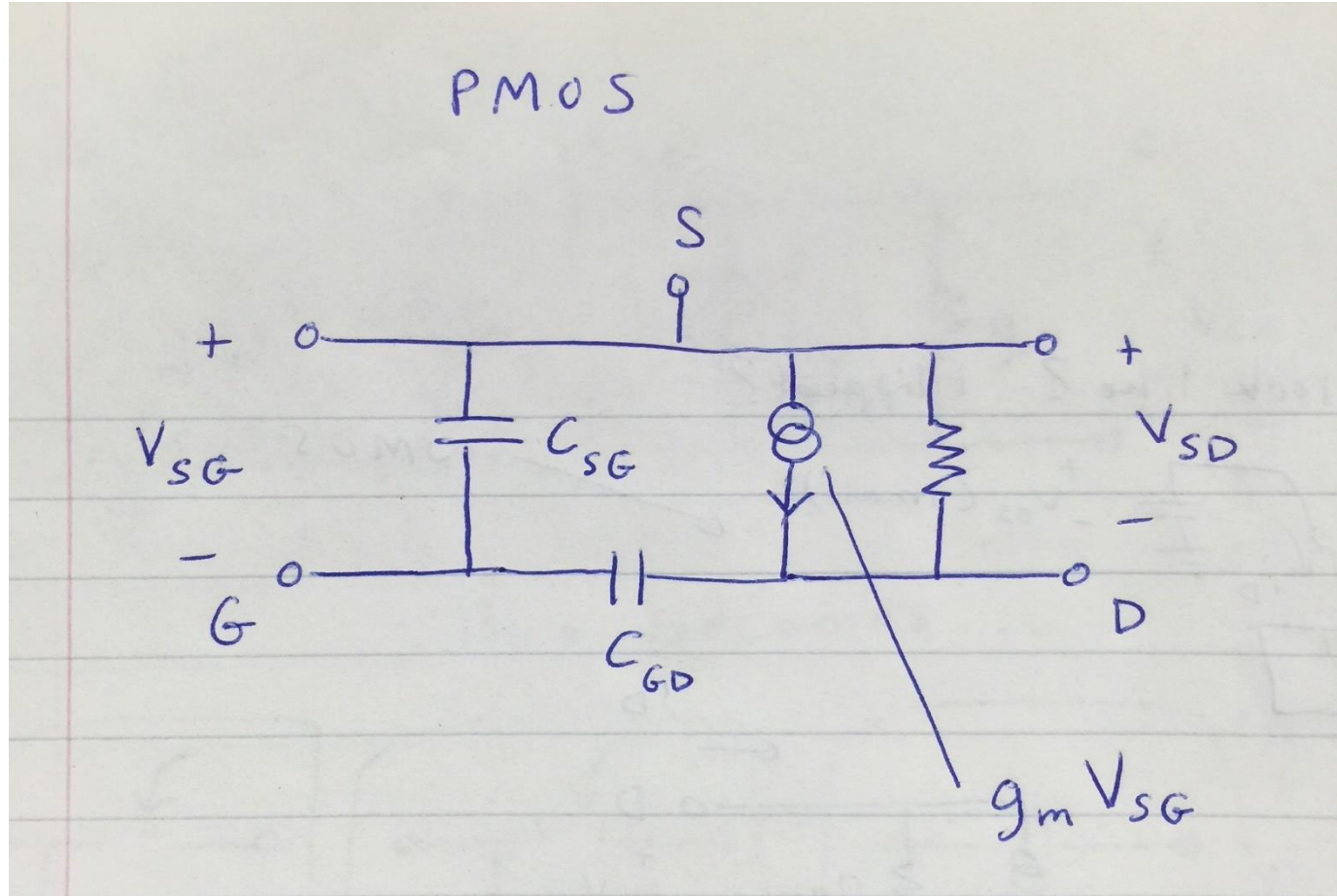
$$\lim_{s \rightarrow 0} = \lim_{j\omega \rightarrow 0} sC_k = 0 \quad \left. \vphantom{\lim_{j\omega \rightarrow 0} sC_k = 0} \right\} \begin{array}{l} \text{capacitors have zero} \\ \text{admittance at low frequency} \end{array}$$

then the matrix becomes

$$\begin{bmatrix} 0 & 0 \\ g_m & g_o \end{bmatrix}$$

b. Repeat for the PMOS (common source)

PMOS

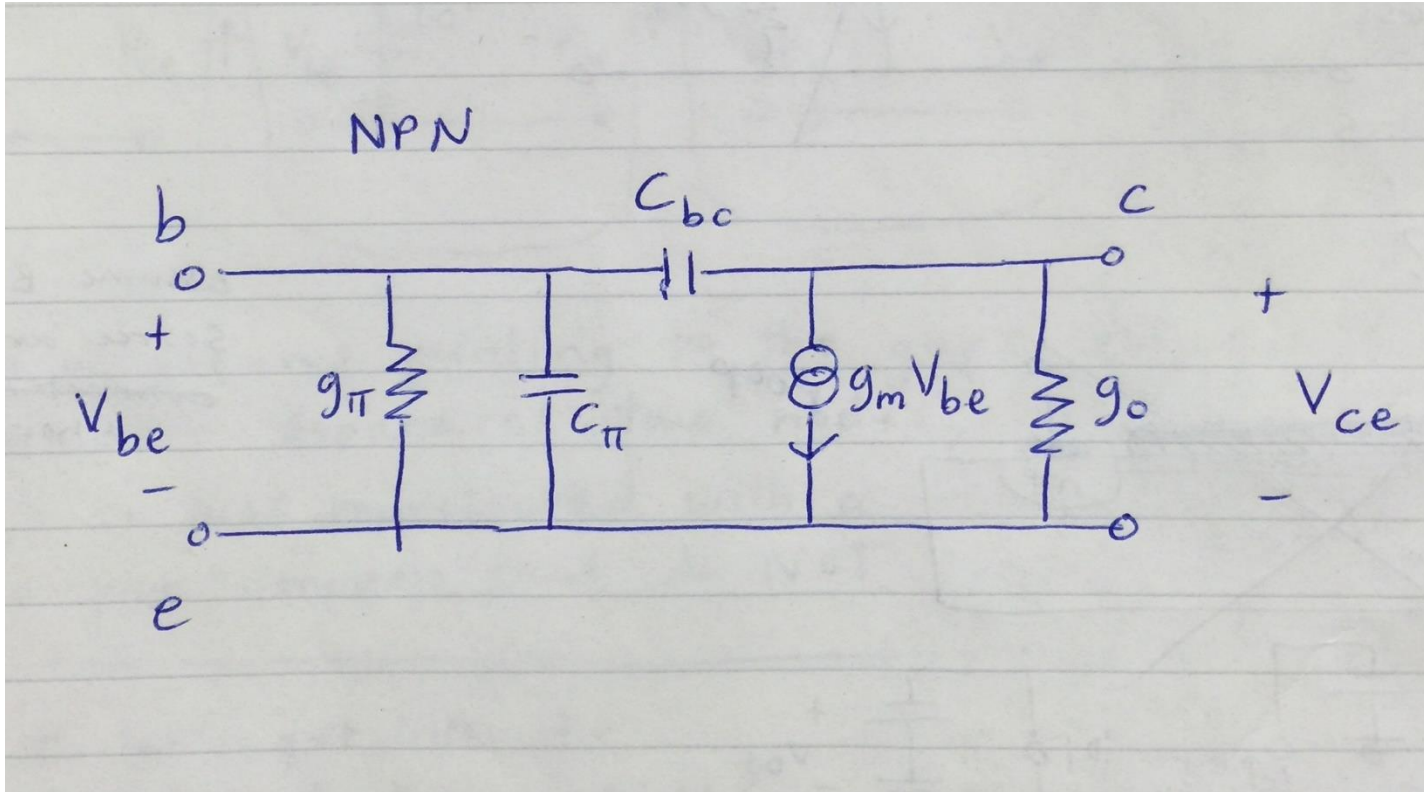


You may have drawn your current source pointing up, but then you must be using the opposite input voltage ($V_{GS} = -V_{SG}$), or label it with $(-g_m V_{SG})$, in which case you will get the same admittance matrix as an NMOS model.

If you have $(-g_m)$ in your matrix, you may still be right, as long as you are consistent with the signs of your voltages and currents.

c. Repeat for the NPN (common emitter).

This is just the hybrid-pi equivalent again from problem 1.



It's important to note that the only difference between the MOSFET equivalent model and the BJT equivalent model is the presence of a resistor on the input side for the BJT. This additional component allows the "input current" to directly affect the output current. BJTs can be thought of as a Current-Controlled Current Source.

The MOSFET model has NO relationship between the input current and the output current. Current cannot pass from the gate to the source or drain. A MOSFET acts as a Voltage-Controlled Current Source.

$$= \begin{array}{c} \text{Circuit Diagrams} \\ + \\ + \\ + \\ + \\ + \end{array}$$

$$= \begin{bmatrix} g_{\pi} & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} sC_{\pi} & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} sC_{bc} & -sC_{bc} \\ -sC_{bc} & sC_{bc} \end{bmatrix} \begin{bmatrix} 0 & 0 \\ g_m & 0 \end{bmatrix} \begin{bmatrix} 0 & 0 \\ 0 & g_o \end{bmatrix}$$

$$= \begin{bmatrix} g_{\pi} + sC_{bc} + sC_{\pi} & -sC_{bc} \\ g_m - sC_{bc} & sC_{bc} + g_o \end{bmatrix}$$

Low frequency :

$$\begin{bmatrix} g_{\pi} & 0 \\ g_m & g_o \end{bmatrix}$$

d. Compare numerically for an NMOS 4007 and a comparable npn 2N3904 both biased at the same (output) current level, $I_C = I_D = 5\text{mA}$ (and $V_{gs} = 3\text{V}$, which was specified later).

Npn 2N3904:

$$g_{\pi} = \frac{I_C}{\beta V_T} = \frac{5\text{mA}}{416 \cdot 25\text{mV}} \sim 4.61 \cdot 10^{-4} (\text{very small admittance})$$

$$g_m = \frac{I_C}{V_T} = \frac{5\text{mA}}{25\text{mV}} = 0.192$$

$$g_o = \frac{I_C}{V_A} = \frac{5\text{mA}}{74\text{V}} \sim 6.76 \cdot 10^{-5} (\text{again very small})$$

All “g” in units of Siemens (Ω^{-1})

$$Y = \begin{bmatrix} 4.61 \cdot 10^{-6} & 0 \\ 0.2 & 6.8 \cdot 10^{-6} \end{bmatrix} \text{ S}$$

NMOS 4007:

λ and V_{th} can be found in the M4007N model on the class website (as “lambda = 15m” and “Vto = 1.3”)

$$g_m = \frac{2I_D}{(V_{GS} - V_{th})} = \frac{2I_D}{(V_{GS} - V_{to})} = \frac{2 \cdot 5\text{mA}}{3\text{V} - 1.3\text{V}} \sim 5.88 \cdot 10^{-3} \text{ S}$$

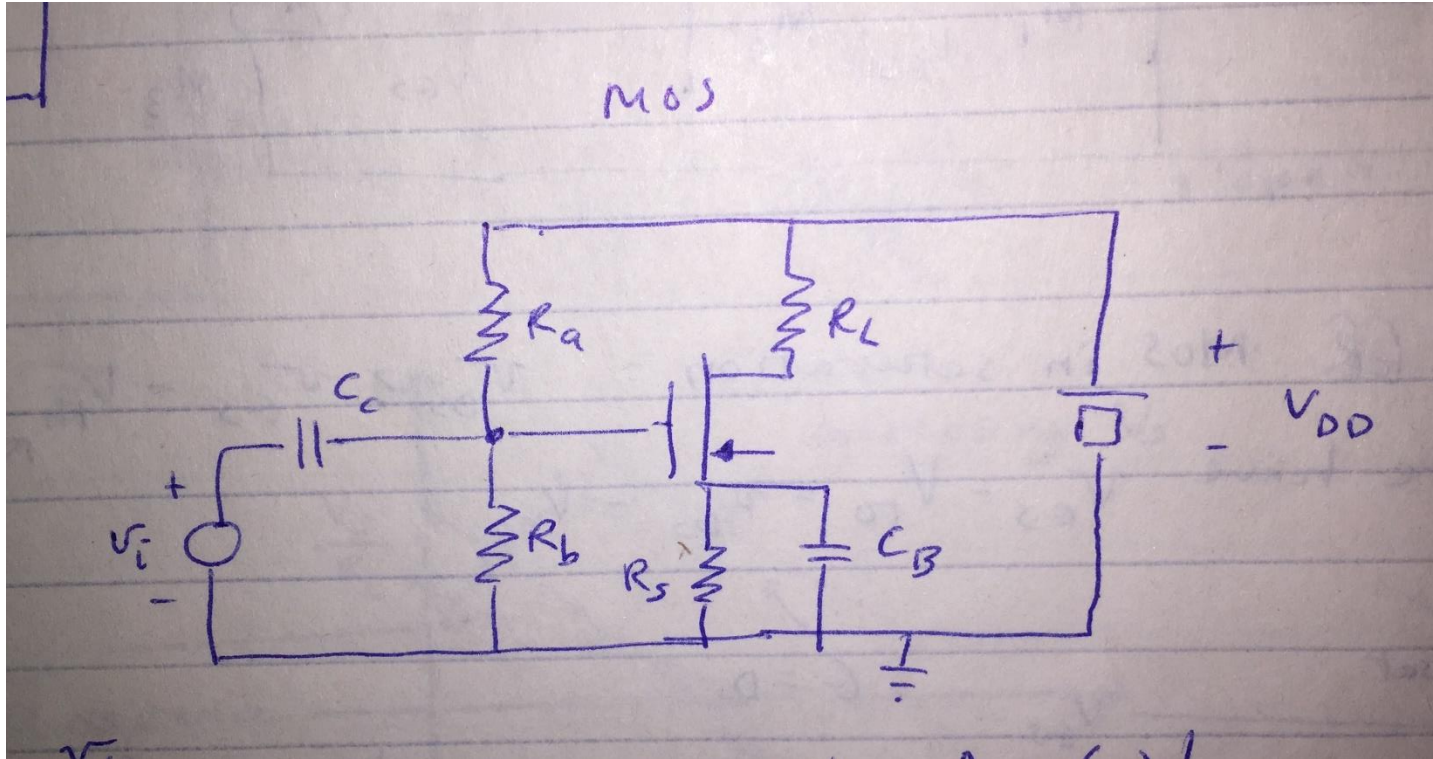
$$g_o \sim I_D \lambda = (5\text{mA})(15 \cdot 10^{-3}) = 75 \cdot 10^{-6} \text{ S}$$

$$Y = \begin{bmatrix} 0 & 0 \\ 5.88 \cdot 10^{-3} & 75 \cdot 10^{-6} \end{bmatrix} \text{ S}$$

The ideal admittance matrix for a transistor only has a (g_m) value in the lower left, which represents the gain (output current over input voltage). You would like the other admittance elements to be zero. You can see that a MOSFET is advantageous for this reason, because it has 1 fewer non-zero element than the BJT. In the 4007 and 3904, we see that the non-gain admittance values are very small, which is good. Higher non-gain admittances mean that the transistor has unwanted behavior in the circuit. The 3904 has a higher gain (g_m) which may or may not be desired, depending on the situation. Note that the MOSFET (4007) gain depends on the input voltage, whereas the BJT (3904) gain does not.

3. (25 points, CS amplifier) Assume an NMOS 4007 is biased at $I_C=12\text{mA}$ for $R_L=120\ \Omega$, find the range of gains available by varying the load resistance (assume a signal source resistance of $R_S=0$ and a 9V power supply).

When biasing a MOSFET transistor, your circuit should generally look like this:



R_L is the load

R_a and R_b are used as a voltage divider to get the right voltage at the gate V_{GS} .

C_C is the coupling capacitance

C_B is the bypassing capacitance

R_S is the source resistance

V_{DD} is a DC battery

v_i is the oscillating signal (input voltage)

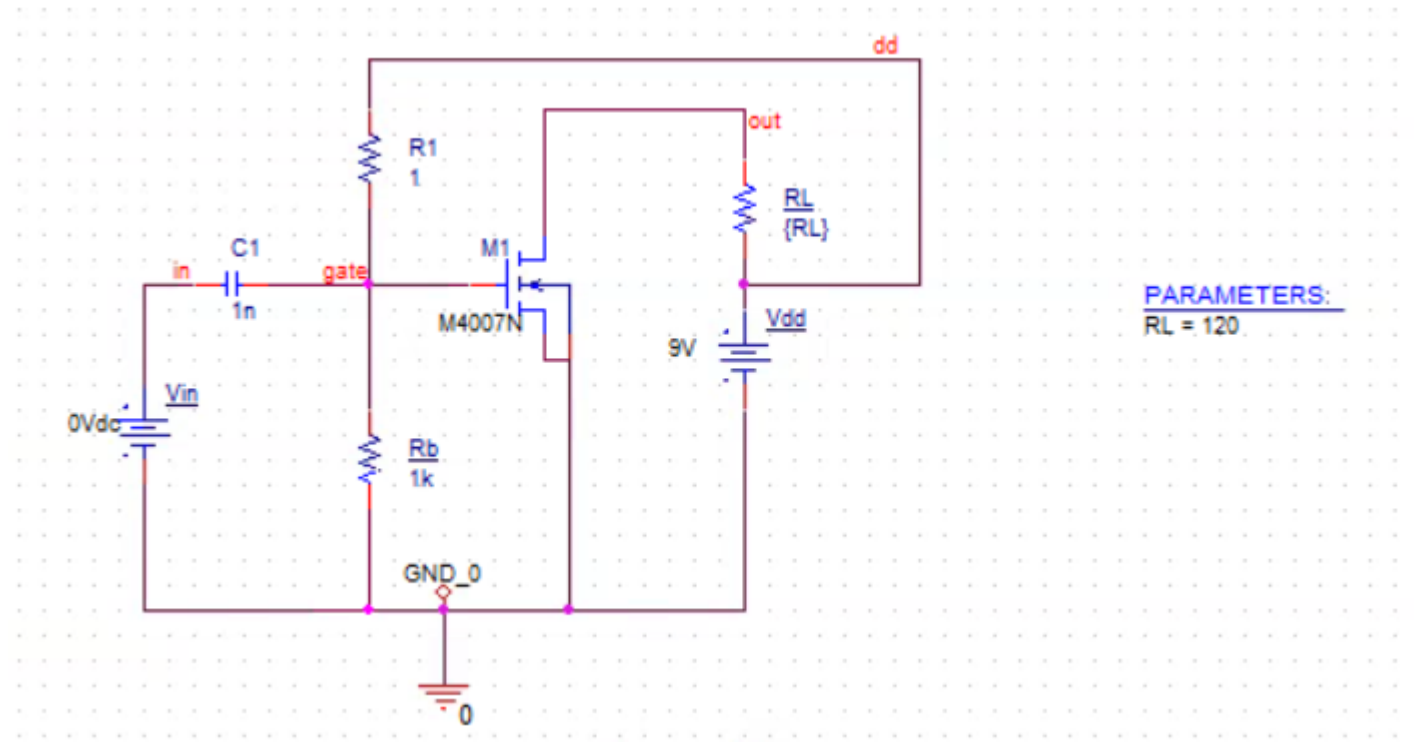
Since the source resistance is zero, you may replace the R_S and C_B with a short-circuit (voltage source to ground is zero). The gain is measured as

$$\frac{v_o}{v_{in}} = v_{load}/v_{in}$$

The desired I_C is 12 mA. To get this current at $V_{DD} = 9V$, look at this curve, for the NMOS (top graph):

http://www.ece.umd.edu/~newcomb/courses/spring2006/303/4007_transcrvs.pdf

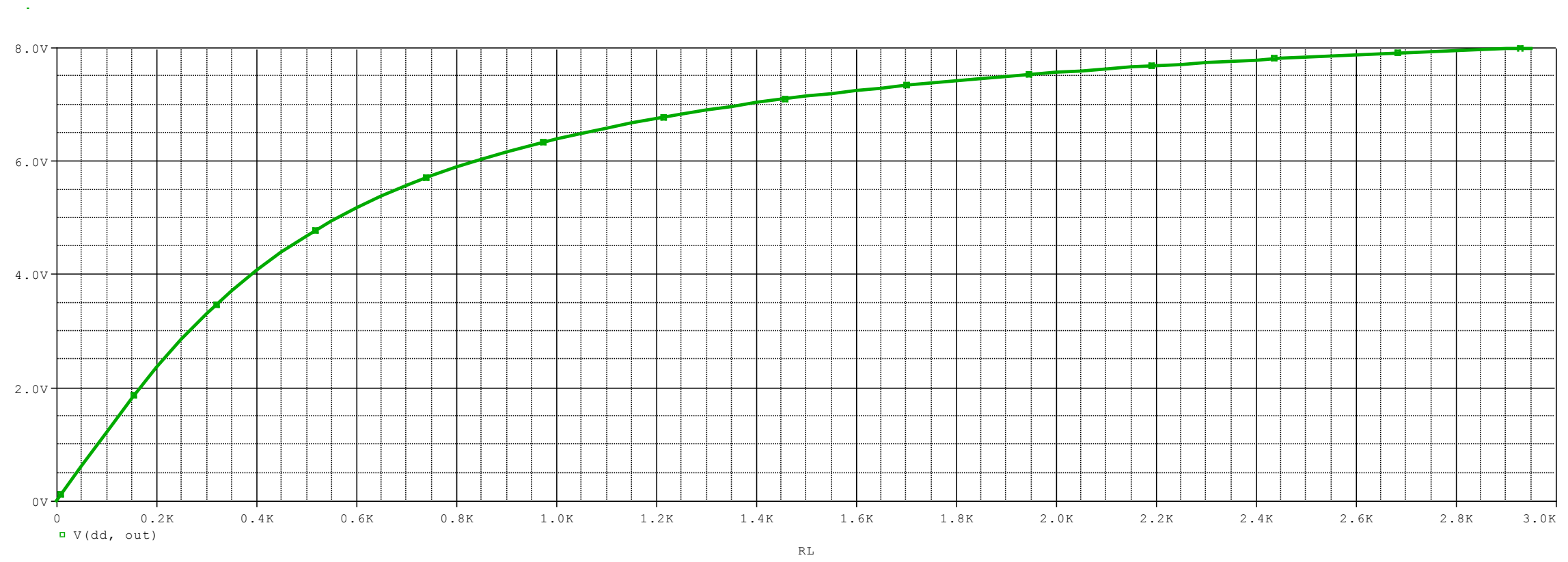
It looks like $V_{GS} \sim 9V$ is necessary. This means that the battery voltage will NOT need to be reduced at all, so R_a in the circuit may be zero, and R_b can be anything you choose.



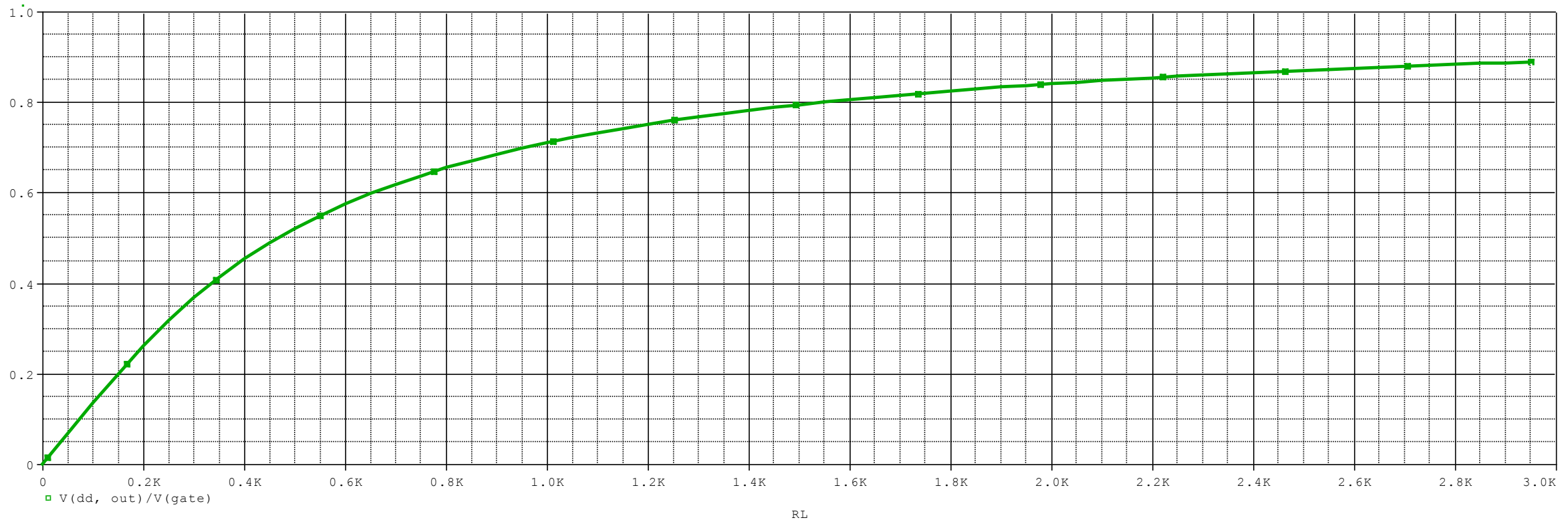
I left the Cc as the default pspice capacitance, 1 nF. In fact, I didn't really use the V_{in} signal for this problem, so that capacitance doesn't matter. Instead of leaving R_a out entirely, I set it equal to 1Ω (which is essentially zero).

Make the simulation profile a DC sweep, and for the primary sweep tab, select “Global Parameter”: run a sweep on the RL load resistance. I varied it from 0.01 ohms to 3000 ohms.

It appears that the voltage reaches 8V, as RL approaches 3000Ω, but it probably goes to 9V.



If I use a trace that is $V(\text{dd, out})/V(\text{in})$, that will show the gain v_{out}/v_{in} . I am using the gate to source voltage v_{GS} as the v_{in} .



Of course, the minimum gain is 0 when R goes to zero, because $v_{load} = v_{out} = i_{load}R_{load}$, so v_{out}/v_{in} goes to zero. It appears that the gain maxes out around 1 if I tested higher resistances (If we are measuring the gain as v_{Load}/v_{GS} . Note that the actual value of the gain could be much higher if we were measuring it as the amplitude of the load with respect to a small time-varying signal (v_{in}). But the plot would still have a similar shape). This makes sense for this circuit. v_{in} is approximately equal to $v_{dd} = 9V$. It is not possible for v_{load} to exceed the battery voltage, because $v_{dd} = v_{load} + v_{DS}$.