

11/12/2003
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TITLE

Current Mode Technique for high speed VLSI circuits with application to current sense amplifier for CMOS SRAM's

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Date: 11/12/03

INTRODUCTION

- Long wire delay caused by interconnect
 - Large capacitive loads
 - Large voltage swings
- Solution
 - Current signals with hardly any voltage swing
 - Current spikes
 - Substrate voltage modulation

OUTLINE

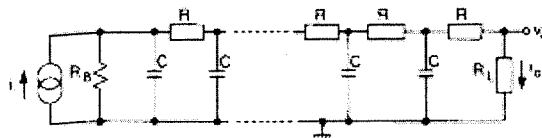
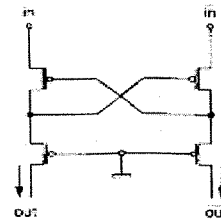
- Voltage Mode Vs. Current Mode

$$\delta t_1 = \frac{R_T C_T}{2} \cdot \left(1 + \frac{2 R_B}{R_T} \right).$$

$$\delta I = \frac{R_T C_T}{2} \cdot \left(\frac{R_B + \frac{R_T}{3} + R_L}{R_B + R_T + R_L} \right) + R_B C_T \cdot \left(\frac{R_L}{R_B + R_T + R_L} \right)$$

$$\delta t_i = \frac{R_T C_T}{2} \cdot \left(\frac{R_B + \frac{R_T}{3}}{R_B + R_T} \right)$$

- Low Resistance Current Transporting Circuits
- Current Sense Amplifier for Fast CMOS SRAMS
- Current Sensing SRAM Data-Path Alternatives
- Speed Performance of current sensing Vs. Voltage Sensing in SRAM data path
- Conclusion
 - Typical SRAM bit-line delay decrease from 5ns to 0.3ns
 - Sensing delay of 2ns with current 140uA
 - Virtual short circuit of current sense amp ensures equal bit-line voltages therefore eliminates the need for bit-line equalization during a read access



COMPARISON OF CURRENT-SENSING AND VOLTAGE-SENSING
SENSE AMPS FOR $C_{BI} = 2 \text{ pF}$

	Current sense amp	Voltage sense amp
Delay	2 ns	6 ns
Current consumption	140 μ A	500 μ A

