3D Design Notes and Examples

Introduction
Lincoln Laboratory has developed a three-dimensional (3D) integrated circuit technology in which circuit structures formed on several silicon-on-insulator (SOI) substrates may be integrated into a 3D integrated circuit. The building blocks of the 3D circuit integration technology are fully depleted SOI circuit fabrication, low-temperature wafer-wafer oxide bonding, precision wafer-wafer alignment, and electrical connection of the circuit structures with dense vertical interconnections. When compared to conventional bump bond technology, this 3D technology offers better circuit-to-interconnect ratio, higher-density vertical interconnections, and reduced system power. The purpose of this section is assist the 3D designer by describing the integration process and highlighting some unique design requirements.

3D Circuit Integration
3D circuits are fabricated by transferring and interconnecting the active sections of wafers fabricated on 150-mm SOI substrates to a base wafer. The active section, labeled a tier, in a 3D system of \( n \) tiers consists of the interconnect and active silicon and is transferred to the base tier, tier 1, which can be either a bulk or SOI wafer. Since all 3D circuits that are designed as part of the digital 3D Multiproject program will be composed of three SOI tiers, the base wafer will also be SOI. The 3D circuit integration process begins with the fabrication of three fully depleted SOI tiers as shown in Fig. 1. Then wafer 2 is inverted, aligned, and bonded to wafer 1 as shown in Fig. 2. The handle silicon is removed from tier 2, 3D vias are etched through the oxides of tiers 2 and 1 and stop on metal pads in tier 1, and tungsten is deposited and planarized using chemical-mechanical polishing (CMP). The structure shown in Fig. 3 is a 2-tier assembly with electrical connections between the top-level metal of tier 2 and the top-level metal of tier 1. Tier 3 is transferred to the 2-tier assembly using the same processes except that the 3D vias connect the top-level metal of tier 3 to the first metal level of tier 2, as shown in Fig. 4. The completed 3D assembly is shown in Fig. 5 after bond pads are etched to expose the back of the first level metal of tier 1 for probing and wire bonding. A detailed list of layer thicknesses is contained in Fig. 6.

3D Design Practices
The layout of each tier of a 3D circuit should be done as in a conventional 2D technology. The designer must take into account the integration process discussed above since the two upper tiers will be inverted with respect to tier 1 and the tiers must be designed so that the three tiers will be aligned during fabrication. The layers for each tier will be placed correctly on each reticle with existing layout software provided the designer has designed each tier with coincident origins and laid out each tier to be aligned. Connections between tiers require a 3DCUT which defines the 3D via starting point on the higher numbered tier and 3DLAND which defines the 3D via stopping location on a metal layer on the lower numbered tier. When the tiers are overlaid, each 3DCUT must exactly match the 3DLANDs in the lower tier and each 3DLAND must have a matching 3DCUT in the higher tier. The top of a 3D via starts on the back side of the higher numbered tier, and the 3DCUT dimension determines its size; the size of the 3D via in the lower tier is defined by the doughnut opening in metal 3 of the upper tier. The 3DCUT feature is unique to the 3D technology, but the designer must ensure that the 3DLAND and doughnut features are included in the metal designs of the FDSOI layers. The metal layers of the 3DLAND and doughnut features are shown for each tier in Table 1; the two 3DCUT layers are color coded to associate the 3DCUT layer with the tiers to be interconnected.
**Thermal Management Considerations**

The analysis and control of temperature effects in a 3D circuit is a topic of current research. The designer can reduce the effects of power dissipation on the operation of 3D circuits by placing the circuits that dissipate the most power in tier 1 since the base of tier 1 is the silicon handle and it will be attached to an IC package for mechanical stability and heat conduction. Heat generated by circuits in tier 3 can be managed by including a back-metal layer to aid the extraction of heat through the tungsten plugs. This technique requires the deposition and definition of an additional metal layer, BM1, to contact the tungsten plugs, as shown in Fig. 6. The BM1 layer must be designed with a 660-nm surround with respect to 3DCUT in order to cover the tops of the tungsten plugs. Bond pads will be opened after definition of BM1.

<table>
<thead>
<tr>
<th>Tier</th>
<th>3DLAND</th>
<th>Doughnut</th>
<th>Tier</th>
</tr>
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<td>None</td>
<td>1</td>
</tr>
<tr>
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<td>2</td>
</tr>
<tr>
<td>3</td>
<td>None</td>
<td>Metal 3</td>
<td>3</td>
</tr>
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Table 1: Metal features associated with 3DCUT and 3DLAND layers required for 3D circuit integration

**Fig. 1:** The three tiers that will be integrated to form a 3D IC at the completion of conventional IC fabrication.

**Fig. 2:** Tier 2 aligned and bonded to tier 1 before removal of the handle silicon. The wafer bond is a low-temperature oxide bond.
Fig. 3: Tier 2 electrically connected to tier 1 with tungsten plugs after removal of the handle silicon, etching of 3D vias between the tiers, and deposition and planarization of tungsten.

Fig. 4: Tier 3 after it was aligned, transferred, and interconnected to the assembly shown in Fig. 3.

Fig. 5: The 3-tier assembly of Fig. 4 shown after bond pad etch and prior to testing the 3D circuit.
Fig. 6: Thickness stack for three-tier structure with an additional metal layer, BM1, used to contact the tungsten plugs to remove heat from tier 3.