Smart Dust: Large-Scale, Low- Power, Flexible Sensor Networks

A proposal to the Laboratory of Physical Sciences

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CONTENTS

1. Introduction

We propose to develop intelligent smart-dust networks for sensing and analyzing the local environment. Each dust particle will be a millimeter-size system that contains sensors, a micro-controller, a transceiver and a power source. An illustration of a dust particle is shown in Figure 1.1. The network can contain several hundreds or even thousands of dust particles. The dust particles sense physical attributes of the environment, and then communicate these attributes to other dust particles over wireless channels. Using distributed local-processing algorithms, the dust particles fuse their data, and make decisions based on the cumulative information of the overall network. The unique aspects of the network will be integration of novel communication and distributed fusion algorithms with physics-based designs, including MEMS technology, 3D integration and low power VLSI architectures.

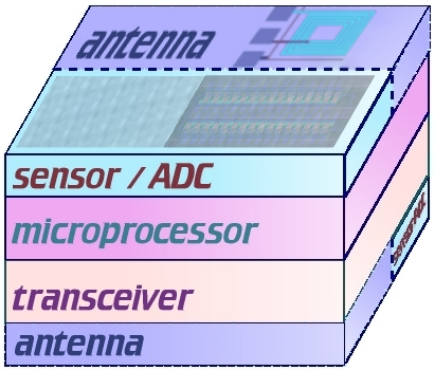


Figure 1.1. Dust Particle Illustration

There are many challenges that arise in designing such networks. Dust particles will be of small size, but must still house sufficient radio frequency and computational circuitry to operate effectively on low power. Dust particles will either be powered externally or by an internal power source that is commensurately sized with respect to the particle.

To allow reliable processing and fusion across the network, while making efficient use of the energy resources at each particle, we propose to consider energy-efficient short-range RF communication, sensing and processing at each node and develop *ad-hoc* networking algorithms for reliable communication and fusion. The network will exploit multiplexing of transmissions in time and frequency, by combining time-division multiple access (TDMA) with frequency-division multiple access (FDMA). We plan to have the network self-assemble whereby the multiple access slots are reused across the network with large enough reuse distances to avoid interference. As a result, each particle will communicate "within its cell" with a small number of dust particles, at a small number of operating frequencies, and a small number of time allocations. Information will be sensed and will then be fused with that of other particles to make network-wide decisions. The information will be communicated digitally using frequency shift keying (FSK) modulation. To develop this network, we have divided the tasks into six major categories:

- Radio Frequency CMOS VLSI Hardware
- Communication, Networking and Local Processing Algorithm Development for Energy-Efficient Fusion in Smart-Dust Networks
- Digital Design: Intra-Node Controller and Computational Components for Interfacing with RF Transceiver, Managing Network Protocols and Data Analysis
- Antenna Design
- Power: MEMS, Batteries, Capacitor Structures and Solar Cells
- Analog Sensing

We plan to develop the smart dust network in several phases.

- **Phase 1**: Develop a small scale (less than 20 nodes) smart dust prototype ad-hoc network using commercially off the shelf (COTS) parts. This network will be prototyped on PC boards, and be used to test basic communication algorithms, to set up the frequency and time divisions for the FDMA-TDMA multiplexing schemes, and to establish channel and source coding protocols. The test vehicle for this prototype network will be to first sense a local maximum (e.g., highest temperature or light intensity), and subsequently estimate the location of the local maximum and track its trajectory in time and space.
- **Phase 2**: Develop smart dust prototype network using chips designed by ourselves, and fabricated through MOSIS. Use a well-established process that is not economically prohibitive, and one that we already have experience with (either the 0.25μm or the 0.5 μm MOSIS). Start integrating ICs into 3D systems. Experiment with other sensors to detect chemical agents and vibrations. Continue to improve algorithms for power and noise tradeoffs, and investigate extensions of the techniques developed for phase one for networks of randomly placed particles.
- **Phase 3**: Develop state-of-the-art smart dust ad-hoc network using a 0.13 or 0.09 micron process. Scale the technology we developed in Phase 2 to lower dimensions that are commensurate with the higher frequency, low size, lower power 0.13μm or 0.09μm processes (whichever is more appropriate 18 months from now), and to larger scale networks.

2. Radio Frequency VLSI Hardware

2.1 Design Criteria:

The dust transceiver system will have to be low power, low noise, and have physical dimensions in the millimeter range. In addition, the transceiver must be relatively inexpensive to fabricate so that thousands can be deployed without prohibitive costs. The frequency of operation must be in the gigahertz range, so that commensurately sized antennas may be utilized. The design will need to accommodate the TDMA-FDMA multiplexing scheme using FSK modulation in order to establish the ad-hoc network described in Section 3 of this white paper. Also, the design should be well suited for 3D integration, which is a key technology we are developing with the LPS. Incorporation of 3D integration transcends the current state of the art, which mainly relies on 2D integration: this should facilitate the development of unique compact smart dust systems. The size, frequency, modulation, power, 3D integration and cost criteria all argue for the use of CMOS technology to develop and fabricate smart dust particles. In our background research, we have developed numerous RF chips and ICs for 3D integration. In addition, we have developed numerical models for analyzing the parasitic effects of EM cross talk and heat production in 3D IC's [1-6]. This background work also points to the use of CMOS technology for achieving 3D smart dust particles. With the constant reduction of feature size, CMOS transistors are operating well into the GHz range. Currently, IBM is offering its 0.13 micron CMOS-RF process through the MOSIS foundry. This process boasts a unity gain frequency f_T = 90GHz. The next generation, which is the 0.09 micron process, has already been made commercially available from UMC and is claimed to have an f_T = 160GHz. Over the next ten years, the Semiconductor Industry Association Roadmap indicates that gate lengths will continue to be reduced to below 0.035 microns, and

operating frequencies should increase at least linearly with gate length reduction. Such high frequency operation should allow for continued scaling of dust particles to sub millimeter dimensions. In addition, reduction in size also corresponds to commensurate reduction in supply voltages, and for various components of the system, a quadratic reduction in power.

2.2 Transceiver Topology:

The transceiver topology is shown in Fig. 2.1. The transceiver will be narrow band and will contain receiver and transmitter blocks. Initial designs will be centered to operate at carrier frequencies in the 10GHz range, spanning a bandwidth of approximately 20MHz. Noise levels at the input should be small enough so that receiving dust particles can detect signals which are at least as low as -100dBm. Precise values of these numbers will depend on the technology, power, noise levels, and the details of the TDMA-FDMA communication network we develop. The receiver hardware will consist of a low-noise amplifier (LNA), a mixer, an IF amplifier, and a local oscillator (PLL-frequency synthesizer). The transmitter will require a frequency synthesizer, a power amplifier and will share the PLL with the receiver.

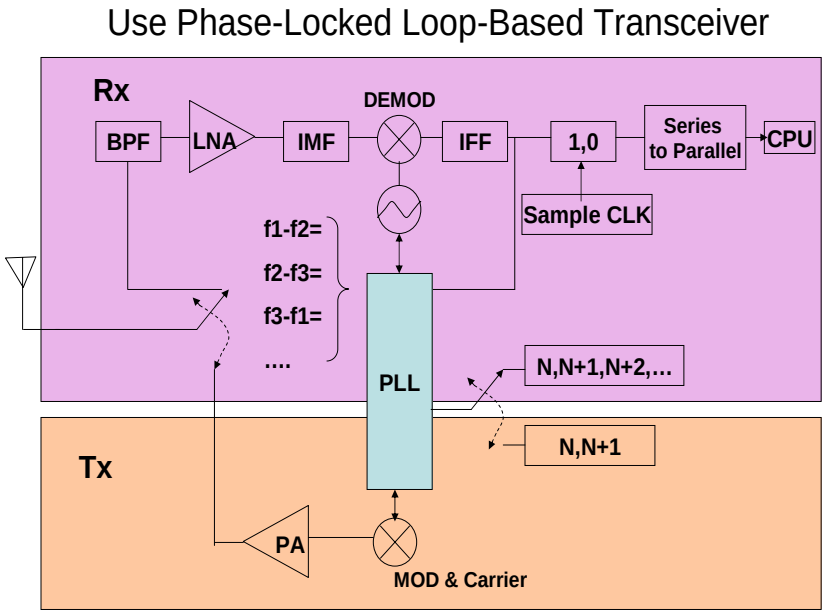


Figure 2.1. Transceiver Topology

- **Phase-Locked Loop**: The transceiver will be centered around a second order phase-locked loop topology. The PLL will be used for frequency synthesis required for both broadcasting and tuning. The PLL will be composed of a phase detector, filter, voltage-controlled oscillator (VCO), and a counter. The counter will be controlled by the microprocessor. Tuning in both the frequency (FDMA) and time (TDMA) domains will be electronic by interfacing the PLL with the microcontroller component of the dust system. The PLL will also serve as the demodulator for the FSK signal by reading corresponding voltage levels on the VCO. A PLL chip we designed in our background investigation is shown in Figure 2.2.

- **Low Noise Amplifer**: The RF receiver input will be a cascode low noise amplifier (LNA) designed to be impedance matched to the antenna, while at the same time providing approximately 20dB gain and simultaneously minimizing power consumption and noise. This constraint of minimizing power and noise simultaneously will be a research challenge. Generally, noise decreases when transconductance increases. However, supply current also increases with higher transconductance. We will optimize our smart dust system so that for the given communication algorithms as discussed in Section 3, we will optimize the noise/power tradeoff. Use of minimum supply voltages will be explored which should help to minimize power without compromising noise performance.

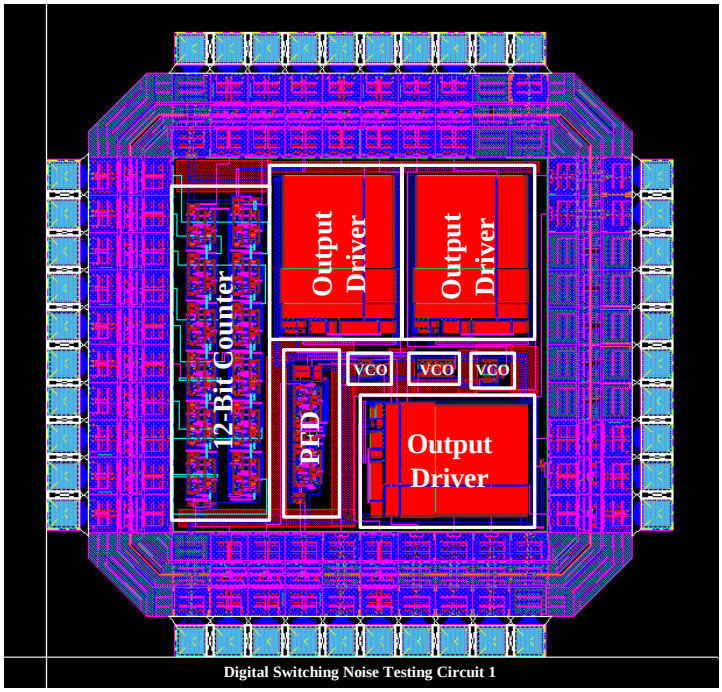


Figure 2.2: PLL Chip Designed for FSK Modulation

- **Mixer**: The initial mixer will be of the Gilbert-cell type, with accommodations made for maximizing swing at low DC bias levels. The PLL will serve as the local oscillator. The mixer will mainly serve as a down-converter to the intermediate frequency (IF). Other mixer topologies will be explored in an effort to minimize supply voltage levels.
- **Power Amplifier:** We will investigate the use of switch-mode type transmitter power amplifiers (PA) in order to maximize power efficiency. A switch mode amplifier theoretically can achieve 100% efficiency because the current and voltage are opposite in phase. Since the development of switch-mode amplifiers require use of passive components, 3D integration should facilitate their application. We plan to operate at the highest frequencies allowable by our active devices. This will facilitate minimizing the size of the passive components, especially antenna, inductor and capacitor structures.
- **Passive Structures (Inductors, Capacitors and Antennas):** Passive components will present a challenge with respect to size constraints. Inductors will be in the nanohenry range, while capacitors will be in the tenth (0.1) picofarad range. 3D integration should be a great asset in fabricating these passive components because the added volume will greatly facilitate fabrication of these elements while at the same time minimizing their resistive parasitic elements which reduce the quality factor. Specific antenna designs are described in Section 5 of the paper, however, the added layers of 3D integration should allow for more efficient antennas and better optimized radiation patterns. We also plan to expand our background on carbon nanotubes [7] to examine their use as inductors. Our background

investigation indicates that CNTs may exhibit very large kinetic inductance, and require a small volume, thereby saving considerable IC real estate.

3. Communication Protocols, Networking and Algorithm Development: Energy-Efficient Algorithms for Integrated Networking and Fusion

In this project we will develop implement and optimize energy-efficient algorithms for data processing, communication, and networking that allow computation of fusion tasks in large networks of randomly distributed sensors. Although our sensor prototypes will be initially limited to sensing temperature or light intensity information, the fusion algorithms we will develop and implement, can be employed, in principle, to perform fusion tasks that arise in a broad range of applications. These include weather forecasting, detection and monitoring of chemical and biological agents, and surveillance tasks, such as target detection, localization and tracking. In particular, the fusion objectives of interest in this project comprise:

- distributed algorithms for computing global statistics of the measurements collected across the network, such as maxima and averages;
- methods for event detection, classification, and localization, such as detection of measurements exceeding a threshold, and localization and tracking of threshold exceeding events;
- algorithms for localized post-detection processing and tracking, such as computation of localized statistics and localized event tracking.

Several important constraints invariably arise in designing resource-efficient physical- and network-layer communication algorithms for performing fusion tasks over the large networks of randomly distributed sensors that we plan to deploy. Limitations in sensor battery power and computing resources place tight constraints in the rate and form of information that can be exchanged among sensors and the type of on-sensor processing that can be performed. Equally important, changes in the network topology and size, due to node mobility, node failures and battery outage, make global knowledge of the changing network topology impractical. As a result, ad-hoc networking and decentralized approaches to fusion are becoming increasingly preferable over their hierarchical centralized counterparts for such large sensor networks.

3.1 Ad-hoc Networking and Fusion

The ad-hoc networking algorithms we propose to develop will provide short-range communication nodes with the capability to communicate and fuse information across large networks. In particular, based on its limited transmit power, each dust particle will be able to establish direct bidirectional communication with a small subset of neighboring nodes (e.g., nodes within an 1-10 m radius) and will thus be aware of (the IDs of) a small subset of communicating nodes.

Performing local processing and fusion prior to relaying data across a smart-dust network can provide substantial data compression savings and as a result, savings in both power and bandwidth usage. A promising approach to performing distributed fusion involves viewing each node in the network as a local fusion host and developing integrated routing/fusion algorithms such that the

fusion objectives are eventually made available to every node in the network. In its most basic form, ad-hoc networking amounts to localized routing algorithms allowing data from any single node to reach a subset of designated receiver (or in principle, all) nodes for future interrogation. More generally, the integrated networking/fusion algorithms we plan to implement will allow for event detection, localization, and tracking and are described in the following sections.

Distributed Computation of Global Maxima and Averages

The localized processing and fusion algorithms we propose to implement and optimize will allow distributed computation of global and local statistics in the measurements, such as global maxima and weighted averages of the sensor data. These algorithms are locally constructed at each node, i.e., they only require that each node be aware of the subset of neighboring nodes with which it can establish bidirectional communication. They are also inherently distributed, scalable and fault tolerant, and can allow substantial savings in communication bandwidth and power usage through local data processing and fusion prior to retransmitting information over the network.

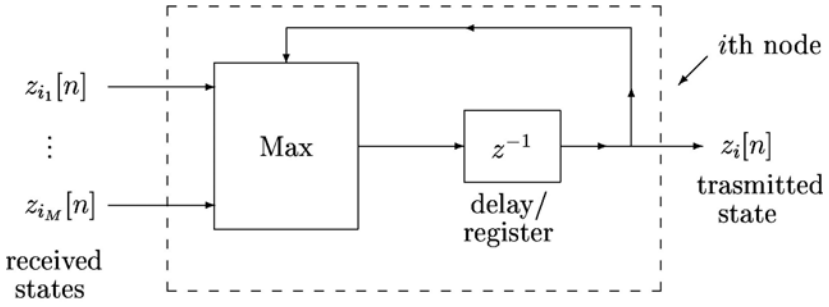


Figure 3.1: Local processing at the *i*th node yielding the global maximum

The simplest task that illustrates the benefits of local fusion involves the computation of the highest temperature (global maximum) among the sensed temperatures. The local fusion rule at a given node is shown in Fig. 3.1, and sets its new local-maximum estimate as the maximum of all the estimates transmitted by neighboring nodes and the node's own local estimate. Simulations, assuming uniformly distributed sensor data, in an ad-hoc network of 10,000 randomly distributed nodes with approx. 10 neighbors/node, and whereby each node broadcasts only improvements in its local estimate, reveal that on average less than 8 state transmissions/node are required until every node in the network obtains the global maximum. Furthermore, the average number of transmissions per node (and thus average energy usage) required for global convergence can be significantly reduced at the expense of delays, if nodes broadcast improved local maxima only a fraction of the time.

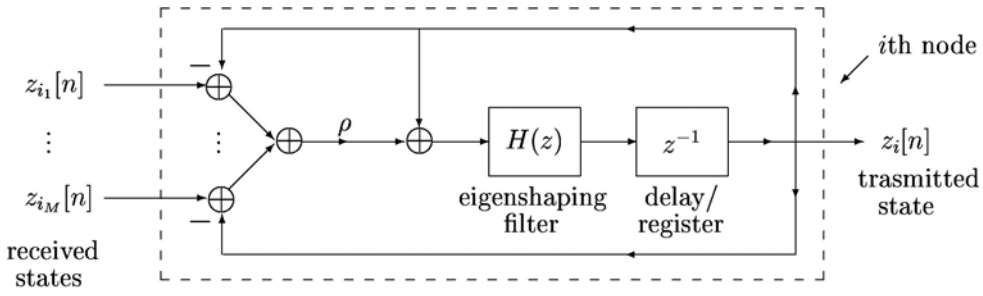


Figure 3.2: Local Processing at the i[th] node yielding the global average

Distributed implementations of the majority of fusion rules (including linear fusion rules) are not, in general, as straightforward, as the global network topology is not locally available at individual nodes. For instance, local averaging of the available states at each node, yields local sequences of estimates that in general do not converge to the global average, but rather to a weighted average that depends on the (unknown) global network topology. In [10] we developed methods for local processing and fusion that allow distributed computation of various global computations, over ad-hoc networks with arbitrary topology, including weighted averages of functions of the node data. These low-complexity local-processing rules are shown in Fig. 3.2, and can be locally constructed and optimized to provide at each node fast-converging approximations to the desired global computation. Fig. 3.3 shows the convergence rates to the global average for a typical network of 400 nodes for various such fusion rules. As the figure shows, the rule corresponding to the steepest curve requires less than 20 local communication and fusion steps to obtain an estimate of the average with 0.1% (−30dB) relative squared-error distortion. We plan to leverage our experience in this area and in developing optimized DSP implementations [20], to implement, test, and optimize these fusion algorithms over the networks we plan to deploy, initially employing tens, and perhaps hundreds of dust particles. We also plan to exploit the fact that these locally constructed algorithms are readily scalable, in order to investigate the trade-offs between processing/communication power, and fusion quality in larger-scale networks involving thousands of nodes.

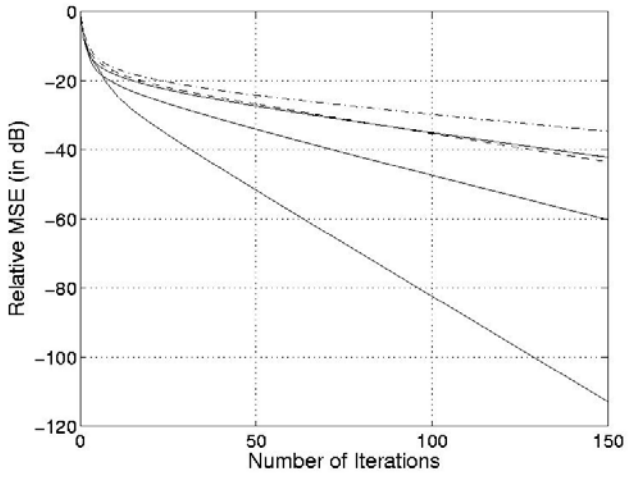


Figure 3.3: Convergence rates of local processing rules for computing averages

The algorithms in [10] can be employed to perform more complex fusion tasks, which can be decomposed into sets of weighted average computations of local function of the sensor data. These include a number of surveillance tasks, such as target detection by majority voting, and target localization. For instance, in [11], we employ these algorithms for distributed target localization via an ad-hoc network of acoustic sensors, whereby each node knows its own location and has measurements that provide relative-range information between the node and the target. In the early stages of this project, involving small-size networks with particles placed in known predetermined locations, we plan to leverage of prior experience with distributed source localization from range-measurement information [11], to develop implement and optimize distributed triangulation algorithms for sensor-location aided event localization and tracking.

Sensor Location Estimation via Networking

The minimum number of hops required to communicate between any two nodes in the network provides a coarse estimate of the relative distance between the two nodes. By combining such relative range information between a node and several properly distributed nodes with known locations it is possible to obtain an estimate of the position of the node. This approach to position estimation is attractive in dense networks, since the minimum number of hops required for communication between any two nodes can be obtained via localized broadcasting and routing. In its simplest form, it involves one of the nodes serving as the source that broadcasts a counter-type message, which will provide the minimum number of hops information when it reaches its destination. In particular, the message is sequentially propagated throughout the network by receiving nodes by locally updating (incrementing by 1) the minimum-number-of-hops counter message and rebroadcasting, until the message reaches the destination node. Fig. 3.4. depicts the localization performance of this method for a network of 5,000 nodes. The node in the center of the blue circle has detected an event, while the 8 circles in the periphery denote reference nodes with (locally) known positions. A single broadcasted message by the detecting node allows each of the reference nodes to obtain range information from the detecting node that can then be used to estimate its location via distributed source localization [11]. The blue circle in the figure denotes the localization error range of this method, which, for this network, is of the same order as the range of a single-hop transmission. We plan to investigate and optimize such coarse sensor location estimators that are based on the minimum number of hops and additional locally available information (e.g., received signal strength in single-hop transmissions), and analyze their

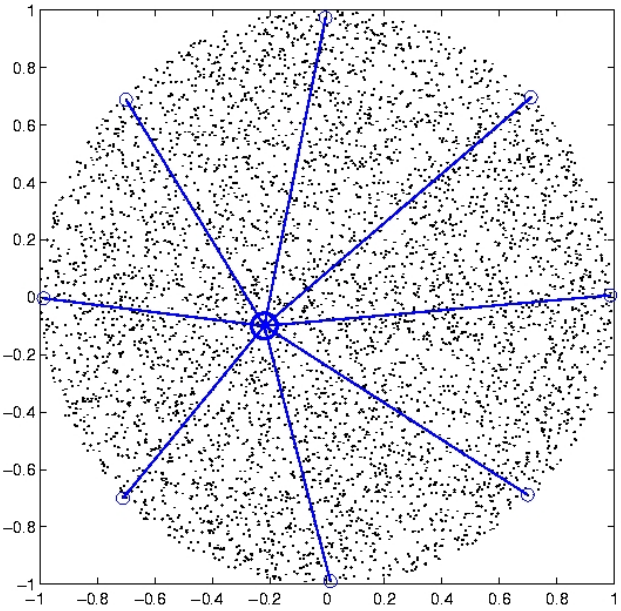


Figure 3.4: Ad-hoc network aided coarse node localization in dense smart dust network

localization performance characteristics as a function of the network node-density and size, the broadcasting range, and the number and location of reference nodes used for triangulation.

Localized Averages and Localized Tracking

At later stages of the project, we plan to focus on methods for performing localized fusion tasks, whereby only a (potentially time-varying) subset of nodes close to the event of interest have relevant measurements for fusion. Our approach consists of methods for distributed localized detection and localization, followed by localized tracking via a properly adapted subset of detecting nodes. In this context we plan to leverage our prior experience [12] involving methods for distributed computation of fusion tasks based on data from only a subset of the nodes in the network, by exploiting the whole network topology. These algorithms are very attractive in the context of tracking and surveillance, as only a subset of the whole set of nodes in the network (those close to the source) have information-bearing measurements, yet, it is in general advantageous (both in terms of power usage and computation delays) to employ the whole network for the computation [12].

3.2 Resource-efficient Point-to-Point Communication

The point-to-point communication algorithms will allow measurements and data to be reliably communicated over a given link while making efficient use of energy (and bandwidth) resources. Transmitter and receiver block diagrams are shown in Figs. 3.5 and 3.6 and comprise the following subsystems:

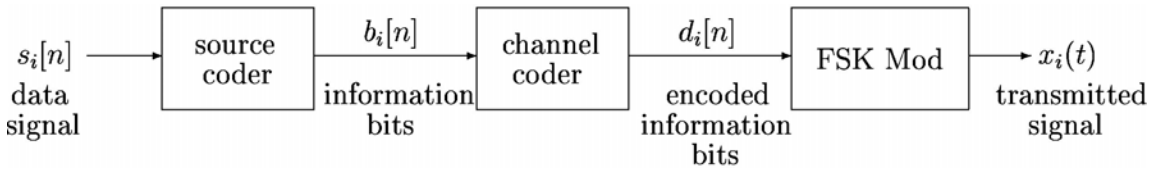


Figure 3.5: Transmitter for communicating a sequence of data or measurements

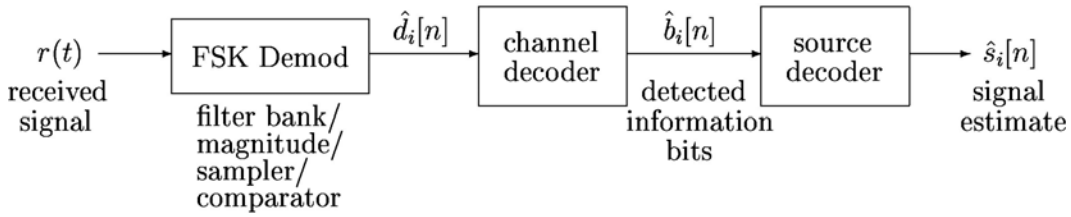


Figure 3.6: Receiver comprising FSK demodulation followed by channel and source decoding

- **Source coding (transmitter) and source decoding (receiver) algorithms**: The source coder compresses the data/measurements that are to be communicated into a sequence of

information bits that are communicated over the channel instead. These algorithms perform signal compression in amplitude and time in order to eliminate redundancy from the data to be communicated. We will leverage our prior experience with low-complexity source encoding algorithms ([8, 9]) in order to implement energy-efficient systems for encoding and communicating the analog measurements in digital form over the wireless channel.

- **Channel coding (transmitter) and decoding (receiver) algorithms**: The error-correcting encoder inserts controlled redundancy into the information bit stream in order to communicate it over the wireless channel to a receiving node at desired fidelity levels. The error-correcting codes we plan to employ are known as rate-compatible punctured convolutional (RCPC) codes [13]. Their advantages are their low encoding and decoding complexity, and the fact that by design they can readily provide different levels of error protection to different information bits, thereby exploiting the fact that the signal distortion due to an error at the receiver strongly depends on the information carried by the erroneously detected information bit. Channel coding also allows for noise resistant operation at decreased receiver power levels of the receiver circuits.
- **Modulation algorithms**: As described in the transceiver design section, the channel-coded information bits are relayed from the microcontroller to the RF circuitry and are communicated over the wireless channel via frequency-shift keying (FSK), at a preassigned carrier frequency. The FSK carrier frequency range will be in the order of 10GHz in our original designs, and may reach 50 GHz at later stages.

3.3 Multiple-Access Protocols

Taking into account the inherent limitations in the RF hardware and the need for ad-hoc networking, we will employ TDMA-FDMA protocols, according to which user transmissions are multiplexed in both time and frequency. According to the protocol, each dust particle periodically communicates with closely located nodes only at preassigned time slots via FSK at a preassigned carrier frequency, and can receive on a single carrier frequency during any non-transmitting time slot. The use of FDMA (as opposed to CDMA) is motivated by the presence of sufficient bandwidth, allowing orthogonal (multiuser-interference free) communication among neighboring nodes. The need for multiple-access in time (TDMA) is motivated by limitations in the transceiver circuitry (dictating that a node can only receive at a single carrier frequency at any given time) and allows each node to receive transmissions from multiple neighboring nodes during any given time frame.

Protocol Assignment

Due to the nature of ad-hoc networking, there is a need for methods for spatial reuse and reallocation of time-frequency slots so as to avoid interference between transmitting nodes. In the initial network prototype, involving fixed sensor placement, the time-frequency slots will be preallocated (and will remain fixed) so as to avoid interference. In the context of random node placement, we will leverage our prior experience with evolutionary algorithms and directed graph theory [14] to generate time-frequency slot assignments so as to avoid interference. Congestions that may inevitably eventually arise due to the time-varying aspects of the network topology can be alleviated by having sensors with interfering transmissions locally readjust their time-frequency slots in order to avoid interference. As an example, in a network of randomly placed sensors,

whereby each node communicates on average with 10 other neighboring nodes within its range (e.g., an area around the node of 10m radius), and a frequency reuse factor of 3 (corresponding to no interference from all nodes outside an area of 60m radius), a 10×20 FDMA-TDMA slot allocation protocol more than suffices to obtain non-interfering transmissions. We remark that, as bandwidth efficiency is not as important as efficient battery-power use, congestions can be always alleviated at the expense of network computation rates (and thus delays in fusion), by increasing the number of TDMA slots in a frame. This approach is also attractive for generating an initial operational network configuration in networks of randomly dispersed dust particles. Indeed, using an FDMA-TDMA allocation table with a large enough number of time-access slots allows the nodes to self-organize and obtain an initial locally constructed multiple-access slot allocation, which can be used to obtain the network topology. The techniques described in Sec. 4.2 [14] can then exploit such network topology information to obtain new more efficient multiple access allocations, involving FDMA-TDMA tables with shorter time frames, thereby obtaining networks with optimized computation rates.

3.4 Optimal Estimation and Management of Random Sensor Networks

The technical objective for this part of the project is the development and demonstration of algorithms for the scheduling and control of sensor networks containing multiple smart dust sensor subsystems (including subtypes). This is critical technology in a smart dust sensor application where there could be tens, hundreds, or thousands of individual sensor elements. The aggregate signal processing will have to "multiplex" the individual sensor signals, and emphasize those with the "highest payoff" (for example, those sensors processing the signals with the greatest uncertainty).

The technical framework we use for sensor management and control will be based on distributed optimization and data fusion. By associating "costs" (including power, signal processing effort, etc.) with the operation and switching of the individual sensors, the sensor systems operations management problem will be formulated mathematically as a stochastic optimal switching control problem. This permits the use of classical mathematical methods (quasi-variational inequalities) to compute real-time strategies for the management of the sensor network.

The key task here will be to develop algorithms for the management and control of sensor networks using limited distributed computing and communications strategies. The work complements the sensor fusion algorithms discussed above. Benefits of this work include real-time feedback strategies for sensor management and data fusion.

The sensor scheduling problem can be posed and "solved" using a version of stochastic dynamic programming. The optimal control law, that is, the algorithm that defines which set of sensors to use at which time, is defined by a set of variational-inequalities; and these in turn are solved by "switching" and "continuation" sets. Essentially, if the estimated state is in a continuation subset, then it is optimal to continue observing with the current sensor suite. The boundaries between the continuation sets are switching sets. When the state encounters a switching set, it is optimal to switch to a new configuration, incurring the switching cost. In the Figure 3.4 we show an example from a sensor scheduling application [17]. In this example, a multimode sensor is being used to measure two different types of signals – say position and velocity. At any given time, the

sensor can either measure signal 1 or signal 2 or take no measurement. The first trace is a plot of the absolute value of the estimation error of signal 1 (a Gauss-Markov process) when observed by the sensor in mode 1, using Kalman filtering algorithm to produce the state estimate. The second trace is the absolute estimation error for the second signal when the sensor is in mode 2. The final trace is the optimal sensor schedule for this case, taking into account the estimation errors and the cost of applying the sensor. The costs p1 and p2 of using each mode of the sensor differ in this example, and the numbers of individual sensor activations differ accordingly. The more expensive sensor is used less often.

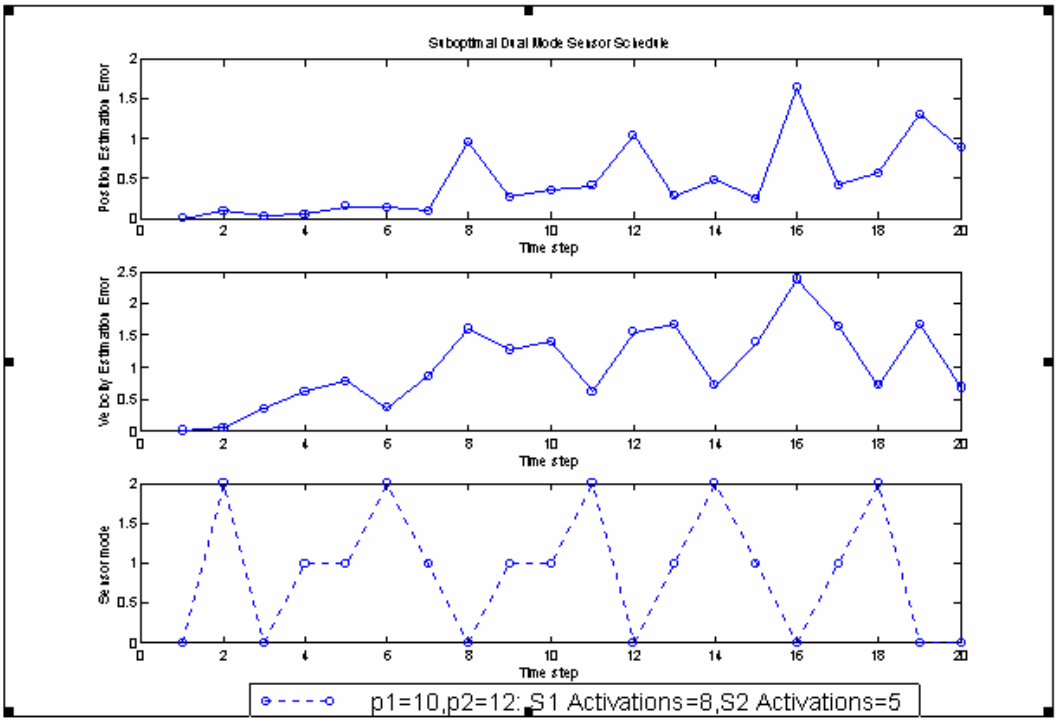


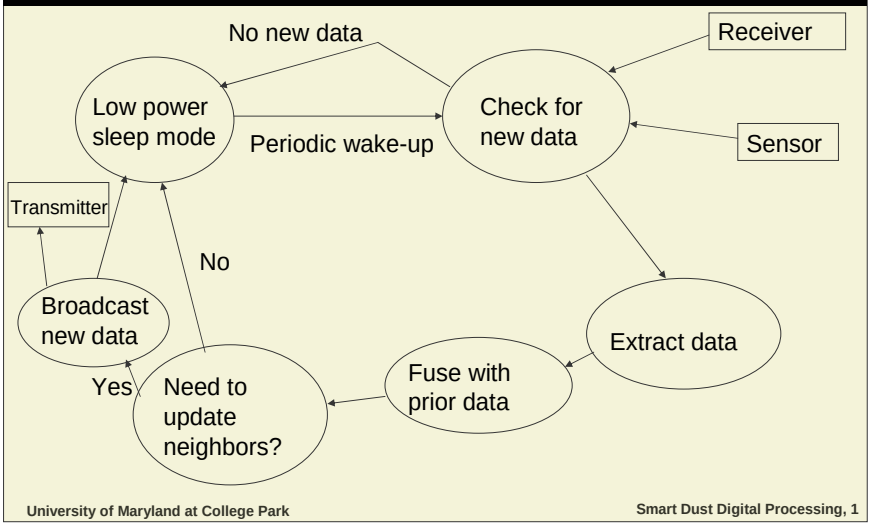
Figure 3.4: Sample sensor schedule for a multimode sensor

This theory of random sensor control for optimal estimation has been treated as a mathematical problem in [15] and [16]. In this part of the project we shall develop computational algorithms for the solution of this problem in specific cases - e.g., multiple random sensors including modal vibration detectors, accelerometers, etc. for rotating machinery. This work will be based on our research in other projects [17].

4. Digital System Design: Intra-Node Control and Computational Components for Interfacing with RF Transceiver, Managing Network Protocols and Data Analysis

The digital subsystem is responsible for control and data processing of a smart dust node, as illustrated in Figure 4.1. This requires close monitoring and control of transceiver circuitry. For example, the digital subsystem will set the counter value of the PLL based on the next channel on which reception will be monitored, carry out reception on this frequency for a pre-specified length of time, extract and examine the quality of the received data, and extend the duration of reception as necessary until the data on the channel is adequately received. The digital controller will repeat this sequence of steps for each active channel during each period of data collection. During transmission, the digital controller will determine what, if any, data needs to be transmitted; carry out the low complexity source and channel coding algorithms described in Section 3.2; and activate the transmitter with transmission frequency and duration based on the TDMA-FDMA protocols of the network.

Figure 4.1. An illustration of the structure of core digital system functionality.



4.1 Digital Controller Design

In our initial prototype, the digital processing engine will be a low power microcontroller, which will integrate lightweight operating system functionality for monitoring and adaptation of node behavior with the data processing tasks to be performed at each node. Use of a low power programmable processor will enable exploration of more complex algorithms for sensor fusion, experimentation with different algorithms and protocols, and run-time adaptation of node behavior, and will provide access to important energy consumption features such as processor shutdown modes and dynamic voltage scaling. Research issues in the design and implementation of the digital processing platform include efficient integration with the radio subsystem, and the mapping of the desired processing algorithms and protocols into energy efficient and highly memory constrained implementations. For this latter task, we will build on our extensive experience in developing transformations for efficient and compact embedded software implementations (e.g., see [20][21]). Our work will involve modeling of the desired smart dust processing in terms of formal models of computation, such as dataflow graphs and finite state

machines, and graph theoretic analysis of these models to map them into the constraints imposed by the restricted processing architecture.

One specific family of candidates for use as the microcontroller in our initial prototype is the Texas Instruments MSP430 family of "ultra-low-power" microcontrollers. Components in this family offer high programmability with active-mode power consumption below 500 microwatts when operating near the lower limit of their voltage range. In addition, these components provide integrated A/D and D/A converters, and processor shutdown modes in which power consumption is reduced to amounts as low as a few tenths of a microwatt during idle periods. Experimentation with microcontrollers such as these in our initial prototype will focus our digital design techniques on the performance and memory constraints that are critical to achieving the desired levels of miniaturization and low power consumption. It will also provide baseline implementations that provide reference points for our future efforts at size/power reduction and 3D integration.

In parallel with development of our initial prototype, we will explore three directions for achieving the high miniaturization and 3-D integration capabilities that will be targeted by our subsequent prototype designs. After a preliminary exploration in which the potential costs and benefits of all three directions are carefully estimated, we will select one of these directions to focus on for the development of our second prototype. Our first direction of exploration will involve developing our own streamlined implementation of the off-the-shelf microcontroller used in the initial prototype. The objective of this implementation will be to maintain at least some of the programmability of the original microcontroller component, but achieve 3D integration capability and significant reductions in power consumption by designing and implementing the integrated circuit ourselves. Mechanisms for power reduction in the implementation will center around removal of unnecessary or underutilized processor features (e.g., instructions, memory capacity, and addressing modes), and careful application of hardware/software co-design [22] to migrate critical functionality into custom hardware implementation. By designing for compatibility with the original microcontroller specification (or a carefully-selected subset of it), we will be able to leverage the compilers, assemblers, and other software development tools that accompany it.

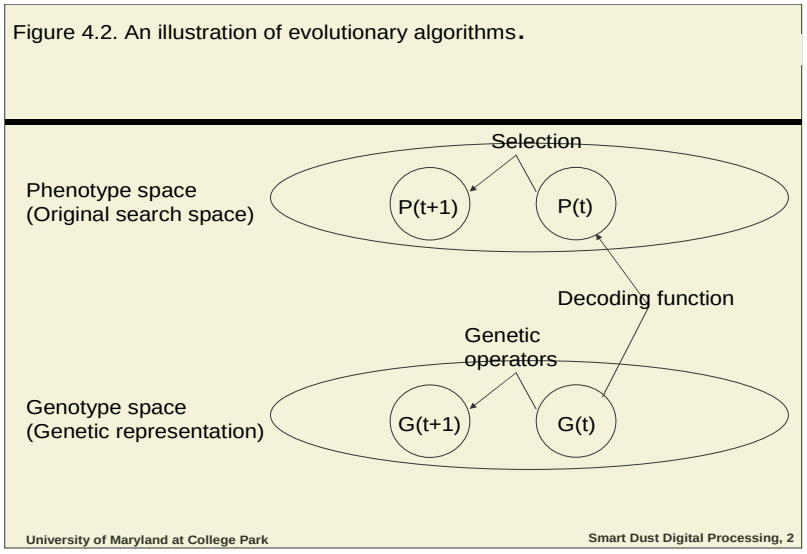
Our second direction of exploration for digital system design will be replacing the microcontroller component with an application-specific integrated circuit (ASIC) that employs dedicated circuitry for all functions. The ASIC will be carefully designed to support the complete digital system functionality for a specific smart dust application, with a specific set of communication protocols. Unlike a microcontroller-based design, this approach will not provide flexibility in accommodating changes in application or communication functionality (without re-fabrication). However, due to its specialization, we can expect significant streamlining of size and power consumption. Extensive use of low power digital system and logic design techniques will be employed. Such techniques include clock gating, controlling input signals to functional modules so that they change only when the module results are needed, arithmetic strength reduction (e.g., replacing multipliers with shift or shift-and-add modules), and reduction of switching activity at the integrated circuit pins. A modular architectural and hardware description language (HDL) design style will be employed so that supported features (e.g., data processing functions or communication protocols) can be easily reconfigured from one integrated circuit implementation to the next, thereby mitigating some of the decreased flexibility as compared to the microcontroller-based design.

Third, we will consider the possibility of licensing the commercial intellectual property (IP) core that underlies the original microcontroller, and using that core for 3D integration in our second-generation prototype. This approach will allow us to leverage state of the art, commercial low power microcontroller technology, and allow us to focus more of our digital system design effort on system-level configuration optimization, as described in more detail below. This possibility is highly speculative at this point, however, because the manufacturer of the microcontroller may not permit such licensing (especially for a low volume research prototype), and because, even if licensing is permitted, the cost is anticipated to be extremely high.

4.2 Network Configuration

Several issues must also be addressed in configuring the smart dust network. These include setting up handshaking protocols and low complexity source-channel coding and decoding, integrating with the transceiver to establish PLL timing, assigning transmission power, and assigning processing tasks to network nodes. The parameters underlying these setup issues form a complex design space, whose efficient exploration will lead to significant power savings.

For example, streamlining the energy efficiency of processing in the smart dust network will require careful balancing of computation and communication across the network nodes. For this purpose, we will explore techniques for strategically assigning sensing and processing tasks to network nodes so that effective trade-offs are achieved across computational accuracy, processing energy consumption, and communication energy consumption. This will involve developing quantitative models of communication and processing energy consumption throughout the network, and modeling the overall network's processing algorithms as task graphs, where graph vertices represent sensing/processing tasks and connections between vertices represent data dependencies (communication requirements) between tasks. We will explore algorithms to systematically embed these task graphs into the sensor network based on the energy consumption constraints predicted by the energy consumption models. This embedding will determine which task graph computations are assigned to which network nodes, and which subset of network nodes is kept idle (turned off).



Similarly, for the assumed TDMA/FDMA communications protocol, the assignment of time/frequency slots to network nodes can be performed strategically to optimize the computation rate of the network, and this assignment may be adapted periodically based on the network state and channel conditions. This problem is discussed further in Section 3.3.

To address such system-level optimization issues, we will explore the use of evolutionary algorithms, which provide a probabilistic search methodology for complex, non-linear optimization problems. In this work, we will leverage our previous experience in architecting evolutionary algorithms for embedded software optimization [14]. An illustration of the general framework of evolutionary algorithms is shown in Figure 4.2. Candidate solutions to an optimization problem are encoded as binary strings based on a "genetic representation" function. This "population" of binary strings is then adapted probabilistically through operations such as "recombination" (combining attributes from two existing binary strings to form a new binary string) and "mutation" (making small perturbations to an existing binary string). As these adaptations occur, the modified population is filtered with a strong bias toward retaining those binary strings that correspond to the most effective candidate solutions. This process of probabilistic adaptation and filtering continues through numerous iterations, and the best candidate solution in the resulting final population is chosen as the output. When the key evolutionary algorithm building blocks, such as the genetic representation, recombination and mutation operations, and filtering mechanism, are designed well, evolutionary algorithms have been shown to be effective across a wide variety of complex optimization problems (e.g., see [23]).

5. Milli and Micro Antennas

Establishing an effective communication link between the dust particles requires electrically and physically small antennas that should be capable of meeting the power requirements of the system. Providing that the antenna size profile (size profile is defined as the radius of the smallest sphere that completely encloses the antenna) should be smaller than 5mm, we propose several antenna topologies that address two primary concerns: The antenna radiation resistance, which is a direct measure of the power gain of the antenna, and the directive gain, or radiation pattern. We assume that the dust particles will be distributed in a plane and therefore the radiation pattern of the identical antennas will be uniform in the polar angle and negligible radiation in the azimuth. Since the dust particles are positioned randomly, maximizing the directive gain in a certain direction will not be useful. Initially, we will assume vertical (with respect to the ground) polarization.

The antennas proposed here are all mounted on a perfectly conducting platform. Antennas mounted on finite size planes provide alternative designs, however, as a proof of concept, we start with infinite perfectly conducting planes to minimize antenna simulation time. We assume that at the early stages the frequency of operation will be f=10GHz. In later stages, where the frequency will increase, say to 50GHz, the antenna electrical and radiation characteristics will remain unchanged provided that all antenna dimensions are scaled uniformly.

5.1 Power Calculations for Simple Dipole Antenna

Simple calculations can be made to determine the minimum power requirements for a communication link between two antennas separated by a distance r. For simplicity, we will assume that the two antennas are positioned such that the transfer of power between them is maximum. This includes polarization and directivity (maximum directive gain). Let P_T be the total power transmitted, P_R be the total received power, then according to the Friis Transmission Formula:

$$P_R = P_T \frac{A_{em}^T A_{em}^R}{r^2 \lambda^2}$$

where r is the distance between the two antennas, and A_{em}^T and A_{em}^R are the maximum aperture area of the transmitting and receiving antennas respectively. The aperture area is expressed as

$$A_{en}^T = \frac{V_{rms}^2}{4R_r S_{av}}$$

where V_{rms} is the voltage at the input terminals of the antenna, S_{av} is the average power density, and R_r is the radiation resistance of the antenna. What is important to note here is that the aperture area is inversely proportional to the radiation resistance.

In light of the severe size constraints placed on the antenna, an electrically small antenna (ESA) will be used. An ESA typically has dimensions $kr < 1$, where k is the wave-vector. There are several antenna shapes types that can be used. The simplest ones are the dipole antenna or the monopole antenna.

For a short (non-ideal) dipole, the radiation resistance, R_r is given by

$$R_r = 20\pi^2 \left(\frac{l}{\lambda} \right)^2 ,$$

and the maximum effective aperture is given by $0.48\lambda^2$. Substituting in the Friis formula, and assuming identical transmit and receive antennas placed to maximize power coupling, we have

$$P_T = P_R \frac{r^2}{0.23\lambda^2}$$

As an example, under optimal matching and polarization conditions, and assuming that the received power should be greater or equal to -100 dBm (0.1 picoWatts), then according to the formula above, if an electrically short dipole antenna is used, we can have the following minimum power requirements:

For antenna separation of 1m, $(P_R)_{\min}$ = 0.482 nanoWatts
For antenna separation of 10m, $(P_R)_{\min}$ = 48.2 nanoWatts

In light of the fact that the aperture area is inversely proportional to the radiation resistance, it is expected that any increase in the radiation resistance (as offered by the alternate designs discussed below) would lead to lower power transmission requirements to achieve -100dBm.

It should be kept in mind, however, that the short dipole antenna has low radiation resistance which needs to be matched to the feed line, and a capacitance which needs to be tuned either by an inductor or a transmission line stub that is connected in parallel with the feed. We also remark that the transmission line stub need not be stretched but can be meandered to reduce profile.

5.2 Inductively-Coupled Small Antennas

Aside from the dipole antenna, the most desirable type of antenna is the patch antenna which offers low cost, high reliability, and minimal physical profile. The microstrip patch antenna becomes resonant when one of its dimensions is approximately equal to one half the wavelength. For an operating frequency of 10GHz, the wavelength is 3cm which requires the smallest dimension of the patch antenna to be approximately 1.5cm. Since the microstrip antenna is inherently a very inefficient radiator, the antenna cannot be used effectively when its length is decreased below the half wavelength mark.

Different antenna configurations can be considered, however, all of these configurations are electrically small in the sense that $kr < 1$. For a monopole operating at 10 GHz, and restricting the height of the antenna and radius to 5mm and 0.1mm respectively, the input impedance of the antenna is approximately

$$Z_{in} = R_{in} + jX_{in} = 30 - j\,100$$

The short monopole antenna presents the simplest possible design configuration. More efficient, yet non-intuitive designs can be adopted that are based on using genetic type optimization algorithms that search for specific optimal antenna characteristics under specified constraints. Two antennas that will be discussed here have been obtained based on previous designs that were optimized.

The first antenna considered will be referred to as Antenna A, shown in Fig. 5.1. This antenna consists of a shorted feed line inductively coupled to a meander antenna. The inductive feed counter balances the inherent capacitive reactance of small antennas, and the meander geometry extends the length of the antenna while maintaining small overall electric volume. The antenna radiation pattern is shown in Fig. 5.2. (Ansoft HFSS was used for all the simulation results presented here.) Note that the power is skewed towards one direction due primarily to the asymmetric feed geometry. This imbalance in the power distribution can be corrected by providing a symmetric inductive feed topology. The antenna return loss is shown in Fig. 5.3, and the input impedance, presented in Fig. 5.4, shows that this antenna does need tuning and its radiation resistance is very close to 50 Ohms, thus providing excellent power match potential.

The second antenna, antenna B, shown in Fig. 5.5, builds upon the same concept of inductive coupling discussed above. However, unlike antenna A, the shorted element in antenna B is pushed further from the ground plane. This change provides a better directionality as shown in Fig. 5.6.

Antennas A and B provide a much improved radiation resistance over the dipole antenna, while eliminating the need for tuning which can reduce the overall efficiency of the antenna-feed system.

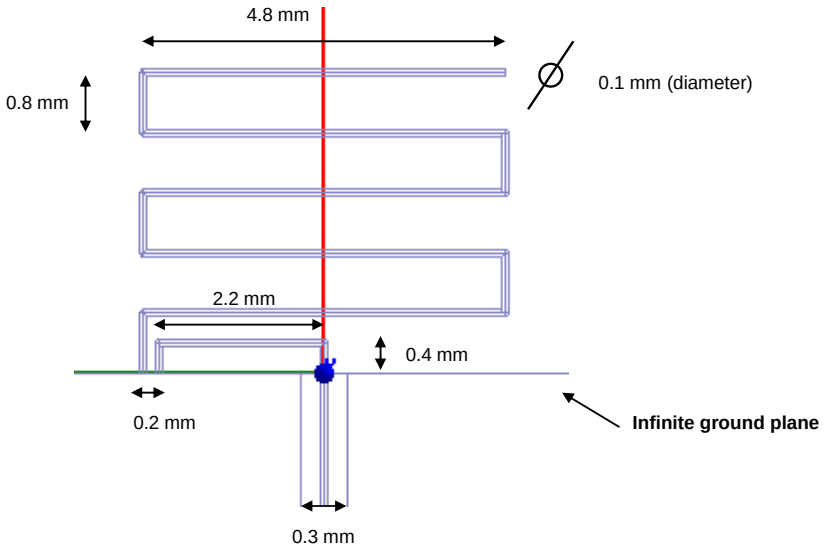


Fig. 5.1. Antenna A.

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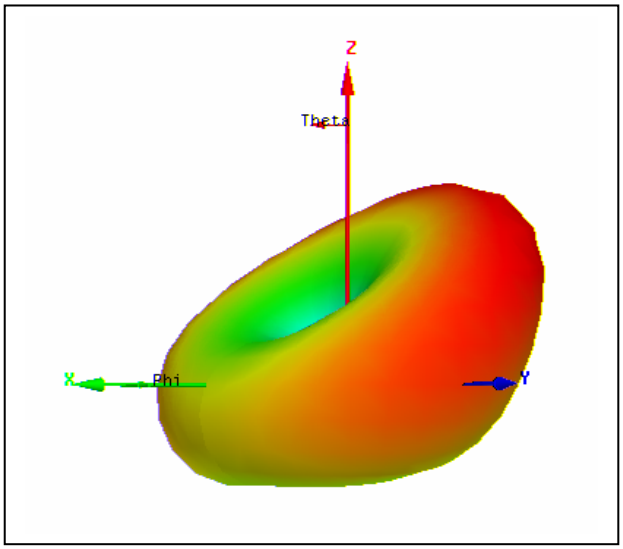

Figure 5.2: Radiation pattern of antenna A

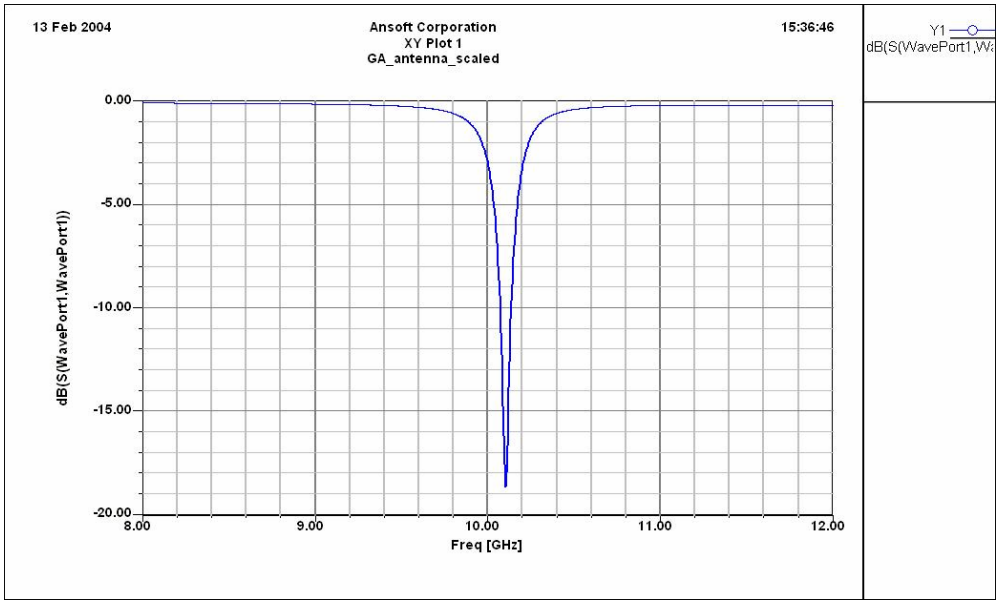

Fig. 5.3. Return loss (S_{11}) of antenna A.

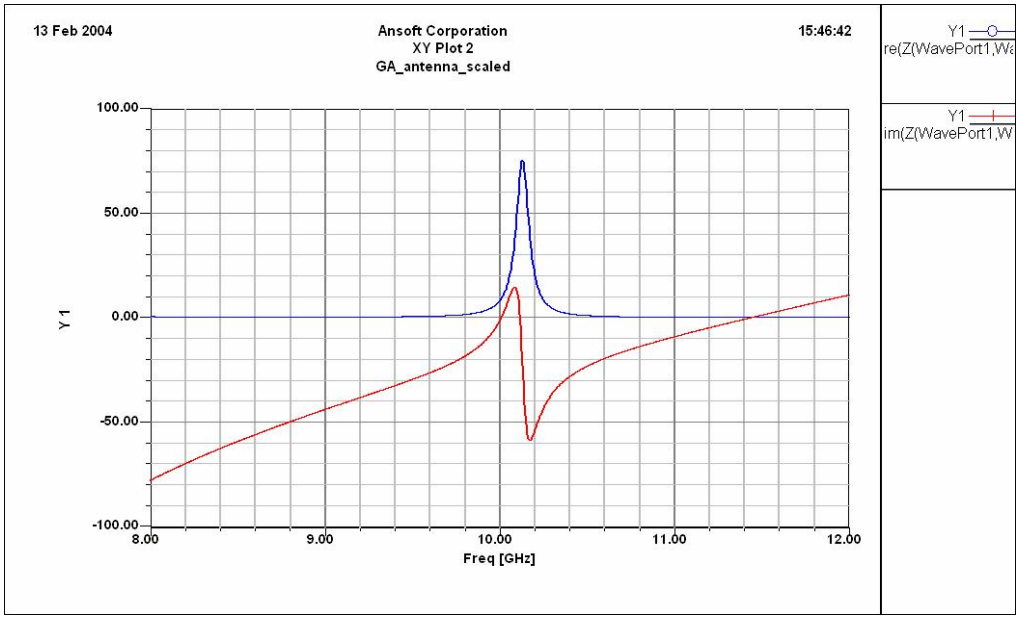

Fig. 5.4. Input impedance (resistance: Blue, Reactance: Red) of antenna A.

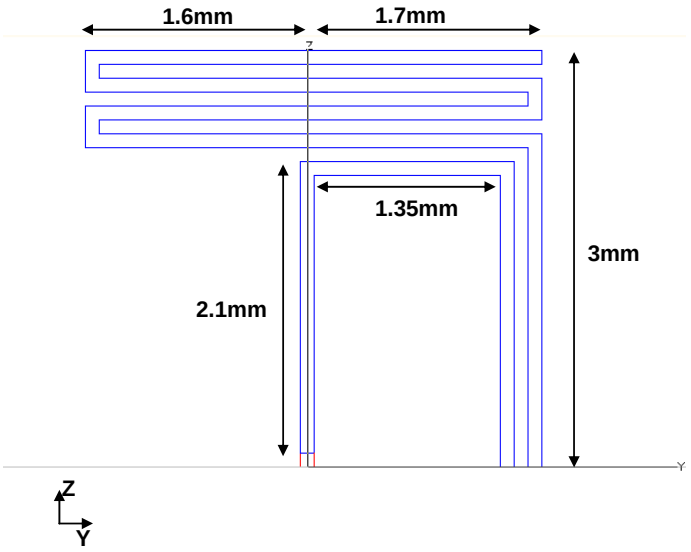

Fig. 5.5. Antenna B.

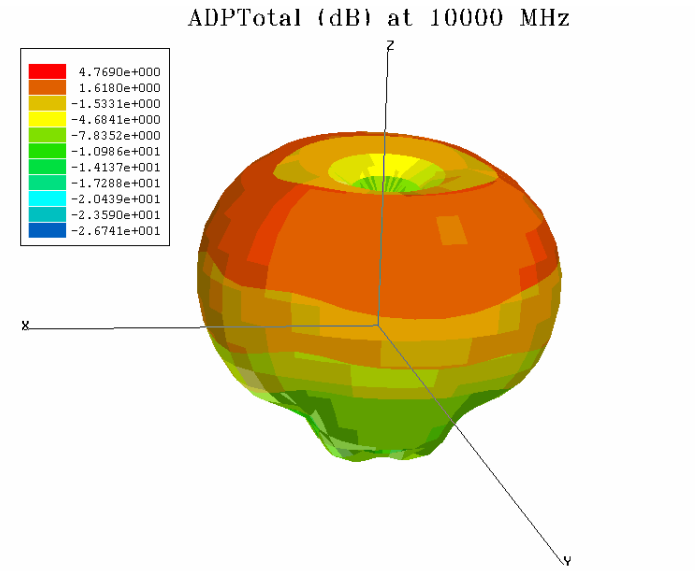

Fig. 5.6. Radiation pattern of antenna B.

5.3 Future Work and Objectives on Antenna Design and Implementation

We emphasize here that the antennas discussed above were not optimized for directivity, radiation resistance and bandwidth. We propose to use genetic algorithms coupled with the Alternate-Direct Implicit Finite-Difference Time-Domain (ADI-FDTD) method to search for more effective topologies[2,3,5]. The ADI-FDTD is an excellent algorithm for simulating structures with wide variance in resolution and can effectively predict the Ohmic losses in the conductors and in the substrate. These losses are expected to rise with the increase in operating frequency, leading to changes in the overall efficiency of the antenna. We plan to investigate volume-based curve-filling

antennas and the hemispherical monopole above perfectly conducting ground plane. A detailed listing of the objectives is given below.

- Development of a full-wave three-dimensional ADI-FDTD algorithm that comprehensively simulate the antennas and the platform. The algorithm will be capable to address structures with wide variation in geometrical resolution while maintaining very efficient run time.
- Adaptation of our genetic optimization algorithm to the antenna problem.
- Application of genetic-based and non-genetic-based optimization algorithm to the antenna problem.
- Feed design for maximum power transfer.
- Matching network design for maximum power transfer.
- Development of space-filling antennas.
- Incorporating electromagnetic band gap material to maximize gain for antennas operating in the 30-50GHz region.
- Antenna fabrication using microlithography and MOSIS.
- Antenna testing for power gain and radiation characteristics.
- Integration of antennas with RF transceiver circuitry for both planar and 3D integrated circuits.

6. Sensors

6.1 MEMS-based Sensors

We plan to design and prototype integrated sensors that include acoustic, visual, and thermal (IR) detectors. These sensors will operate on several levels: (a) Individual integrated sensor chips will be able to process their own data and make independent decisions. (b) The individual multi-modal sensors ICs will be networked to enable decisions based on information provided by the network as a whole. The individual sensing elements will be based largely in CMOS and MEMS technologies:

- Optical sensors will consist of CMOS focal plane arrays;
- The vibration sensor will be constructed of a MEMS-based microphone.

Each sensor will be associated with the necessary electronics to transform the associated output to an electrical signal that can eventually be processed and disseminated over a wireless network. Where possible, the sensors, mixed signal electronics, including analog front-end and RF components, and the digital processing, will be contained on a single chip. More details of individual sensor elements and associated electronics are described below.

Acoustic Sensor

Our vibration and acoustic sensor will utilize a MEMS-based microphone. Due to the high performance standards applied to microphones in communication applications, careful design, characterization and design optimization are needed for development of a sensitive micromachined acoustic device. Today's MEMS-based microphones are divided into four categories: dynamic, condenser, electret, and piezoelectric. Most previous micromachined microphone work has focused on condenser designs because of their sensitivity and compatibility with thin film fabrication techniques. We plan to build on these past experiences and results in order to

incorporate the electronics and the sensors into a single, self-contained "System-on-a-Chip" in the most robust and efficient way and therefore, we plan on designing silicon condenser microphones with on-chip CMOS circuitry using MOSIS for the fabrication of both CMOS and MEMS components. This work is motivated based on the work reported by Bernstein et al. from the Draper Laboratory at the Solid-State Sensors and Actuators Workshop in 1996. They reported a monolithic silicon microphone with on-chip JFET buffer amplifiers with a sensitivity of -50 dB and a bandwidth of 20 kHz. The device consists of the perforated bridge electrodes on top of 1mm diaphragm (see Figure 6.1) which utilized both surface and bulk micromachining techniques. This is a prime example of a MEMS-based microphone device that uses only batch microfabrication techniques for its development. However, the important optimization issues involve the changes in diaphragm compliance, area, gap and damping. Focused Ion Beam (FIB) is a powerful fabrication technology that allows the investigation of both the development and optimization of a MEMS-based microphone device without requiring extra lithography, deposition and etching steps. We will be using FIB for this purpose in order to enhance and optimize the operation of our devices.

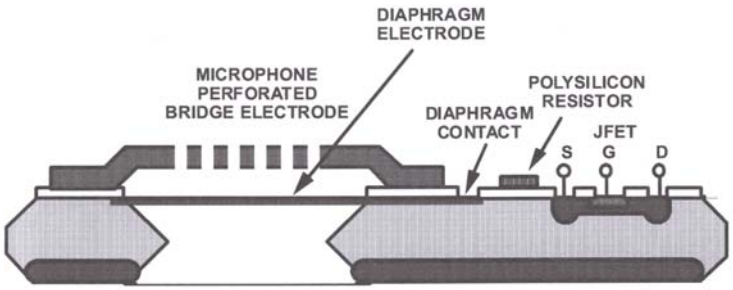

Figure 6.1. Schematic of a condenser microphone with on-chip circuitry (Bernstein et. al. 1996)

Optical Sensor

We plan to employ CMOS active pixel technology to develop the optical image sensor. We will begin with standard designs that are realizable using the MOSIS facility. This design consists of a photodiode, which is connected to a simple CMOS amplifier circuit within a single pixel element. The amplified photo-signal is thereby activated to provide higher contrast relative to neighboring pixels. We plan to go beyond standard designs to perform signal processing directly at the pixel level. More specifically, we plan to map the pixel array directly onto a numerical grid where computations, such as differentiation, can be directly performed. By performing the signal processing directly at the pixel level, we will be able to facilitate packing more computational power into a single integrated sensor system IC. Using device modeling, at later stages we also hope to design our own photodiodes that are specifically optimized for the optical sensing tasks that will be required.

Chemical Sensor

Chemical "nose" chips are currently available commercially. Cyrano Scientific (http://cyranosciences.com/products/Nosechip.html) markets a stand-alone chip, which is less than 0.5cm on a side capable of sensing a variety of pathogens and toxic materials. The chip is an array of resistors made of a graphite-impregnated polymer. Graphite makes the polymer matrix conductive. The polymer backbone is decorated with pendant groups that bind with target analytes. When these analytes are bound, the polymer swells, separating the graphite particles, reducing conductivity. We plan to investigate the use of this sensor in our initial COTS designs.

7. Power

Providing adequate power to smart dust particles will be a challenge. Power can come from internal batteries, or by harvesting external energy. Harvested energy may come from a variety of sources, including solar energy, wind, as well as microwave radiation beamed into the area.

7.1 Power Requirements

The power requirements of a smart dust particle depend on many factors. These include the distance to broadcast between particles; the number of different particles we want to establish communication with; the type of data communicated; the noise levels that can be tolerated; amount of processing power necessary to the specific task. We expect the power required by each dust particle to be in the area of several milliwatts for one of our preliminary generations of chips which we expect to fabricate with the 0.18micron process. This number is largely governed by tradeoff between noise and power in the transceiver, the power required to broadcast EM radiation, and power required for digital algorithm implementation: Below we summarize average results of numerous power calculations we performed for the dust particles operating under a bias of approximately 1V and a carrier frequency of 10GHz.

- LNA: 1mW (Relatively large power required to overcome noise constraints)
- TI MSO430 Microcontroller: 1mW
- PLL: 0.1mW
- Power Amp and Transceiver Broadcast Antenna 0.2mW

The total energy needed by the network will depend on the time required to sense communicate and fuse data. We expect to have data rates in the kbits/sec range. For the small and intermediate-size networks we plan to deploy, these data rates translate to requiring system times on the order of fractions of a second to seconds to collect and fuse data, and will thus require on the order of 10 mWseconds or 0.003mWh of energy to complete a fusion task over the network. Below we describe a tiny battery that stores 300 times that energy in a 2mm size volume. A major goal of this research will be to optimize our designs with respect to power use. Our objective will be to reduce the power requirement below 1 mW per dust paricle. We will explore use of lower supply voltages, actively switching circuit polarities to reduce supply rails. folded cascode circuit topologies, maximum noise thresholds, use of new materials for passive devices (e.g. carbon nanotubes), application specific communication schemes and digital processors for minimizing power.

7.2 Power Sources

There are numerous power sources that are currently being investigated for small size applications. We have compiled a data base which is on the web (http://www.enee.umd.edu/~neil/micropower/). In addition, we expect to pursue the following options.

- **Batteries**: In the early stages of the project, we plan to employ tiny COTS batteries to power our smart dust particles. The first group of batteries will be the size 5-type. They are approximately 5mm x 2mm in size and can provide 35mAh of energy at 1.4V. This power will be more than adequate for our initial smart dust particles, and these batteries are readily available for a few dollars. We also plan to experiment with a new battery that has been

developed by TPL Inc. This battery is reported to be 3mm in diameter, and can provide 1mAh of energy at 1V. Use of these two batteries will allow us to make consistent progress on the dust system while new methods for providing dust power are being developed. In particular, we have developed several initial designs for harvesting energy, which are described next.

- **Solar Cells**: We plan to investigate the use of solar cells for providing power to smart dust particles. On average one square centimeter of sunlight corresponds to 100mW of incident power. As current solar cells are approximately %10 efficient, a one square millimeter solar cell can deliver approximately 0.1mW of power on an average sunny day. As solar cell are mainly special forms of PN junctions, the first stage of our investigation will be to determine if reasonable-quality solar cells can be produced through the MOSIS process, thereby providing a platform for readily integrating these solar cells into our IC development. We remark that solar cells obviously have limitations in providing a steady source of power to smart dust particles, especially for use at night, indoors, and inclement weather.

- **EM Rectennas**: Energy beamed from EM sources sweeping an ad hoc array may be stored in capacitors. The EM radiation will be received by our circuit antenna, passed through a rectifying diode, and then stored as separated charge on a capacitor. The input impedance to the radiation will be sufficiently large so as to develop a high enough voltage to forward bias the rectifying diode. The storage capacitors must have enormous plate surface areas in order to retain significant amounts of energy. “Corrugation” processes, in which high density arrays of posts are fabricated, have been used routinely in dynamic random access memory (DRAM) circuits. A set of micron-square posts ten microns high on two micron centers can be fabricated using today’s dry etch technology. Such structures, shown in Figure 7.1, exhibit a factor 20 increase in effective surface area. Also, recent research in high-k dielectrics has produced commercially available metallorganic chemical vapor deposition (MOCVD) systems that deposit continuous films of tantalum pentoxide 7.5 nm thick. Such films have a dielectric constant of 25. A silicon square 1mm on a side, fabricated in such a way, creates a 100 microfarad capacitor. These wafers can be pre-scribed into chips and thinned to 50 micron thicknesses. Ten of these structures can easily be stacked (head to tail) to form a 1000microfarad capacitor. A one volt bias can provide a storage charge of .001 coulomb on this structure, resulting in a half a millijoule of stored energy. In this configuration, such a capacitor can source a milliwatt for 500 milliseconds. This can provide power to active elements in the ad-hoc network between refresh times (from microwave beam sources). The evolutionary path here is to make dielectric-k higher and make deeper trenches. The insulator thickness may also be scaled to produce milliwatts to provide power to millimeter scale dust particles. The rectenna and capacitor concepts are illustrated in Figures 7.1 and 7.2.

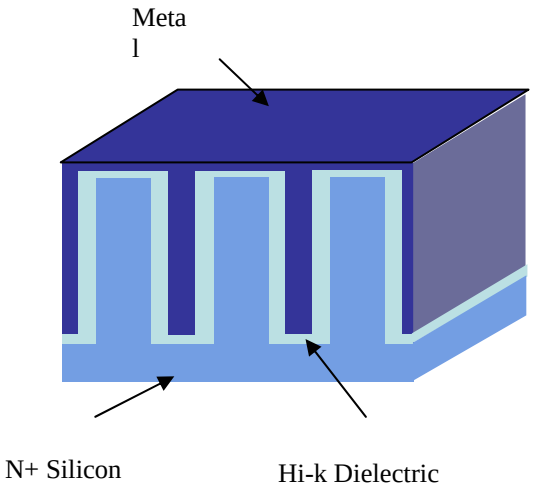

Figure 7.1: Cross section of high density micro capacitor to be used by rectenna.

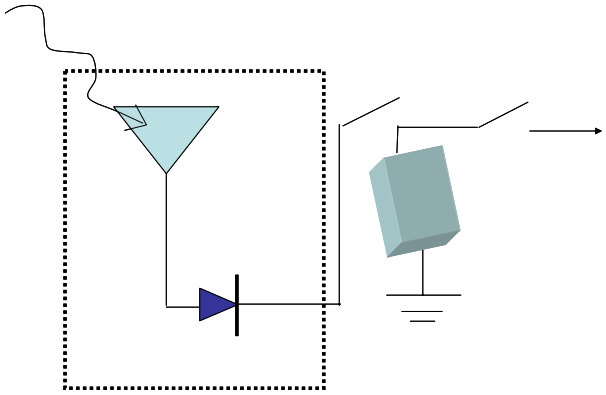

Figure 7.2 Illustration of rectenna. (antenna, diode, charging capacitor bank)

7.3 MEMS Power

- **MEMS Batteries**: Currently, research is also underway to develop microscale MEMS batteries. These are batteries that use 3D stacking and the hope is that they can produce significantly more power than the standard planar type batteries that are currently used. Current stability appears to be a major obstacle in the development of these batteries, however, if we regulate these batteries with current sources, we are should be able to transform them into a stable power source.

MEMS-Based Power Harvesting: We are proposing a to investigate a MEMS approach to extracting mechanical power directly from the environment.

- Inertial Power Generation: allowing electronic devices to act as parasites on moving bodies, enabling power generation through movement of directional micromotor drives (e.g. attaching a device to an ambulatory human).
- Thermal Energy Transfer: using large external thermal gradients to energize electronic components (e.g. placing a device on an engine block).
- Environmental Stimuli Extraction: using continuous source phenomena in the localized environment to generate power (e.g. placing a microturbine or “windmill” in a HVAC system or in the path of a PC cooling fan).

Our research group in the MEMS Sensors and Actuators Lab (MSAL) at the University of Maryland is in a unique position to address and investigate the integrative materials, fabrication, and technology approaches needed to develop high performance, reliable, robust integrated MEMS devices suitable for micropower generation[24-30]:

- **Microtribology** [28]: A non-contact method has been developed to study the frictional dynamic behavior of interacting micro-machined surfaces. The results of this study can be

directly used to achieve an optimum design for microball-bearing mechanism of a micromotor. This method will increase the efficiency of any generator by minimizing internal friction.

- **3-D Silicon Fabrication Technology** [25]: Using gray-scale-mask method, a technique is being developed to fabricate 3-D structures in silicon with arbitrary angles. This new technology can be applied to realize an optimum design for the bearing mechanism. This originates from the capability of this method in fabricating arbitrary angles through which linear and circular v-grooves with different angles are feasible. A kind of prototype "windmill" structure is currently well in development in our laboratory, is shown Figure 7.5.
- **Integration of Dielectric Material Processes and Bulk Micromachining** [29]: The requirement for reliability makes it necessary to avoid high temperature processes in developing microstructures. Spin-on dielectrics (such as BCB-based polymers) as planarizers and inter-layer dielectrics have simple low-temperature processes and can replace traditional methods of multi-level interconnect that usually include high temperature processes, which induce stress on microstructures. We are developing methods to integrate these new IC technologies with conventional bulk micromachining processes such as KOH anisotropic etching of silicon to allow the fabrication of MEMS sensors and power devices on top of existing circuit stacks.
- **Characterization of Dielectrics** [30]: We have developed testing methodologies, fabrication techniques and sophisticated instrumentations in our group to characterize the electrical properties (dielectric constant, breakdown voltage, and leakage current) of spin-on polymers as inter-level dielectrics. The results of this study will be used used to optimize the design parameters for the development of a microgenerator.

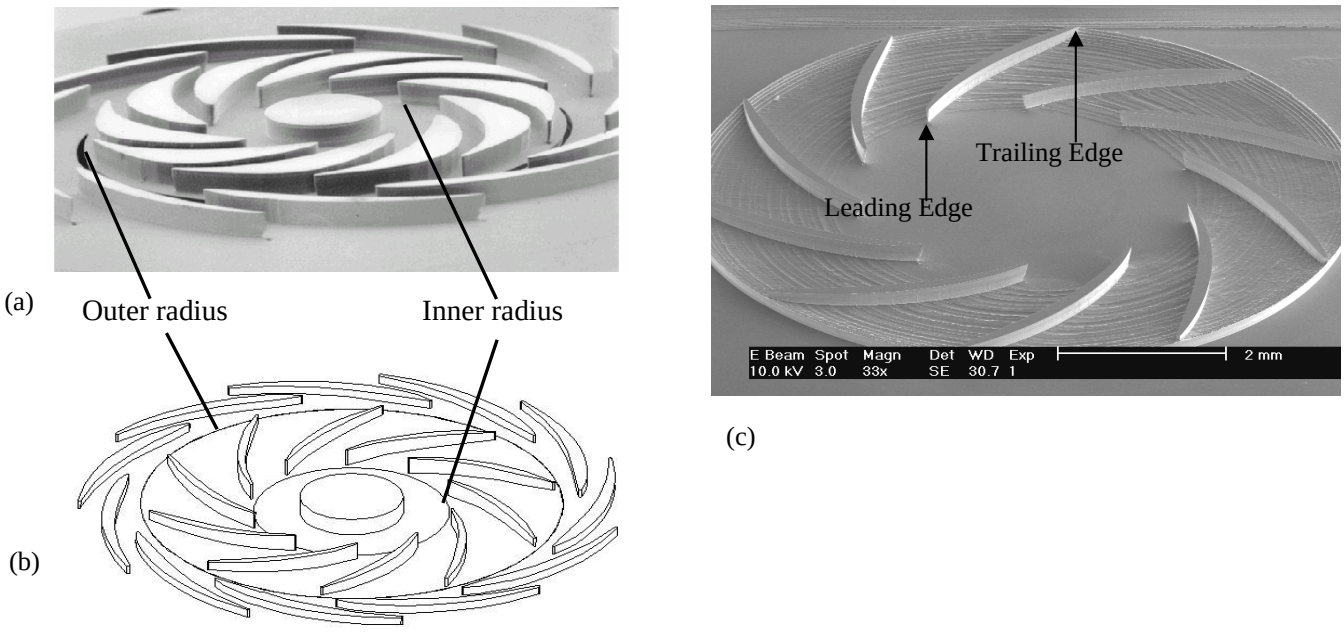

Figure 7.5. (a) An SEM image shows a compressor rotor for the MIT micro turbine engine fabricated by planar techniques. (b) A schematic of a rotor shows the preferred taper going from a 200 μm etch depth on the outer radius to a 400 μm etch depth on the inner radius. (c) Variable height micro-compressor in silicon showing the leading edge etched 350 m and the trailing edge etched 140 m.

8. Milestones

6-month milestones:

- Simulation of the smart dust network that computes highest sensed measurement (global maximum) and provides elementary operations, such as node-mode control (turn on and sleep mode) and node querying.
- Simulation and preliminary implementation of digital processing algorithms using microcontroller development platform.
- Make significant progress in prototyping PC board based small smart dust system. Begin designing our own chips for smart dust aimed at 0.5μm process.

12-month milestones:

- Optimization of the source-coding and channel-coding algorithms for energy-efficient communication and local fusion. Study of the trade offs between energy efficiency sensor density and computation quality.
- Complete implementation, testing, and integration of digital processing engine and embedded software for first prototype.
- Optimize design, fabricate and test basic antenna structures. Upgrade ADI-FDTD code to model antenna details. Link antenna structures with RF circuits.
- Complete PC board based system. Use system to test protocols and fusion. Send 0.5μm or (0.25μm) chips out for fabrication. Investigate low power topologies (folded designs and switched polarity)
- Design the circuits and layouts of vibration and optical sensors.
- Design and model the microgenerator in detail; design and implement test equipment.

24-month milestones:

- Simulation of sensor-location aided localized routing algorithms for energy-efficient event-detection and event localization in networks with predetermined node placement. Coarse event-range estimation in networks of randomly placed nodes based on the minimum number of hops from the event location.
- System architecture design and simulation for second-generation (3D integrated) prototype of digital processing engine. Evolutionary algorithm formulation of optimizing network configuration.
- Begin looking at improved antenna structures based on genetic algorithms. Scale antennas for higher frequencies.
- Test our own chips. Make multi-chip module from working chips. Begin 3D integration of chips and antenna. Continue investigation of low-power circuit topologies.
- Fabricate of vibration and optical sensors through MOSIS; test fabricated chips.
- Design and implement the microgenerator power electronics and control; design the fabrication process flow.

36-month milestones:

- Dust particle position estimation based on routing length and distributed triangulation in large networks of randomly placed sensors. Event detection, and event localization in large networks of randomly placed nodes.
- Complete low power implementation, testing and 3D integration of digital processing system for second-generation prototype. Complete implementation of evolutionary algorithm and integrate optimization results into system prototype.
- Fabricate and measure antennas that are based on genetic and non-genetic based algorithms. Scale antennas for higher frequency operation.
- Fabricate the microgenerator components.
- Obtain working smart dust system integrated into 3D. Start scaling down system to redesign and fabricate with advanced 0.13μm or 0.09μm CMOS technologies.
- Test the microgenerator components; optimize the design and fabrication process.

48 month milestones

- Extend digital subsystem with libraries and reconfiguration capabilities for design flexibility and multi-mode operation. Power/performance modeling of system prototype and integration of modeling into evolutionary optimization framework.
- Obtain working system using advanced CMOS. Begin implementing for 3D integration.
- Continue optimizing hardware design

60-month milestones

- Integrated optimized networks for (RF circuitry and microcontroller) energy-efficient event detection, localization, and tracking in large networks of randomly distributed sensors. Distributed network sectoring, sector-based event detection, localization, and tracking based on a dynamically updated detecting subnetwork.
- Design and implement the microgenerator mechanical drive mechanism; integrate into the system.
- Develop state-of-art 3D millimeter scale smart dust system.

9. Statement of Work and Personnel

1. The overall project will be organized and managed by Neil Goldsman. His responsibility will be to ensure the various sub-projects are well coordinated and very well integrated into a synergistic effort. Babis Papadopoulos will assist Neil in this effort to help ensure that the communication, digital design and signal processing end of the program is well integrated. Biweekly meetings will be held to facilitate this process. This will require the equivalents of 0.5 months' summer salary for Goldsman and Papadopoulos
2. The RF VLSI part of this proposal will be headed by Neil Goldsman. This will require 2 graduate students, approximately 115K in fabrication costs, technical support and 1.5 months of summer faculty salary.

3. The communication network and sensor management part of the project will be lead by Babis Papadopoulos with the aid of Gil Blankenship. We foresee this part of the project requiring 3 graduate students and 2.5 months of equivalent faculty salary.
4. Digital Design will be lead by Shuvra Bhattacharyya, which we expect to require 2 graduate students and 1 month of equivalent faculty summer salary. Costs will cover micro controller programming and ASIC design.
5. Antenna design will be directed by Omar Ramahi with help from Neil Goldsman, for which we are recommending 1 student, 1 month equivalent faculty summer salary and 10K fabrication costs.
6. Sensors will be directed by Martin Peckerar, with help from Reza Ghodssi and Neil Goldsman. We expect this to require 1 month summer faculty salary, two graduate students as well as technical support.
7. Power will be directed by Reza Ghodssi, with help from Martin Peckerar and Neil Goldsman. We expect to support this effort at the level of two graduate students and 1 month summer equivalent salary. We also expect fabrication costs on the level of 75k, as well as the technical support.

Personnel

1. Neil Goldsman (Prof. ECE Dept.) PhD Cornell University , Analog and RF Communication VLSI, Device Physics
2. Haralabos (Babis) Papadopoulos (Assist. Prof. ECE Dept.) PhD MIT, Communications and Signal Processing
3. Shuvra Bhattacharyya (Assoc. Prof. ECE Dept) PhD UC Berkeley, Digital Design and Signal Processing
4. Omar Ramahi (Assist. Prof. ME and ECE Depts.) PhD. University of Illinois, Electromagnetics
5. Reza Ghodssi (Assist. Prof. ECE Dept.) PhD University of Wisconsin, MEMS
6. Martin Peckerar (Prof. ECE) PhD University of Maryland, Analog Circuits, Material Processing and Device Physics
7. Gilmer Blankenship (Prof. ECE) PhD MIT, Control, Communication and Signal Processing.

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11. Facilities

- Anechoic chamber for electromagnetic testing (chamber size: 25 ft x 10 ft)
- Low-to-High frequency source generator (45MHz to 27GHz)
- Electromagnetic spectrum analyzer (45MHz to 26GHz
- State-of-the-art Vector Network Analyzer (45MHz to 50GHz) with highly accurate 2.4mm test set
- High-frequency precision spherical dipole for shielding and calibration
- 4GHz and 600MHz oscilloscopes
- PC board milling machine
- Dielectric probe
- Antennas and assorted high-precision probes
- Access to micro-fabrication facilities at the University of Maryland at College Park

The ***MEMS Sensors and Actuators Lab (MSAL)*** (http://www.ece.umd.edu/MEMS/) at UMD, directed by Professor Ghodssi, was established in January 2000. A variety of MEMS-based

processing tools are currently fully functional in the class-100 microfabrication room at MSAL that include a brand new Quintel model Q4000-6 contact mask aligner with precision front-to-back alignment capability for lithography, a P-1 Tencor profilometer, a temperature-controlled silicon micromachining bath, a Samdri–795 supercritical CO_2 dryer, a polymer-processing station with programmable spinner, a Lindberg 1200C box furnace, and an electroplating bath. MSAL also houses a number of testing and instrumentation equipment that include a Veeco NT1100 model optical profilometer with both static and dynamic measurement capabilities (nano to micron level) for both MEMS and NEMS devices, a MEMS-based probe station with a high power microscope, two class-100 characterization stations, and a state-of-the-art Nikon digital camera and a Leica stereomicroscope. In addition, simulation and modeling software (MEMCAD, FlumeCAD, ANSYS, L-edit, FemLab and AutoCAD) are installed on fourteen SUN and DELL workstations in MSAL for design and analysis of MEMS devices and systems.

The lithography step of our MEMS-based 3-D structures and devices will be carried out in the state-of-the-art class-10 cleanroom at the ***Laboratory for Physical Sciences (LPS)*** (http://www.lps.umd.edu/). The facilities at LPS include a 5X GCA ALS i-line stepper, Karl Suss contact aligner, PlasmaTherm (Unaxis) RIE and ICP, Oxford Plasmalab PECVD-RIE, Oxford HDCVD, Leica Cambridge electron-beam lithography system, CHA electron-beam metal evaporation system, flip-chip bonder and various wet processing equipment.

The A.J. Clark School of Engineering at UMD also houses three conventional cleanrooms for microelectronics, nanotechnology, optoelectronics and MEMS processes. Each facility has fundamental microfabrication equipment such as contact-mask aligner for photolithography, thin film deposition tools for evaporating and sputtering metals and dielectric films and a variety of wet-bench stations. One of these, the ***Laboratory for Advanced Materials Processing (LAMP)*** (http://www.enma.umd.edu/LAMP/), established in 1997 and directed by Professor Rubloff, is the primary site for in-situ chemical characterization of materials and processes (mass spectroscopy, FTIR, and acoustic sensing) as realized in semiconductor fabrication processes. In addition, a brand new class-100 ***Central Fabrication Facility*** is recently (September 2003) built and operational in the ***Institute for Research in Electronics and Applied Physics (IREAP)*** (http://www.ipr.umd.edu/iprweb/research.htm) for MEMS and Microsystems research at UMD. The new facility houses the following state-of-the-art MEMS equipment: (1) an inductively coupled plasma tool for deep reactive ion etching (DRIE) processes, (2) an aligner and bonder machine for both precision lithography and aligned wafer-level bonding research, (3) a chemical mechanical polisher for wafer alignment and bonding, multilevel MEMS structures, novel structures with conformal coatings, and systems-on-chip, an FIB machine and (5) an RF sputtering tool for deposition of both thin film metal and dielectric films.

12. Budget

Goldsman 2months	$21,607
Papadopoulos 2 months	$17,510
Bhattacharyya 1 month	$9,620
Ramahi 1 month	$8,782
Ghodssi 1 month	$9,280
Peckerar 1 month	$8,126
Blankenship 1 month	$11,992
Technician (1)	$40,000
Graduate Research Assistants (11)	$237,446
Administrative	$21,495
Total Salaries	$385,858
Fringe Benefits	$96,465
Tuition	$76,780
Total Salaries and Fringe Benefits	$559,103
Processing and Fab (MOSIS)	$200,000
Consultant	$25,000
Total Direct Costs	$784,103
F&A (27.5%)	$194,514
Total Costs	$978,616

13. Appendix

Power and Noise Calculations

We performed initial calculations to estimate the power requirements of our smart dust circuits. Below are a summary of the fundamental figures of merit for the CMOS processes that we expect to utilize in our initial investigations. We provide power values for different biases for the LNA and PLL. The calculations were all analytical, and account for tradeoffs between power and noise. In other words, it is tempting to design our circuits to use minimum power. However, the noise levels would most likely cause the circuits to be essentially dysfunctional. (Finding the minimum power, while maintaining noise tolerance, as well as linearity and impedance matching, will be part of our long term investigation.) The tables on the following pages summarize the amplifier characteristics for different power levels used. The design criteria used for these calculations are given in Table 1. All calculations are based on TSMC 0.25um and TSMC 0.18um process technologies. (The 0.13um process is also available in MOSIS, which could possibly support an even better performance of the circuit. However, less expensive prototyping will be accomplished first with older processes.)

Table 1 Design restrictions of the circuit

Frequency	5 (GHz, 0.25μm); 10(GHz,0.18μm)
Power Consumption	<=1 (mWatts)
Smallest Detectable Signal	1 (μV)
Source Resistance	50 (Ohms)

Table 2 Basic parameters for different processes in MOSIS

(a) NMOS

	TSMC 0.25 micron	TSMC 0.18 micron
$V_{th}(V)$	0.48	0.51
$W_{\min} / L_{\min}$	0.36/0.24	0.27/0.18
$K' = U_0 C_{OX} / 2 \quad (\mu A / V^2)$	124.3	168.3
$t_{OX} \quad (meters)$	5.7e-9	4.1e-9

(b) PMOS

	TSMC 0.25 micron	TSMC 0.18 micron
$V_{th}(V)$	-0.47	-0.53
$W_{\min} / L_{\min}$	0.36/0.24	0.27/0.18
$K' = U_0 C_{OX} / 2 \quad (\mu A / V^2)$	-24.4	-36.2
$t_{OX} \quad (meters)$	5.7e-9	4.1e-9

1. LNA

(a) 0.25um process,

W/L = 60, W = 14.4 um, f = 5 GHz
COX = 0.0060526 F/m^2
For minimum sized transistor, CGS = 0.34863 fF
CGS1 = 13.945 fF

Table 3 Calculated performance of LNA at different VDD values

V_{DD} (V)	0.5	0.6	0.7	0.8	0.9	1.0
V_{in_min} (V)	2.517e-9	5.9122e-10	3.3983e-10	2.4068e-10	1.8756e-10	1.5442e-10
g_{m1} (mA/V)	0.44073	1.8764	3.2644	4.6092	5.9147	7.184
Av (V/V)	6.6951	18.833	32.758	46.245	59.333	72.055
Av (DB)	16.515	25.498	30.306	33.301	35.466	37.153
NF (DB)	31.253	8.106	5.0845	3.8928	3.2543	2.856
Power (mW)	3.3696e-3	7.3288e-2	0.25879	0.58965	1.0923	1.7906

MOSIS has the following test results for the 0.25um process:

CIRCUIT PARAMETERS		UNITS
Inverters	K	
Vinv	1.0	1.00 volts
Vinv	1.5	1.08 volts
Vol (100 uA)	2.0	0.12 volts
Voh (100 uA)	2.0	2.25 volts
Vinv	2.0	1.15 volts
Gain	2.0	-17.41
Ring Oscillator Freq.		
D1024_THK (31-stg,3.3V)	201.59 MHz	
DIV1024 (31-stg,2.5V)	269.26 MHz	
Ring Oscillator Power		
D1024_THK (31-stg,3.3V)	0.10 uW/MHz/gate	
DIV1024 (31-stg,2.5V)	0.06 uW/MHz/gate	

COMMENTS: DEEP_SUBMICRON

(b) 0.18um process,

W/L = 78, W = 14 um, f = 10 GHz
COX = 0.0084146 F/m^2
For minimum sized transistor, CGS = 0.27263 fF
CGS1 = 14.177 fF

Table 4 Calculated performance of LNA at different VDD values

V_{DD} (V)	0.5	0.6	0.7	0.8	0.9	1.0
V_{in_min} (V)	NA	4.7991e-10	2.3258e-10	1.5568e-10	1.1812e-10	9.5828e-11
g_{m1} (mA/V)	NA	2.3116	4.7697	7.1257	9.3913	11.576
Av (V/V)	NA	22.823	47.085	70.33	92.676	114.22
Av (DB)	NA	27.167	33.458	36.943	39.339	41.155
NF (DB)	NA	6.7681	3.7954	2.8712	2.4198	2.1518
Power (mW)	NA	0.062229	0.30911	0. 78845	1.5407	2.6012

MOSIS has the following test results for the 0.18um process:

CIRCUIT PARAMETERS		UNITS
Inverters	K	
Vinv	1.0	0.75 volts
Vinv	1.5	0.79 volts
Vol (100 uA)	2.0	0.07 volts
Voh (100 uA)	2.0	1.64 volts
Vinv	2.0	0.82 volts
Gain	2.0	-22.97
Ring Oscillator Freq.		
D1024_THK (31-stg,3.3V)	342.52 MHz	
DIV1024 (31-stg,1.8V)	402.90 MHz	
Ring Oscillator Power		
D1024_THK (31-stg,3.3V)	0.07 uW/MHz/gate	
DIV1024 (31-stg,1.8V)	0.02 uW/MHz/gate	

COMMENTS: DEEP_SUBMICRON

2. PLL Power Consumption

size = Minimum Size for all the transistors;
inverterNum = 9;
NandNum = 3;
phaseDifference = 0.05 rad;
Ipump = 10e-6 Amp;
VcoStage = 3;
freqClock = 0.5 * freqOscillation GHz;

Table 5 0.25 um, Oscillating Frequency = 5 GHz

V_{DD} (V)	0.5	0.6	0.7	0.8	0.9	1.0
Power of Single Inverter (mW)	0.0033	0.0047	0.0064	0.0084	0.0106	0.0131
Power of all inverters (mW)	0.0294	0.0424	0.0577	0.0753	0.0953	0.1177
Power of Charge Pump (mW)	0.00025	0.0003	0.00035	0.0004	0.00045	0.0005
Power of VCO (mW)	0.0039	0.0056	0.0077	0.0100	0.0127	0.0157
Power in PLL (mW)	0.0336	0.0483	0.0657	0.0857	0.1085	0.1339

Table 6 0.18 um, Oscillating Frequency = 10 GHz

V_{DD} (V)	0.5	0.6	0.7	0.8	0.9	1.0
Power of Single Inverter (mW)	NA	0.0037	0.0050	0.0065	0.0083	0.0102
Power of all inverters (mW)	NA	0.0331	0.0451	0.0589	0.0745	0.0920
Power of Charge Pump (mW)	NA	0.0003	0.00035	0.0004	0.00045	0.0005
Power of VCO (mW)	NA	0.0044	0.0060	0.0079	0.0099	0.0123
Power in PLL (mW)	NA	0.0378	0.0514	0.0671	0.0849	0.1048