Derivation of MOSFET Threshold Voltage from the MOS Capacitor

ENEE 313 Notes
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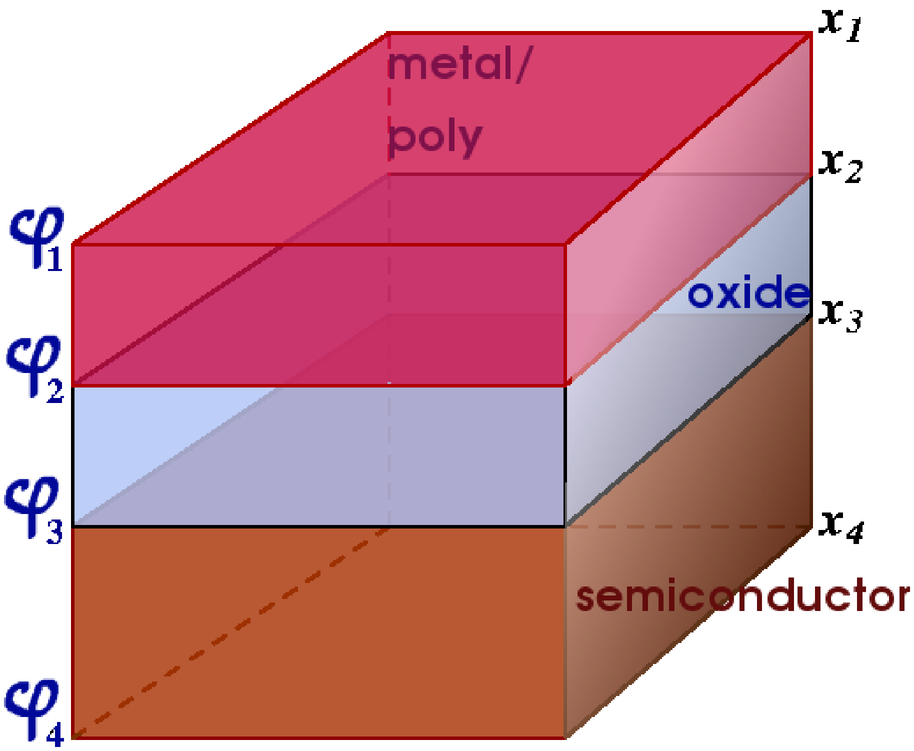
Threshold voltage is the voltage applied between gate and source of a MOSFET that is needed to turn the device on for linear and saturation regions of operation. The following analysis is for determining the threshold voltage of an N-channel MOSFET (also called an N-MOSFET). The analysis is performed with a MOS capacitor like the one shown below.



Structure

- MOS Capacitor: Top layer is N-type polysilicon or metal. For this derivation we will assume it is heavily doped N-type polysilicon with doping N_D
- S_1O_2 (oxide) insulation sandwiched between two conductors
- The bottom layer is P-type semiconductor of doping N_A

We will relate the built-in potential of the device to the voltage drop across the three layers. Since we have not added any external voltages, the total drop will be due to the built-in potential only. The total potential drop is the sum of the drops over different layers.

$$\varphi_1 - \varphi_4 = (\varphi_1 - \varphi_2) + (\varphi_2 - \varphi_3) + (\varphi_3 - \varphi_4) \quad (1)$$

$$(\varphi_1 - \varphi_2) = \varphi_{\text{poly}} \quad = \text{drop across poly} \quad (\varphi_{\text{poly}} = 0) \quad (2)$$

$\left(\varphi_2 - \varphi_3\right) = \varphi_{ox} =$ drop across oxide (3)

$\left(\varphi_3 - \varphi_4\right) = \varphi_{Si}$ = drop across P-type silicon (4)

Define $\varphi_1 = \varphi_n$, $\varphi_4 = \varphi_p$, $\varphi_3 = \varphi_s$ & $\varphi_{bi} = \varphi_n - \varphi_p$ (5), where s=surface between p-Si and SiO$_2$

$\varphi_p = -V_{Th} \ln \frac{\mathrm{N_A}}{\mathrm{n_i}}$ = built in potential on P-substrate (6)

φ_s is the potential at the surface between the p-Si and SiO$_2$

Summing all the drops we write the built in potential as

$\varphi_{bi} = \varphi_n - \varphi_p = \varphi_{ox} + \varphi_{Si} = \varphi_{ox} + \left(\varphi_s - \varphi_p\right)$ = total potential drop. (7)

Now we know the built in voltage in terms of two unknowns φ_{ox} & φ_{Si}. Our goal now will be to reduce the number of unknowns, and eventually determine the built in voltage as a function of the surface potential φ_s only.

We now need to find φ_{ox}, we know

$\varphi_{ox} = \int_{x_2}^{x_3} \mathrm{E_{ox}}\, dx = E_{ox}\left(x_3 - x_2\right) = E_{ox} t_{ox}$ (8)

$\left(E_{ox}\right.$ = constant because the is no charge in oxide$\left.\right)$

Now need to find E_{ox}. So the next ten or so lines of equations are written to determine E_{ox}.

Start by using Gauss' law

$\varepsilon_{ox} E_{ox}\big|_{x=x_3} = \varepsilon_{Si} E_{Si}\big|_{x=x_3}$ (9)

We can calculate E_{Si} at interface

Use depletion approximation to calculate E_{Si}. In the silicon under the oxide the p-type material is depleted due to the built in potential. Thus, there is charge there due to acceptor ions since the holes are absent. Use the depletion approximation to solve for the field in the silicon due to the ionized acceptors. The width of the depletion region is w_D.

Starting with the Poisson equation, while using the approximation that $n=0$, $p=0$ in the depletion region, we have:

$$\frac{\mathrm{dE_{Si}}}{\mathrm{dx}} = \frac{\mathrm{-q}}{\varepsilon_{\mathrm{si}}}\mathrm{N_A} \quad (10)$$

$$\mathrm{E_{Si}}\left(x\right) = \frac{\mathrm{q}}{\varepsilon_{\mathrm{si}}} N_A \left(w_D + x_3 - x\right) \quad (11)$$

$$\mathrm{E_{Si}}\left(x_3\right) = \frac{\mathrm{q}}{\varepsilon_{\mathrm{si}}} N_A w_D \quad (12)$$

$$\varphi_{Si} = \int_{x_3}^{x_4} \mathrm{E_{Si}}\left(x\right) dx \quad (13)$$

$$= \frac{1}{2}\left(base\right)\left(height\right)\text{of depletion region} = \frac{1}{2} E_{Si}\left(x_3\right) w_D = \frac{1}{2}\left(\frac{\mathrm{q}}{\varepsilon_{\mathrm{si}}} N_A w_D\right) w_D \quad (14)$$

Solve for w_D

$$w_D = \left[\frac{2\varepsilon_{Si}}{\mathrm{qN_A}}\varphi_{Si}\right]^{1/2} = \left[\frac{2\varepsilon_{Si}}{\mathrm{qN_A}}\left(\varphi_s - \varphi_p\right)\right]^{1/2} \quad (15)$$

Finally, substituting w_{D} of (15) into equation (12), we have some usable expression for field in terms of the surface potential:

$$E_{ox} = \frac{\varepsilon_{Si}}{\varepsilon_{ox}} E_{Si} = \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \frac{q}{\varepsilon_{Si}} N_A \left[\frac{2\varepsilon_{Si}}{\mathrm{qN_A}}\left(\varphi_s - \varphi_p\right)\right]^{1/2}$$
$$= \frac{1}{\varepsilon_{ox}}\left[2\varepsilon_{Si}\mathrm{qN_A}\left(\varphi_s - \varphi_p\right)\right]^{1/2} \quad (16)$$

Note that all terms in (16) except for the surface potential are determined by the manufacturer, or are material constants.

Finally we can now find φ_{ox}

$$\varphi_{ox} = E_{ox} t_{ox} = \frac{t_{ox}}{\varepsilon_{ox}}\left[2\varepsilon_{Si}\mathrm{qN_A}\left(\varphi_s - \varphi_p\right)\right]^{1/2} = \frac{1}{C_{ox}}\left[2\varepsilon_{Si}\mathrm{qN_A}\left(\varphi_s - \varphi_p\right)\right]^{1/2} \quad (17)$$

where $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ is the capacitance of the oxide capacitance of the MOSCAP per unit area.

An important point to notice here is that φ_{ox} is now written in terms of φ_s, so we have reduced the number of unknowns to one.

Now back to original equation

$$\varphi_{bi} = \varphi_n - \varphi_p = \varphi_{ox} + \varphi_{si} = \frac{1}{C_{ox}}\left[2\varepsilon_{Si}\mathrm{qN_A}\left(\varphi_s - \varphi_p\right)\right]^{1/2} + \left(\varphi_s - \varphi_p\right) \quad (18)$$

φ_{bi} is also called $\varphi_{ms} = -V_{FB}$

Note that all terms in this equation are now known except for φ_s

Include Gate Voltage

Now, instead of working with just the built in potential, we add a voltage V_G to the gate of the MOS capacitor. Now the equation for the total electrostatic potential drop across the MOS capacitor is:

$V_G + \varphi_{bi} = \varphi_{ox} + \varphi_{Si} = \varphi_{ox} + \left(\varphi_s - \varphi_p\right)$ = total potential drop. (19)

Of course, since we have added V_G, values for φ_{ox} and φ_{Si} will change. However, if we look back at equation (18), we see that the only parameter that is not already determined in that equation is the surface potential φ_s. V_G will cause the potential at the interface φ_s to change. So we can conclude that the effect of adding a gate voltage to the MOS capacitor will cause the surface potential to change as shown in equation (20):

$$V_G = \frac{1}{C_{ox}}\left[2\varepsilon_{Si} q N_A (\varphi_s - \varphi_p)\right]^{1/2} + \varphi_s - \varphi_p - \varphi_{bi} \quad (20).$$

As shown in equation (20), changing the gate voltage will change the surface potential. This will ultimately change the concentration of electrons at the Si-SiO$_2$ interface, and eventually, for a MOSFET adjust the drain current for the devices.

THRESHOLD VOLTAGE

Threshold Voltage Definition: V_{TH} **is the value of** V_G that will cause the interface potential to be equal in magnitude and opposite in sign to the substrate potential φ_p . Physically this mean that there would now be a mobile electron concentration at the surface that is equal in magnitude to the mobile hole concentration is the p-substrate. When this happens we say that the surface is **INVERTED, and the electron channel at the surface is called the inversion layer.**

So define threshold voltage as

$$V_G = V_{TH} \quad \text{when } \varphi_s = -\varphi_p \quad (21)$$

Substituting in V_{TH} and φ_s , we obtain the following expression for **the threshold** voltage in n-channel MOSFETs.

$$V_{TH} = \frac{1}{C_{ox}}\left[4\varepsilon_{Si} q N_A \,|\varphi_p|\,\right]^{1/2} + 2\left|\varphi_p\right| - \varphi_{bi}$$