SiC Power MOSFET Gate Oxide Breakdown Reliability – Current Status

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Gate oxide TDDB

--- more current ➔ shorter lifetime

**Intrinsic**

FN tunneling

**Extrinsic**

Trap-assisted tunneling
Pananakakis et al., JAP 78(4), 2635(1995)

Other seen even worse:

Lichtenwalner, D. J., B. Hull, et al., 2018 IRPS.

R. Watersa and B. Van Zeghbroeck, APL 76(8), 1039(2000)
Gate dielectric on any substrate is inferior to thermally grown SiO₂ on silicon!

Early results of SiO₂ on SiC thoroughly confirmed the fear!

However ....

Things started to change about 10 years ago.

L. Yu, K. P. Cheung, J. Campbell, J. S. Suehle and K. Sheng, 2008 IIRW FINAL REPORT, pp141-144

“Intrinsic” breakdown reliability has no problem!
Log(T\(_{63\%}\)) vs. E\(_{\text{OX}}\) (MV/cm)

- McPherson IEDM98 175\(^\circ\)C 9nm
- McPherson IEDM98 150\(^\circ\)C 9nm
- Suehle TED97 400\(^\circ\)C 22nm
- Suehle TED97 400\(^\circ\)C (15nm)

Its better than silicon!

300 \(^\circ\)C, 6.5 MV/cm, 10 yr. (For 63% failure)

How is that possible?

Breakdown is linked to tunneling current.

Reliable tunneling current data as a function of temperature is missing for both Si and SiC.

The physics of breakdown is known…. or is it?

Thermal-chemical model:
Current does not play a role, and the kinetic equation is problematic.

Hydrogen release model:
Hydrogen release as a function of tunneling current may differ between Si and SiC
How do released hydrogen generates defect is not known.

Anode-hole injection model:
Anode-hole is created by the decay of interfacial plasmon, Si and SiC is different.
How do hole injected from anode creates defect is not known.
Another possibility: Silicon data is not intrinsic.

SiC nMOS capacitors (40 x 250 um^2) with 50 nm thermally grown SiO_2

No extrinsic failure out of > 800 devices

Small sample size is very misleading.

- **a1**: 10,000 devices with 1% failures.
- **b1**: 10,000 devices with 10% failures.
- **a2**: 50 devices with a concentration of failures.
- **b2**: 50 devices with a smaller concentration of failures.

**Legend:**
- **ln(-ln(1-F))**
- **T_{BD}(s)**

**Graphs:**
- **10,000 devices**
- **50 devices**

**Note:** The graphs illustrate the difference in failure rates and distributions between small and large sample sizes.
Extracting lifetime directly leads to underestimation!

It may not be big enough to explain the result.
Intrinsic breakdown reliability of SiO$_2$/SiC MOS system is proven.

What about extrinsic failures?
Improving wafer cleanliness improved the initial distribution which is worse than this.

Further improvement in wafer cleanliness cannot improve beyond this.
The “luck defect” model

It explains further improvement must come from improving the oxide growth process itself.
Avalanche rugged low on-resistance 1200 V SiC MOSFETs with long-term stability

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Fig. 4. Positive stress oxide breakdown.

Fig. 5. Negative stress oxide breakdown.
Breakdown population is a joint distribution of intrinsic and extrinsic distributions.


Intrinsic failure (thick oxide): $\beta > 15$

Extrinsic failure (all oxide): $\beta < 1$

Lifetime is determined by the Extrinsic distributions.

First extract the distribution
Then do the projection.
The significance of Weibull slope $\beta$

### Failure fraction scaling:

$$\tau_{F1} = \tau_{F2} \left( \frac{\ln(1-F_1)}{\ln(1-F_2)} \right)^{1/\beta}$$

### Active area scaling:

$$\tau_{63}^P = \tau_{63}^T \left( \frac{A_T}{A_P} \right)^{1/\beta}$$

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<table>
<thead>
<tr>
<th>$\beta$</th>
<th>From characteristic failure time ($t_{63}$) to 0.63% failure time</th>
<th>From 100$\mu$m x 100$\mu$m test structure failure time to 10 cm$^2$ product failure time</th>
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<tbody>
<tr>
<td>$0.5$</td>
<td>$T_{63}/10000$</td>
<td>10 billion times shorter</td>
</tr>
<tr>
<td>$15$</td>
<td>$T_{63}/1.36$</td>
<td>2.15 times shorter</td>
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</tbody>
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For intrinsic lifetime of thick oxide, $t_{63}@E$ of any size test device is adequate.

For extrinsic lifetime of any oxide, failure fraction and test device area must be accounted for.
Status

Extrinsic failure still dominates SiC MOSFET breakdown reliability

No TDDB result with sufficient device under test has been reported.
   (Encouraging ramp voltage test has been reported)
   (Our TDDB result has too small an area)
   (These represent two examples of dramatic improvement – no longer stuck)

No extrinsic TDDB lifetime has been reported with proper extraction.

No standard reliability requirement has been established.

We are not out of the wood ... yet.