Short-circuit Capability of SiC MOSFETs

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Outline

1. Introduction
2. Test setup configuration
3. Test results
   - Current Saturation
   - Short-circuit
4. Design for longer Short-circuit Times
5. Conclusion
Short $L_{ch}$ results in lower $R_{ch}$ but reduces short-circuit time ($t_{sc}$).
Test setup

- Protector Resistor
- Bleeder Resistor 66kΩ
- DC Link Capacitor 300µF
- Ceramic Capacitor
- DC Source
- GND

- V_{DS}
- V_{G}
- DUT

- 5kΩ
- 18 V
- 700 V
- 62.5 A
- 1 µs
D1 (Si) is best up to 400 V
D3, D4 (SiC) seem best among SiC devices

<table>
<thead>
<tr>
<th>#</th>
<th>Material</th>
<th>Rating</th>
<th>$V_{GS}$</th>
<th>Area [mm$^2$]</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1</td>
<td>Si</td>
<td>900V/5.1A</td>
<td>9V</td>
<td>7.85</td>
</tr>
<tr>
<td>D2</td>
<td>SiC</td>
<td>900V/11.5A</td>
<td>18V</td>
<td>1.89</td>
</tr>
<tr>
<td>D3</td>
<td>SiC</td>
<td>1200V/12A</td>
<td>20V</td>
<td>3.85</td>
</tr>
<tr>
<td>D4</td>
<td>SiC</td>
<td>1200V/14A</td>
<td>20V</td>
<td>3.96</td>
</tr>
<tr>
<td>D5</td>
<td>SiC</td>
<td>1200V/31.6A</td>
<td>20V</td>
<td>8.48</td>
</tr>
</tbody>
</table>
All devices have 10 µs short-circuit time at $V_{DS}=300$ V

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<th>Material</th>
<th>Rating</th>
<th>$V_{GS}$</th>
<th>$V_{DS}$</th>
<th>Area [mm$^2$]</th>
<th>$E_{diss}$/Area</th>
<th>$V_{max}$ ($t_{SC}=10$ µs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1</td>
<td>Si</td>
<td>900V/5.1A</td>
<td>10V</td>
<td>300V</td>
<td>7.85</td>
<td>1.00J/cm$^2$</td>
<td>400V</td>
</tr>
<tr>
<td>D2</td>
<td>SiC</td>
<td>900V/11.5A</td>
<td>20V</td>
<td>300V</td>
<td>1.89</td>
<td>5.22J/cm$^2$</td>
<td>200V</td>
</tr>
<tr>
<td>D3</td>
<td>SiC</td>
<td>1200V/12A</td>
<td>20V</td>
<td>300V</td>
<td>3.85</td>
<td>3.71J/cm$^2$</td>
<td>300V</td>
</tr>
<tr>
<td>D4</td>
<td>SiC</td>
<td>1200V/14A</td>
<td>20V</td>
<td>300V</td>
<td>3.96</td>
<td>4.93J/cm$^2$</td>
<td>600V</td>
</tr>
<tr>
<td>D5</td>
<td>SiC</td>
<td>1200V/31.6A</td>
<td>20V</td>
<td>300V</td>
<td>8.48</td>
<td>5.41J/cm$^2$</td>
<td>500V</td>
</tr>
</tbody>
</table>

![Graph showing gate voltage and $I_{DS}$/Area over time](image)
D4 is the only 1200V SiC MOSFET with $t_{sc}=10\mu s$ at 600V

$V_{\text{max}}(t_{sc}=10\mu s)=400V$

$V_{\text{max}}(t_{sc}=10\mu s)=200V$

$V_{\text{max}}(t_{sc}=10\mu s)=300V$

$V_{\text{max}}(t_{sc}=10\mu s)=500V$

$V_{\text{max}}(t_{sc}=10\mu s)=600V$
Device are degraded after short-circuit test

Before SC test

After SC test

$V_T$ shifts to positive by 0.5 V

$V_{GS} = 8V \sim 20V$

$R_{on}$ increases
Conclusions for short-circuit test

✓ Only D4 could withstand 10μs of short-circuit time at 50% of the rated voltage.

✓ Design modification may improve short-circuit time.
Design for longer short-circuit times

[A] Conventional

[B] Shielded MOSFET

[C] BGMOSFET

2. Proceedings of the 30th ISPSD, 2018
[A] Increase in channel length increases $R_{\text{on}}$ (not preferred)
Long channel length results in:

- Higher channel resistance
- Lower output conductance

![Graph showing the relationship between drain current and drain voltage for different channel lengths.](image)
Very short channel length results in very high currents at short-circuit

\[ V_{gs} = 20V \]

- \( L_{ch} = 0.3\mu m \)
- \( L_{ch} = 0.5 \sim 2.0\mu m \)
Short channel length leads to high electric field at Point “A”
Short channel length leads to high peak electric field at Point “A”
Short-circuit time improves with shielded P+ structure\(^1\) + No increase in \(R_{\text{on}}\) + Reduced saturation current

Additional P⁺ shielding does not help

Source Metal

Inter Layer Dielectric

N⁺ Poly Si

Gate Ox, 500Å

N⁺ Source

2E17/cm³

Lₜₜ = 0.5µm

d=0.4µm

P⁺ = 1E19/cm³

P⁺ = 1E19/cm³

0.2µm

0.4µm

N drift layer for 1.2 kV device

: 10 µm, 1E16 /cm³

Substrate

Drain

V₉₅ = 20V

Shielded MOSFET, d=0.2µm (Lₜₜ=0.5µm)

Shielded MOSFET, d=0.4µm (Lₜₜ=0.5µm)

Drain voltage (V)

Drain current (A)
Electric field at point “A” reduces in shielded MOSFET
$R_{on}$ remains the same with shielded MOSFET

**Source Metal**

**Inter Layer**

**Dielectric**

**N$^+$ Poly Si**

**Gate Ox, 500Å**

**Ni Ohmic**

**P$^+$**

**N$^+$ Source**

2E17/cm$^3$

$L_{ch} = 0.5\mu$m

0.6µm

$d=0.2\mu$m

**P$^+$ = 1E19/cm$^3$**

**P well = 1E18/cm$^3$**

3.0µm

**N drift layer for 1.2 kV device**

: 10 µm, 1E16 /cm$^3$

**Substrate**

**P well = 1E18/cm$^3$**

**N$^+$ Source**

**Drain**

### Graph

- **V$_{gs}$ = 20V**
- **Conventional**
  - *(L$_{ch}$=0.5µm)*

**Shielded MOSFET, d=0.2µm**

*(L$_{ch}$=0.5µm)*

**Shielded MOSFET, d=0.4µm**

*(L$_{ch}$=0.5µm)*

**Drain current (A)**

- 1.5E-5
- 1.0E-5
- 5.0E-6
- 0.0E+0

**Drain voltage (V)**

- 0
- 5
- 10
- 15
- 20
1.2 kV rated SiC Buffered-Gate MOSFETs
Kijeong Han, Woongje Sung, B. Jayant Baliga
Proceedings of the 30th ISPSD conference, 2018
BG MOSFET increases $R_{on}$ but further reduces short-circuit current
- May require additional processing

![Graph showing the comparison between BG MOSFET and Conventional MOSFET with different channel lengths and x values at a gate voltage of 20V.](image)
Conclusions

We can keep short channel length and increase short circuit time by using Shielded MOSFET\textsuperscript{1}.