SiC MOSFETs at GeneSiC

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GeneSiC Mission

GeneSiC is dedicated to providing SiC-based power devices that offer

- Best-in-class performance
- Highest Quality for SiC power devices
- Competitive pricing
- Wide range of products applicable to wide range of applications
- Strong Product and Customer Support
Expertise Areas

- **SiC Device Design and Concepts**
  - Experts in SiC Designs and Concepts
  - 2D Device Simulations, Layout

- **Device Fabrication**
  - Fabrication Techniques for SiC
  - State-of-the-art Fab for standard proc

- **Testing & Packaging**
  - On-wafer and packaged parts tested in-house at GeneSiC
  - Packaging with partners
GeneSiC’s MOSFET Efforts

- DARPA/ONR HPE II Program 2005-7
  - 10 kV MOSFETs
- Commercial SiC MOSFETs 2015 -
- ONR Phase I/II SBIR Program 2016-
  - 6.5kV SiC MOSFET
- PowerAmerican BP3 2017-
  - 3.3kV SiC MOSFETs
Today’s Talk

• Epilayer and Device Design

• Static Electrical Characteristics
  – Impact of Device Design on Key MOSFET parameters
  – Temperature dependence of key parameters

• Double-Pulse Switching Performance
  – Influence of Drive Voltages

• Reliability and Robustness
  – HTGB
  – Avalanche Robustness
• SiC Planar DMOSFETs fabricated on 35 µm thick, \( \approx 2.8 \times 10^{15} \text{ cm}^{-3} \) doped N-drift epilayers
  – 2.74 mm x 2.74 mm Dies
  – FATFETs for field-effect mobility characterization

• The device design space constituted different JFET Doping Profiles, Channel Lengths and JFET spacings
  – Device Simulations used to ensure peak oxide field does not exceed 4 MV/cm
• 2.74 mm x 2.74 mm die
  – Active Area = 0.046 cm²
• $R_{on,sp}$ of 17.0 mΩ-cm², and breakdown voltage of 4600 V measured at 25°C
• BV close to theoretical limit for 35 µm/3x10^{15} cm⁻³ thick N- drift layer
• $V_{TH}$ extracted as 2.4 V (at $I_D = 5$ mA)
The temperature co-efficient of $R_{on}$ tracks very closely to the temperature dependence of (bulk) electron mobility

- On-Resistance is solely determined by N- drift layer properties

Impact of Gate Bias on $R_{DS,on}$ is less significant at higher operating temperatures

<table>
<thead>
<tr>
<th>Temperature</th>
<th>25°C</th>
<th>150°C</th>
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<tbody>
<tr>
<td>Increasing $V_{GS}$ from 15 V to 20 V</td>
<td>13.2% $R_{ON}$ reduction</td>
<td>2% $R_{ON}$ reduction</td>
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</tbody>
</table>
• $V_{TH}$ decreases from 2.4 V at 25°C to 1.4 V at 175°C.
  
  – Linear temperature co-efficient $= -6.3$ mV/°C
  – Mild temperature co-efficient of $V_{th}$ is an indication of a low (acceptor-type) MOS interface charge
• Breakdown voltage increases linearly with measurement temperature
• Extracted temperature co-efficient of avalanche breakdown as 1.33 V/°C
The negative drain bias (synchronous rectifier mode) performance of the DMOSFET at 25°C and 150°C is shown.

Depending on the magnitude of the gate bias and the junction temperature, the device operates in either purely bipolar mode, purely unipolar mode, or in a mixed-mode.
- **Switching waveform at 2 kV 5 A**
  - Room temperature
  - $V_{gs-on} = 20$ V
  - $R_{gs-on} = 10$ Ohm (external)

- **Switching-on loss at 2 kV**
  - Room temperature
  - $V_{gs-on} = 20$ V
  - $R_{gs-on} = 10 - 40$ Ohm (external)
Dynamic Test Results – Switching OFF

- **Switching waveform at 2 kV 5 A**
  - Room temperature
  - $V_{gs-off} = -5$ V
  - $R_{gs-off} = 5 \text{ Ohm (external)}$

- **Switching-on loss at 2 kV**
  - Room temperature
  - $V_{gs-off} = -5$ V
  - $R_{gs-off} = 5 \text{ - 40 Ohm (external)}$
DPTs on Device #4036 at Elevated Temperatures

Switching Loss at Elevated Temperatures

- Test temperatures: 25 °C, 60 °C, 100 °C (± 10 °C)
- Test conditions
  - $V_{dc} = 2$ kV
  - $V_{gs-on} = 20$ V, $R_{gs-on} = 20$ Ohm (external)
  - $V_{gs-off} = -5$ V, $R_{gs-off} = 5$ Ohm (external)

Switching-on Loss at 2 kV

Switching-off Loss at 2 kV
Dynamic Test Results – Switching OFF (Cont’d)

- **Switching waveform at 2 kV 5 A**
  - Room temperature
  - $V_{gs\text{-off}} = 0$ V
  - $R_{gs\text{-off}} = 5$ Ohm (external)

- **Switching-on loss comparison**
  - Room temperature
  - $V_{gs\text{-off}} = 0$ and -5 V
  - $R_{gs\text{-off}} = 5$ Ohm (external)

Zero gate-off voltage is not recommended:
- Safe concern
- No switching loss reduction

Gate ringing ≈ 4 V > $V_{gs\text{(th)}}$
$dv/dt = 40$ kV/μs
$V_{gs}$: 20 V/div
$V_{ds}$: 1 kV/div
$I_d$: 2 A/div
$di/dt = 0.28$ kA/μs
$di/dt = 0.06$ kA/μs
$di/dt = 0.17$ kA/μs

Switching-off Loss at 2 kV, $R_{gs\text{-off}} = 5$ Ω

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Energy Efficiency Through Innovation

The Ohio State University
High-Temperature Gate Bias Stressing

- Stress Bias applied with device on a 150°C hotplate
- Transfer I-V measured at 150°C within 5 seconds after interruption of stress bias
- $V_{GS}$ shifts by +0.35 V during the PBTS sequence
- $V_{GS}$ shifts by -0.02 V during the NBTS sequence
• A behavioral SPICE model has been developed by GeneSiC for SiC MOSFETs
• Using this model, we have accurately modeled the DC and capacitance characteristics of the 4.6 kV SiC DMOSFETs
Avalanche Robustness of 4600 V DMOSFETs

• Short-Circuit and Unclamped Inductive Switching (UIS) tests are widely used to define the SOA limits of power devices.

• Avalanche ruggedness of a power device is determined by its ability to dissipate avalanche energy (EAV) without catastrophic device failure.
  – Both single-pulse and repetitive avalanche ratings are important for ultra-fast SiC power MOSFETs, since high voltage overshoots can be generated due to high \(\frac{di}{dt}\) during device turn-off.

• An avalanche rugged device enables snubber-less converter design, leading to drastic reduction in cost, # of components and converter size.

• Automotive applications such as anti-lock braking systems and engine control units require power devices to dissipate more consistent overload transient energy release from inductive loads (motors, actuator controlled solenoids).
UIS Test Setup

Energy Efficiency Through Innovation
SiC MOSFET successfully conducts a single-pulse avalanche energy ($E_{AS}$) of 927 mJ (11.9 J/cm$^2$ normalized to the total chip size), at a peak drain current of 7 A, and drain voltage of 5100 V.

An $E_{AS}$ of 11.9 J/cm$^2$ is among the highest ever recorded for a SiC MOSFET.
Failure analysis after avalanche test

- Microscope images were taken after decapping the avalanche failed parts
- Failure location is clearly localized within the active area of the chip, close to the gate pad
The power transient (drain current x drain voltage) measured during the 927 mJ UIS test was fed into an R-C network representing the transient thermal impedance of the packaged MOSFET.

The evolution of the junction temperature transient was then simulated in SPICE:
- Peak $T_J = 850^\circ C$ during the avalanche pulse is simulated, which is responsible for device destruction.
Stability of Electrical Characteristics after single pulse avalanche stress

- Minor degradation of Vth, drain/gate leakage current observed after single avalanche pulses of increasing energy up to 800 mJ
- No degradation (not shown) of output, transfer and body diode characteristics as well
Summary

• Large-Area, 2.74 mm x 2.74 mm SiC DMOSFETs fabricated with
  – \( BV > 4600 \) V
  – Low \( R_{ON,SP} \) (17 m\( \Omega \)-cm\(^2\))
  – \( V_{TH} \sim 2.4 \) V
• Investigated impact of device design variations on key MOSFET electrical parameters
• Quantified temperature dependence of \( R_{DS,ON} \), \( V_{TH} \) and \( BV \)
• Demonstrated Double-Pulse Switching Performance at \( V_{DS} = 1800 \) V and \( I_D = 6 \) A
  – Quantified Impact of gate drive voltage and \( R_{G,ext} \) on turn-on energy losses
• Developed comprehensive SPICE model for SiC MOSFETs
• Presented preliminary results from BTS measurements
• Presented experimental results from single-pulse avalanche robustness measurements
\( R_{DS,ON} \) for Various Designs

- \( R_{DS,ON} \) reduces with increasing JFET spacing
- Higher JFET doping has clear impact in reducing \( R_{DS,ON} \)

- \( R_{DS,ON} \) increases with increasing \( L_{ch} \)
- Higher variation in \( R_{DS,ON} \) observed in devices with low JFET doping
Drain Leakage Current ($I_{DSS}$) for various device designs

- No significant impact of JFET Doping on $I_{DSS}$
- Median $I_{DSS}$ is higher for wider JFET spacing, for devices with higher JFET doping

- Median $I_{DSS}$ values are < 30 nA at $V_{DS} = 2400$ V
- No significant impact of $L_{CH}$ on $I_{DSS}$
Gate Leakage Current ($I_{GSS}$) for various device designs

- Median $I_{GSS}$ values < 1 nA for all designs
- No impact of JFET doping on gate leakage current

- Very slight statistical decrease of $I_{GSS}$ observed for longer channel DMOSFETs
Gate Threshold Voltage ($V_{TH}$) for different device designs

- No impact of JFET Doping on $V_{th}$
- $V_{th}$ is only weakly dependent on the JFET Spacing

- Clear dependence of $V_{th}$ on MOS channel length is observed
  - $V_{th}$ reduction at lower channel lengths is due to the DIBL effect
Parasitic Capacitance Measurement (Device # 171 vs. Device #061)

- **Test conditions**
  - Room temperature
  - $V_{ds} = 0 \text{ to } 2.5 \text{ kV}$
  - Test frequency = 100 kHz

**Test results on device #171**

**Comparison between two devices**
• $V_{DS}$ fall time = 30 ns achieved for switching at 1800 V and 6 A, with +20 V drive voltage and $R_{G,ext} = 10 \, \Omega$
Double Pulse Switching Characterization (Univ. of Bremen)

- $V_{DS}$ rise time = 30 ns achieved for switching at 1800 V and 6 A, with -3.3 V Gate Drive Voltage
Energy Efficiency Through Innovation

Double Pulse Switching Characterization (Univ. of Bremen)

- Energy Losses are extracted from switching waveforms measured at various drain current levels and different gate drive voltages
- 22% decrease in $E_{ON}$ observed, when gate drive voltage is increased from $+15$ V to $+18$ V
- Further increase of drive voltage from $+18$ V to $+20$ V only yielded 9% improvement in $E_{ON}$
• Dedicated double-pulse board developed by Prof. Kaminski’s group at Univ. of Bremen for high-voltage switching of GeneSiC DMOSFETs. Studied impact of $V_{\text{drive}}$ in the range of +15-20 V, and (external) gate resistance in the range of 10-30 Ω on switching characteristics.

• Performed switching measurements at DC link voltage of 1800 V and $I_D = 6$ A.
  – The body diode of a second MOSFET was used as the FWD.
Double Pulse Switching Characterization (Ohio State Univ.)

- Dynamic Test at Room Temperature
  - Tests performed on device #4036 at 2 kV, upto 5 A
    - Switching on
      - \( V_{gs-on} = 20 \) V and \( R_{gs-on} = 10, 20, 30, 40 \) Ohm (external)
    - Switching off
      - \( V_{gs-off} = -5 \) V and \( R_{gs-off} = 5, 10, 20, 30, 40 \) Ohm (external)
      - \( V_{gs-off} = 0 \) V and \( R_{gs-off} = 5 \) Ohm (external)

- Gate on/off resistance limitations

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Switching-on with 20 V and 5 Ohm

Switching-off with - 5 V and 0 Ohm