Status of PEMC

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On July 16, 2014 NY Governor Andrew M. Cuomo announced Phase-1 of the New York Power Electronics Manufacturing Consortium:

- Class-100 cleanroom with ISO-9001 quality, MES controls and ESD protection
- Capacity to produce 30,000-50,000 wafers/year
- New equipment specified for 200mm, capable of processing 150mm wafers
- Full complement of metrology and analytical equipment
- SUNY Poly’s proven environment for partnership and IP protection
SiC Technical Transition Team

“PEMC - Power Electronic Manufacturing Consortium” for SiC manufacturing with production capabilities at SUNY Polytechnic Institute”

Lab Core Expertise / Capabilities

- High volume SiC manufacturing
- Equipment procurement
- Equipment/process verification and validation (V&V),
- Device integration, ISO 9001 2008 quality certification and product qualification

Key Equipment / Infrastructure

- Class 100 Cleanroom with ESD controls
- Full suite of 200mm State of the Art high volume manufacturing equipment capable of processing 150mm SiC wafers
- BEOL/FEOL Contamination isolation
- Factory Information system (MES, QMS, YMS, FDC)
Some Critical Process Capabilities
Photo lithography Capabilities

Coat:
- Thick and thin resist
- Positive and negative tone resist
- Photo-definable polyimide process

Expose:
- 5X i-line stepper with 0.35um resolution
- High throughput with <40nm overlay accuracy
- Front and back of wafer alignment

General:
- Separation of FEOL and BEOL processes
- High throughput, production-proven equipment set

Equipment Set:
- In-line FEOL and BEOL coat tracks
- Two i-line steppers
- Polyimide coat track
- Automated optical overlay and CD
- Automated optical inspection for both FEOL & BEOL
Ion Implant Capabilities

Implant Capabilities:

- Ion species available:
  - Nitrogen
  - Aluminum
  - Boron
  - Argon
- Implant energy range: 2 - 335 KeV for singly charged species
- Dose range: $2 \times 10^{10} - 1 \times 10^{16}$ /cm$^2$
- Heated wafer chuck up to 700 C

Equipment – 300 mm medium current implanter modified for 150 mm SiC

- Robotic handling modified for 150 mm SiC heated implants
- Automated wafer handling with cassette to cassette operation
- Average front side particle adders $<20 \@ >0.20$ um
- Internal ESD control
- Energy contamination spec: $<0.1\%$
- Beam parallelism: $<0.2$ degrees
- Programmable chuck tilt and rotation
Thermal / CVD Process Capabilities

**PECVD:**
- Oxide - Silane Based
- Nitride - Silane Based

**LPCVD:**
- High Temperature Oxide
- Low Temperature Oxide
- Polysilicon

**Atmospheric:**
- High Temperature Oxidation,
- Dry/Wet Oxidation/Anneal (general use furnaces)
- Anneals:
  - Rapid Thermal Processing to 1200°C, N2, O2, Ar (vacuum capable)
  - High Temperature Implant Activation

**Equipment:**
- Rapid Thermal Anneal System ~8 W.P.H. (single wafer system)
- Four Tube Horizontal Furnace System
  1. Gas phase doping Tube - 100 Wafer Batch
  2. Dry/Steam Oxidation Tube – 100 Wafer Batch
  3. HTO LPCVD Tube - 50 Wafer Batch
  4. LTO LPCVD Tube - 50 Wafer Batch
- Four vertical single tube furnace systems
  1. 2x High Temp. Oxidation
  2. One LPCVD Polysilicon
  3. One LPCVD HTO
- High Temperature Implant Activation – 50 Wafer Batch
- 3 Chamber PECVD system: (1 Nitride, 2x Oxide – Single Wafer Chambers)

*Throughput Capability is process dependent*
Dry Etch Process Capabilities

Etch Capabilities:

- FEOL SiC, silicon, and dielectric using photoresist and oxide masks
- MOL Gate and ILD
- BEOL metal/strip and dielectric
- FEOL, MOL, and BEOL ash

Equipment Set – 150mm tools capable of 200mm upgrade:

- FEOL: ICP chamber for SiC and Si etch, Capacitively Coupled chamber for oxide etch
- MOL: ICP chamber for polysilicon gate etch, Capacitively Coupled chamber for oxide etch
- BEOL: ICP chamber and passivation chamber for metal etch, capacitively coupled chamber for oxide and nitride etch
- Dedicated FEOL, MOL, and BEOL downstream plasma ash chambers for PR strip
  - Full spectrum optical endpoint systems on most chambers
  - All tools have automated wafer handling with cassette to cassette operation.
Metrology Capabilities

Defect Inspection:

- Bare substrate and epi-wafer characterization.
- Confocal optics and differential interferometry for surface defects.
- Photoluminescence for crystal defects (e.g. Basal Plane Dislocation (BPD)).
- Tunable automated defect classification (ADC)

- High-resolution defect review (patterned and unpatterned).
- Separation of FEOL and BEOL processes.
- Si particle counting.
- Defect review SEM with EDX capability

General:

- Transparent film measurement using reflectometry and ellipsometry
- Step height measurement using profilometers
- Film stress over temperature
- 4-point probe for sheet resistance
- Metal contamination control using TXRF.

Equipment Set:

- Unpatterned SiC wafer inspection with photoluminescence
- Bare Si wafer particle inspection
- 4-Point Probe Wafer mapping system
- Automated Film measurement systems FEOL & BEOL
- Film stress measurement system
- Automated optical inspection for FEOL & BEOL
- Cassette to cassette automated inspection microscopes
- SEM defect review SEM with EDX
- TXRF
- Profilometers
- Automated overlay and CD metrology
Test Capabilities:

Parametric testing for SiC MOSFETs, JFETs, SBDs, and thyristors
- 100, 150, 200 mm SiC Wafer diameter
- Up to 5000 V, 100 A, 250°C testing
- Cassette-to-cassette handling
- Automatic data transfer & analysis

TDDB reliability testing for SiC MOSFETs and IGBTs
- Fully automatic cassette-to-cassette
- High temp and higher voltage failure rate acceleration
- Failure rate analysis (time zero, extrinsic, intrinsic failures)

Equipment Set – 150mm tools capable of 200mm upgrade:
- Fully automatic high power parametric tester
- 3-TDDB test systems for reliability tests
- Parametric test system for engineering / SPC structures
- SMU based test system for threshold voltage stability
- Parametric Curve Tracer test system for FA & engineering tests
- 4-Fully-auto probers for 150, 200 mm SiC wafers (low voltage)
- 2-Fully auto probers for 150, 200 mm SiC wafers (high voltage)
- 2-Manual/semi-auto probers for up to 200 mm engineering tests

Manual for up to 5 KV, Semiauto for up to ~600 volts
Status/Schedule/Next steps
On Aug 20, 2015 NY Governor Andrew M. Cuomo announced Phase-2 of the New York Power Electronics Manufacturing Consortium

SiC Module and Power Block Fab Located at SUNY Poly in Utica, NY:

- Class-1000 cleanroom with ISO-9001 quality, MES controls and ESD protection
- 185ksqft floor space, 52ksqft fab space, capacity to produce 300,000+ modules/year
- High level of automation with flexibility to produce multiple product families
- Products to serve diverse markets: Industrial, Transportation, Aerospace, Auto, ...
- SUNY Poly’s proven environment for partnership and IP protection
NY-PEMC SiC Timeline

given by P. Farrar at Semicon West, 13-July, 2016

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<td>Fab Prep</td>
<td>Equipment Installation</td>
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also: "35 of 63 tools on-site today"
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