USCi MOSFET progress
(ARL HVPT program)

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- USCi product line
- 1200V MOSFET progress
- 10kV IGBT and MPS progress
USCI Released Products

- **JBS Diodes**
  - 650V
  - 1200V
  - Best in class VF-Qc
  - Excellent UIS and Surge
  - Die suitable for 250°C

- **Normally-on JFET**
  - 1200V
  - Lowest RdsA 1200V switch
  - Excellent Short circuit
  - Robust UIS
  - Die suitable for 250°C

- **Cascode co-pack**
  - 1200V
  - Replaces IGBT+FRD
  - Or MOSFET+JBS
  - 0 to 12V gate drive
  - Excellent Diode behavior
  - Excellent Short circuit
  - Robust UIS

Custom 10KV diodes
Custom 300°C Diodes
Overview of USCI Transistor Technologies

- **Normally-on Trench Vertical JFET**
  - Circuit Protection
    - Current limiter
    - SSPC
    - SCCB
  - Switching: Super cascode
    - 6.5KV
    - 10KV

- **Normally-off Trench Vertical JFET**
  - Tj > 200°C
  - Switching applications
  - All Vds ratings

- **SiC Planar MOSFET**
  - Tj < 200°C
  - Switching applications
  - > 1.7KV (Planar)
  - > 650V Trench

**USCi**: 11th annual SiC MOS workshop, UMD College Park, August 18-19, 2016

- 1200V RdsA - 1.75mΩ·cm²
- 650V RdsA - 0.75mΩ·cm²
- 1200V RdsA - 3mΩ·cm²
- *Target 1200V RdsA* – 4-5mΩ·cm²

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1200V MOSFET Development Status
1200V 40mOhm MOSFET in TO-247 (6-inch X-fab): static characteristics

1st engineering lot: performance to be further optimized

Edge-termination and passivation are ok!
Inductive Load Switching Performance of the 1200V 40mOhm MOSFET in TO-247 (1st Engineering Lot)

Switching loss can be reduced by decreasing external gate resistor $R_G$ of the MOSFET.

Normal Switching Characteristics
Oscillations caused by the testing setup
Turn-on: $t_r=44$ns, $E_{on}=538\mu$J
Turn-off: $t_f=28$ns, $E_{off}=201\mu$J
<table>
<thead>
<tr>
<th>Test</th>
<th>stress condition</th>
<th>duration</th>
<th>sample size</th>
<th>status</th>
</tr>
</thead>
<tbody>
<tr>
<td>HTGB</td>
<td>VGS=+20V, VDS=0, Ta=150C</td>
<td>1000hrs</td>
<td>77</td>
<td>Pass</td>
</tr>
<tr>
<td>HTGB</td>
<td>VGS=-10V, VDS=0, Ta=150C</td>
<td>1000hrs</td>
<td>77</td>
<td>Pass</td>
</tr>
<tr>
<td>HTRB</td>
<td>VDS=960V, VGS=0, Ta=150C</td>
<td>1000hrs</td>
<td>77</td>
<td>Pass</td>
</tr>
<tr>
<td>AC</td>
<td>Tamb=121ºC, 100% RH, 205 Kpa,</td>
<td>96 Hrs</td>
<td>77</td>
<td>Pass</td>
</tr>
</tbody>
</table>
1200V 40mOhm MOSFET in TO-247: preliminary reliability assessment

1000 hr HTRB @ VDS=960V, VGS=0, Ta=150C
1000 hr HTGB @ Vgs=+20/-10V, Vds=0V, Ta=150°C

HTGB (Vgs=+20V), 150°C

HTGB (Vgs=-10V), 150°C
Autoclave @ Ta=121°C, Rh=100%, P=205kPa

Graphs showing the comparison of Pre AC Test and Post AC Test for IDSS2 @1200V (left) and VTH-5.0 @10mA (right).
1200V 40mOhm MOSFET in TO-247: preliminary UIS robustness evaluation

*Vgs=+12V  Vgs=-5V
Id=20A
Vds=0V  Vds~1700V

Optimization of unit cell has been implemented in a new lot in order to suppress electric field in gate oxide and further improve UIS robustness.

L=5mH, E=1.4J

Avalanche is clamped within each active cell
1200V 40mOhm MOSFET in TO-247: preliminary short-circuit capability assessment

$V_{DS} = 600V$

$V_{GS} = -5V$ to $+15V$

$I_D$

8us

Device ID#: A23
External $R_g = 22\Omega$

10us

Device ID#: A23
External $R_g = 22\Omega$

Two devices tested:
Device #A23: Pass 8us SC testing, fail 10us SC testing
Device #A26: Pass 8us and 10us SC testing
Device #A26: pass 10μs SC test

Device #A23: fail at 10μs SC test

- Device unit cell layout will be optimized in a new lot;
- Vt increased in a new 1200V-40mOhm lot;
- SC-capability will be re-evaluated;
- 3300V SC-robust MOSFET lot is in the line;
The threshold voltage of the second qualification lot is basically in the target range.
10kV IGBT and MPS Development Status
After top-side MOS structure is formed, substrate is completely ground away, N-type field-stop layer and P+ injector are ion-implanted, and laser-activated.
Starting Epi: 11um of 8E15cm⁻³ N type (Si-face).
Blanket nitrogen and aluminum co-implants
Laser-assisted P & N dopant activation
Diode mesa isolation and contact metal deposition (inset)
Diode singulation, packaging and testing

Laser-activated PN diode have been formed!
First IGBT results (4-inch fab) Laser backside activated

- PN-junction knee voltage is present;
- C-face may be a challenge;
- P+ ohmic contact may be poor;
- Narrow process window for laser activation;
High-voltage MPS diodes

MPS diodes with 22mm² active area: bipolar operation is present, but diode performance on 150um (free-standing epi) has significant die-to-die and wafer-to-wafer variation.
10kV IGBT/MPS module design

- USCi in-house packaging
  - low-cost and short lead time
- Voltage rating up to 10kV
  - Small change to 15kV
- One solder joint – chip to DBC
- Pressfit Power Leads
  - Replaceable leads
- 60A max continuous
  - 20A per pin
- Tjmax=175C ~ 200C
- Al wire bond

USCi: 11th annual SiC MOS workshop,
UMD College Park, August 18-19, 2016
Established a 6-inch platform for large area 1200V MOSFETs targeting power modules

New 1200V 40 mOhm MOSFET lot is in the line (6-inch):
- Optimized unit cell structure and device layout – expecting target performance;
- Process tuned;
- Increased Vt;
- Reduced Idsx leakage and improved shielding of gate oxide;
- Expect improved UIS and SC capability;

3300V SC-robust MOSFET lot is in the line (6-inch)
- Ion-implanted and laser-activated PN junction demonstrated on Si-face, although process is not reproducible and so far not successful on C-face
- IGBT process baseline demonstrated at 4-inch fab, including substrate removal, backside ion implantation and laser-anneal, although major technological challenges are unresolved
  - Thick epi wafer warpage, LTV, TTV, and surface roughness are problematic on 4-inch;
  - Laser-activation of p- and n-type dopants and ohmic contact formation on C-face of a free-standing low doped epi was not successful – we may have to abandon original IGBT approach;

New combined 6.5kV and 10kV IGBT/MOSFET lot is in the line (4-inch)
- Life-time enhancement;
- Optimized unit cell structure;
- Improved shielding of gate oxide;
- To be completed and tested;

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