4H-SiC MOSFETs with: (i) Phosphosilicate glass gate dielectric (ii) Surface counter-doping with Sb

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Channel mobility problem in SiC power MOSFETs

- Channel mobility in commercial MOSFETs low $\sim$20 cm$^2$ V$^{-1}$ s$^{-1}$
- Channel can contribute up to 50% of total on-resistance
- Higher mobility $\rightarrow$ Smaller chip size, lower operating oxide fields, less design constraints, lower blocking voltages etc.

\[ R_{\text{channel}} \propto \frac{1}{\mu_{\text{channel}}} \]
SiO$_2$-4H-SiC interface traps

Nano-scale imperfections and defects at/near the SiO$_2$/SiC interface

\[ J = \sigma E = q n \mu E \]

- Interface traps reduce both \( n \) and \( \mu \) by trapping and Coulomb scattering

\[
4H-SiC \begin{cases} 
N_{it} \sim 10^{13} \text{ cm}^{-2} & \text{(as-oxidized, without passivation)} \\
\frac{\mu_{ch}}{\mu_{bulk}} \approx 1\% \end{cases}
\]

Interface trap passivation

**As-oxidized**

**NO annealed**

- Ideal model: Slope = $C_{ox}/q$

- Measured:
  - Slope $\ll C_{ox}/q$

- **As-ox:** >90% free e- remain trapped
- **NO:** Reduction of trap density: $>10^{13}$ cm$^{-2}$ → $\sim 10^{12}$ cm$^{-2}$

- **Ideal model:** Slope = $C_{ox}/q$
- **Measured slope:** ≈ $C_{ox}/q$

- **NO annealing:** $t_{ox}$ = 550 A

- **1175°C NO annealing**

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- **Interface trap passivation**
Si MOSFET: ‘Universal’ mobility behavior

\[
\frac{1}{\mu_{\text{ch}}} = \frac{1}{\mu_{\text{phonon}}} + \frac{1}{\mu_{\text{coulomb}}} + \frac{1}{\mu_{\text{SR}}}
\]

Takagi et al., IEEE TED, 12, 2357 (1994)

- Low electron density \(n\): Coulomb scattering
- Moderate \(n\), moderate temperature: Phonon scattering
- High \(n\): Surface roughness scattering
Mobility in NO annealed 4H-SiC MOSFET

$S. \text{ Dhar et al., ICSCRM (2011)}$

$T < 373 \text{ K, } T \uparrow \mu \uparrow$
- Coulomb scattering
- Thermally activated transport

$T > 400 \text{ K, } T \uparrow \mu \downarrow$
- Coulomb scattering at low fields
- Phonon and surface roughness scattering at high $E$ fields

$1175^{\circ}C \text{ NO}$
$t_{ox} = 550 \text{ A}$

No $n$ dependence

$\propto T^1$

Hall Mobility (cm$^2$ V$^{-1}$ s$^{-1}$)
Temperature (K)

- $n_s$: 7.4E11 cm$^{-2}$
- $n_s$: 1.4E12 cm$^{-2}$
- $n_s$: 4.0E12 cm$^{-2}$
- $n_s$: 5.0E12 cm$^{-2}$
Summary of 4H-SiC MOS interface treatments

THIS TALK

- Group I: Hydrogen/wet anneals: $\mu \approx 200 \text{ cm}^2 \text{ V}^{-1} \text{s}^{-1}$, weakly bonded, instability
  - Na, K: $\mu \approx 200 \text{ cm}^2 \text{ V}^{-1} \text{s}^{-1}$, heavy instability (mid 2000s, Chalmers Univ., Sweden)
  - Cs, Rb: $\mu \approx 40 \text{ cm}^2 \text{ V}^{-1} \text{s}^{-1}$, high $D_{it}$, Lichtenwalner et al., Appl. Phys. Lett. (2014)

- Group II: Alkaline earth metals
  - Ca, Ba, Sr (oxide interlayers): $\mu \approx 90 \text{ cm}^2 \text{ V}^{-1} \text{s}^{-1}$, low $D_{it}$, Lichtenwalner et al., Appl. Phys. Lett. (2014)

- Group III: B (Borosilicate glass): $\mu \approx 100 \text{ cm}^2 \text{ V}^{-1} \text{s}^{-1}$, low $D_{it}$, Okamoto et al., IEEE EDL, (2014)

- Group V: N (Various processes): $\mu \approx 35 \text{ cm}^2 \text{ V}^{-1} \text{s}^{-1}$, low $D_{it}$, most reliable oxide

Most widely studied SiC MOS system 2000-2014

- P (Phosphoslicate glass): $\mu \approx 100 \text{ cm}^2 \text{ V}^{-1} \text{s}^{-1}$, low $D_{it}$, poor long term stability
  - Okamoto et al., IEEE EDL, (2010)

- Sb (surface doping) + N: $\mu \approx 100 \text{ cm}^2 \text{ V}^{-1} \text{s}^{-1}$, low $D_{it}$, technologically promising
  - Modic et al., IEEE EDL, (2014)
Scaling between interface trap density and mobility

\[ \frac{1}{\mu_{ch}} = \frac{1}{\mu_{phonon}} + \frac{1}{\mu_{coulomb}} + \frac{1}{\mu_{SR}} \]

- NO annealing: Most established trap passivation method
- \( \mu \) scales with number of interface traps (Rozen et al. IEEE TED, 2011)
- Trapping and Coulomb scattering limited at low gate voltages
Recent Results: Non-scaling between trapping and mobility

\[
\frac{1}{\mu_{\text{ch}}} = \frac{1}{\mu_{\text{phonon}}} + \frac{1}{\mu_{\text{coulomb}}} + \frac{1}{\mu_{\text{SR}}}
\]

- Surface counter doping by N and P
- Inaccurate \( D_{\text{it}} \) measurements as ‘fast traps’ not included. (Yoshioka et al., J. Appl. Phys., 2012)
Nitridation and phosphorus treatments lead to unintentional surface counter-doping.
‘Fast states’ and the $C-\psi_s$ method

Generation of very fast states by nitridation of the SiO$_2$/SiC interface

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Fast states at SiO$_2$/SiC interfaces annealed in NO at 1150–1350 °C have been investigated. The response frequency of the interface states was measured by the conductance method with a maximum frequency of 100 MHz. The interface state density was evaluated based on the difference between quasi-static and theoretical capacitances ($C-\psi_s$ method). Very fast states, which are not observed in as-oxidized samples, were generated by NO annealing, while states existing at an as-oxidized interface decreased by approximately 90%. The response frequency of the very fast states was higher than 1 MHz and increased when the energy level approaches the conduction band edge. For example, the response frequency (time) was 100 MHz (5 ns) at $E_C-E_T=0.4$ eV and room temperature. The SiO$_2$/SiC interface annealed in NO at 1250 °C showed the lowest interface state density, and NO annealing at a temperature higher than 1250 °C is not effective because of the increase in the very fast states. © 2012 American Institute of Physics.

[http://dx.doi.org/10.1063/1.4740068]
What is PSG?

\[ \text{SiO}_2 + \text{P}_2\text{O}_5 \rightarrow (\text{P}_2\text{O}_5)_x(\text{SiO}_2)_{1-x} \]

Advantages and disadvantages:

- Low \( D_{it} \)
- High \( \mu_{fe} \)
- Instability
  - Polarization at low E-field stress
  - Electron/hole trapping at high E-field stress
Phosphosilicate glass (PSG) formation process

\[ 4\text{POCl}_3 + 3\text{O}_2 \rightarrow 2\text{P}_2\text{O}_5 + 6\text{Cl}_2 \]

**Condition:**

Maintain \(\text{POCl}_3\) at 15°C; bubble through by \(\text{N}_2\);
Anneal at 900~1100°C (15min) flowing \(\text{O}_2\);
Post anneal (drive-in, 30min) with \(\text{N}_2\) at same temperature as annealing.

Allows the study of annealing temperature variation
Phosphorus uptake with temperature variation

![Graph showing phosphorus uptake with temperature variation. The x-axis represents annealing temperature (°C) ranging from 900 to 1100. The y-axis represents phosphorus interface coverage and bulk percentage. The graph shows a decrease in both parameters as the temperature increases.]

Courtesy: C. Xu and L.C. Feldman, Rutgers Univ.
Reason for different P uptake

\[(\text{P}_2\text{O}_5)_x \ (\text{SiO}_2)_{1-x}\]

<table>
<thead>
<tr>
<th>POCl$_3$ temp</th>
<th>Bulk P percent (%)</th>
<th>$x$ value</th>
</tr>
</thead>
<tbody>
<tr>
<td>900°C</td>
<td>6.7</td>
<td>0.115</td>
</tr>
<tr>
<td>950°C</td>
<td>5.2</td>
<td>0.087</td>
</tr>
<tr>
<td>1000°C</td>
<td>4.6</td>
<td>0.076</td>
</tr>
<tr>
<td>1050°C</td>
<td>4.6</td>
<td>0.076</td>
</tr>
<tr>
<td>1100°C</td>
<td>4.2</td>
<td>0.069</td>
</tr>
</tbody>
</table>

During the drive-in annealing, some P$_2$O$_5$ is lost to the gas phase by evaporation.

Interface traps correlation with P coverage

$C-\psi_s$ characterization

Taking ‘fast states’ into account, higher P coverage leads to lower $D_{it}$

Courtesy: $C-\psi_s$ code provided by D. Morisette, Purdue Univ.
PSG: Lower density of ‘fast traps’

Low temperature G-ω measurement

Wei-Chieh Kao et al., Semiconductor Science and Tech., 2015
PSG Instability

1000 °C PSG

Capacitance (F)

Voltage (V)

\[ \Delta V \sim -2.9 V \]

1100 °C PSG

Capacitance (F)

Voltage (V)

\[ \Delta V \sim 0.65 V \]

BTS condition: 150°C, +1.5MV/cm, 5 min
Two competing mechanisms of instability: trapping and polarization

BTS: \[ qN_{\text{net}} = q(N_{\text{trp}} - N_{\text{pol}}) = C_{\text{ox}} \times \Delta V_{\text{FB}} \] (1)

Relaxation (20 days): \[ N_{\text{pol}} \approx 0, \quad qN_{\text{trp}} = C_{\text{ox}} \times \Delta V_{\text{FB}} \] (2)

(assumption: electron trapping relaxes much slower than polarization)

Devices with 1 h BTS:

<table>
<thead>
<tr>
<th>T (°C)</th>
<th>( N_{\text{pol}} (\times 10^{12} \text{ cm}^{-2}) )</th>
<th>( N_{\text{trp}} (\times 10^{12} \text{ cm}^{-2}) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000</td>
<td>1.23</td>
<td>0.77</td>
</tr>
<tr>
<td>1050</td>
<td>0.40~0.66</td>
<td>0.60~1.45</td>
</tr>
<tr>
<td>1100</td>
<td>0.32</td>
<td>0.88</td>
</tr>
</tbody>
</table>

Polarization scales with phosphorus uptake.
Field-effect mobility $\mu_{fe}$ dependence on $P$

At high E-field, mobility of 1000°C PSG is highest.

Possible reason: Trade-off between trap passivation and counter-doping

$L = 150\mu m$, $W = 290\mu m$
Temperature dependence of mobility: PSG

\[
\frac{1}{\mu} = \frac{1}{\mu_c} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_{sp}}
\]

- \(\mu_c\): \(T \uparrow, \mu_c \uparrow\)
- \(\mu_{sp}\): \(T \uparrow, \mu_{sp} \downarrow\)
- \(\mu_{sr}\): weak \(T\) dependence

MOSFET (900°C) mobility from 80K to 250K. The arrow represents the rising of ambient temperature.

MOSFET (1100°C) mobility from 100K to 400K. The arrow represents the rising of ambient temperature.
PSG Summary

- POCI$_3$ annealing temperature variation causes different P interface coverage
- Correlation: higher P coverage results in lower $D_{it}$
- Two competing mechanisms of instability identified: trapping and polarization. Polarization charge scales with P uptake.
- Correlation between P coverage and $\mu_{fe}$ needs further investigation
- Temperature dependence of $\mu_{fe}$ shows different limiting mechanisms: Coulomb scattering $\mu_c$ and surface roughness scattering $\mu_{sr}$.
Separation of trap passivation and counter-doping effects

• Difficult to investigate using N or P as they result in both effects

• Heavier dopants (As, Sb) not expected to chemically passivate dangling bonds

• Surface counter-doping with Sb
Effects of surface counter-doping

- Higher carrier density at same $E_\perp$
- Less traps filled at $V_T$ due to less band-bending, efficient screening ($\mu_C \uparrow$)
- $E_\perp \downarrow \rightarrow \mu_{SR} \uparrow$ for same carrier density

- Ideally $V_T$ reduction is smaller as counter-doping thickness is reduced
- In practice, $V_T$ determined by combination of doping and interface charge
Sb surface doping process

80 keV, 2.2E13 cm\(^{-2}\) Sb\(^+\)

Activation 1550°C

~100 Å Sb counter-doping

Controlled oxidation

SIMS

Sb concentration (atoms/cm\(^3\))

Post activation anneal

SRIM simulation

Source

Gate

Drain

Oxide

p-type SiC
Sb profile after oxidation

- ~75% of Sb lost during oxidation
- Total interfacial amount: ~5.7E12 cm\(^{-2}\)
- Total activated amount: ~10%
- Width of profile limited by depth resolution of SIMS. Layer < 10 nm
- No crystal damage detected by ion scattering

**Graphical Elements**

- SiO\(_2\)
- SiC
- FWHM ~10 nm
Surface counter-doping results

**Graph: Field-effect mobility**
- **p-well:** $6E15 \text{ cm}^{-3}$
- **T=300 K**
- **Sb+NO**
- **NO**
- **Sb**

**Table: Sample Characteristics**

<table>
<thead>
<tr>
<th>Sample</th>
<th>Oxide Thickness (NM)</th>
<th>Threshold voltage (V)</th>
<th>$\mu_{FE, max}$ (cm$^2$ V$^{-1}$ s$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NO</td>
<td>60</td>
<td>2.0</td>
<td>32</td>
</tr>
<tr>
<td>Sb</td>
<td>65</td>
<td>1.5</td>
<td>80</td>
</tr>
<tr>
<td>Sb+NO</td>
<td>80</td>
<td>1.1</td>
<td>110</td>
</tr>
</tbody>
</table>
Sb acts as a dopant but does not passivate traps

Low temperature

High temperature
Temperature dependence of ‘Sb+NO’ mobility

- Low field performance at high temperature better than NO
- High field performance at higher temperature similar to NO
- Low temperature behavior same as NO
‘Universal’ mobility behavior for NO annealed interfaces
‘Sb+NO’: Threshold voltage stability
Sb process applied to heavier doped p-wells:

<table>
<thead>
<tr>
<th>P-body doping</th>
<th>Standard NO(no Sb)</th>
<th>Sb 2.5E13cm⁻²</th>
<th>Sb 5E13cm⁻²</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al 1E17</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Al 5E17</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Al Implant concentration 1e17/cm³: mask Mo 1000 A, SiO₂ 150 A
Sb process applied to heavier doped p-wells:

P-well: $1E17$ cm$^{-3}$, tox: $\sim60$ nm

Main advantage of surface counter-doping: Higher sub-threshold slope
Sb process applied to heavier doped p-wells:

- P-well: $5 \times 10^{17} \text{ cm}^{-3}$, tox: $\sim 60 \text{ nm}$

- Higher S can be obtained on heavy p-wells
- Process optimization: Uneven activation/loss of Sb
Summary

• Highlights of recent SiC MOS channel engineering results presented
• Transport limited by ‘fast traps’ and ‘surface roughness’
• Details of these mechanisms not clear
• ‘Universal’ mobility behavior in SiC MOSFETs identified
• PSG is a unique model system to study channel transport with minimal effects of trapping
• Surface counter-doping processes have strong potential for threshold voltage control and sub-threshold slope improvement in practical MOSFETs
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