High mobility 4H-SiC MOSFET using a combination of counter-doping and interface trap passivation

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Motivation: Interface traps may not be the only mobility limiting factor!

[Diagram showing energy levels and interface traps]
Counter-doping


- n-type counter-doped layer is normally off due to depletion from backside p-n junction since it is thin.
- Positive gate voltage allows for carriers, forming a channel between source and drain.
- Higher carrier density at same applied E-field.
- Less traps filled at $V_T$ due to less band-bending.
- More Coulomb screening.
- $E\text{-field } \downarrow \rightarrow \mu_{SR} \uparrow$ for same carrier density.
Threshold reduction due to counter-doping

Counter-doping charge
\[ N_d x_d = 10^{12} \text{ cm}^{-2} \]

- Threshold reduction is less as counter-doped layer thickness is decreased

Courtesy: Dr. Yuming Zhou (AU)
Surface counter-doping

Fiorenza et al. APL, 103, 153508 (2013)

- Nitridation and phosphorus treatments lead to unintentional thin counter-doped layers
Arsenic and Antimony Motivation

- N,P: trap passivation and counter-doping
- As, Sb: counter-doping only
Sb and As surface doping process

60keV 2.2E13 cm\(^{-2}\) As\(^+\)
80 keV, 2.2E13 cm\(^{-2}\) Sb\(^+\)

Activation 1550C

Controlled oxidation

\(~100\) A Sb counter-doping
Antimony profile

- Antimony pile-up at interface
- Antimony is lost during oxidation
- Activated antimony percent unknown

SIMS detection limit is \(\sim 5 \times 10^{17}\) atoms/cm\(^3\)
High field-effect mobility Sb+NO

MOSFET p-well doping: $6 \times 10^{15}$ cm$^{-3}$

<table>
<thead>
<tr>
<th>Process</th>
<th>Threshold Voltage (V)</th>
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<tbody>
<tr>
<td>NO</td>
<td>2</td>
</tr>
<tr>
<td>Sb</td>
<td>1.5</td>
</tr>
<tr>
<td>Sb+NO</td>
<td>1</td>
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</tbody>
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Field-Effect mobility (cm$^2$V$^{-1}$s$^{-1}$)

Oxide Field (MV/cm)

T = 300 K

- Sb+NO
- Sb
- NO
Temperature effects on mobility

(1) Sb : Counter-doping
(2) NO: Trap passivation
Sb does not passivate interface traps

Sb only

\[ \Delta V_{FB} = 9 \text{V} \]

NO

\[ \Delta V_{FB} = 1.5 \text{V} \]

Sb mobility pure counter-doping effect
CCDLTS Spectra: Sb-Implanted and NO-30 Samples

Contributed by A. Basile, P. Mooney
Simon-Fraser University

- CCDLTS spectra for an Sb-implanted 4H-SiC MOS capacitor (black) and a capacitor NO-annealed for 30 min (red) showing near-interface oxide traps O1 and O2 in both devices.

- A signal from near-interface traps on the SiC side of the interface (B1) overlaps the O1 trap signal in NO-annealed capacitors.

- The absence of the B1 traps in Sb-implanted devices accounts for the lower CCDLTS signal at 100K.

CCDLTS measurements confirm that Sb does not passivate near-interface oxide traps.
High temperature mobility

Sb+NO max $\mu_{FE}$ decrease with increased T attributed to phonon scattering
Summary

• Sb and As counter-doping leads to high transconductance devices

• Sb process allows separation of counter-doping and trap passivation effect on mobility

• Sb and As counter-doping impact on DMOSFET?

• Process has a potential advantage for improvement of sub-threshold slope and threshold voltage control
Thank you
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Back up Slides
Future Work

• Quantification of As and Sb as a function of oxide thickness using SIMS (Rutgers)

• Sb+NO on heavier doped p-well (Yongju, Auburn)

• Activated percent of Ab and As?

• Use of C-ψs analysis and simulation of CV curves for non-uniformly doped samples (Purdue?)

• Determination of Sb ionization energy in 4H-SiC (Simon-Fraser University)
High temperature effects on mobility

High temperature reduces mobility more with counter-doping than passivation. Phonon scattering effect with high carrier concentration?
Low temperature mobility

Sb only

Sb+NO
• Since all the methods of present study result in similar effective mobility at operating $E_{ox} \sim 4\text{MV/cm}$, it is better to increase threshold voltage $V_t$ to about 5V, high enough to provide safe normally-off operation at elevated temperatures and immunity from $dV/dt$ related false turn-on;

• This will enable a unipolar gate drive, 0V … +25V, without the need for negative turn-off bias and eliminating concerns over any NBTS-related $V_t$ instabilities ;

• Better transconductance is desirable than with NO-process for faster switching
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Antimony I-V Breakdown
$I_d$-$V_g$ threshold $E_{ox}$ comparison
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