georgezaki@gmail.com **George F. Zaki** Cell: (301) 979-2981

Objective: To use my research and professional knowledge in advancing development and innovation in science and technology while expanding my technical and professional skill base.

Education:

- **University of Maryland at College Park, Electrical and Computer Engineering Department, MD, USA**
  - **Ph. D.**, GPA: 4.0 May 2013
    Thesis titled: "*Scalable Techniques for Scheduling and Mapping DSP Applications onto Embedded Mutliprocessor Platforms*"
  - **M.S.**, GPA: 4.0 Dec. 2012
- **Cairo University, Electronics and Electrical Communications Department, Cairo, Egypt**
  - **M.S.**, Cumulative grade: 92.2% Oct. 2008
    1st out of a class of 50 students
    Thesis titled: "*Hybrid Data Gathering Method for Wireless Sensor Networks"*
  - **B.S.**, Cumulative grade: 92.4% May 2005
    5th out of a class of 550 students

Graduate Courses:

Technology Law Seminar; Simulation of Discrete-Event Systems; Compilers and Optimization; High Performance Computing; Advanced Digital Signals Processing; Mathematical Foundation for Computer Engineering; Computer Aided Design for Digital Systems; Design of Distributed Computer Systems; Computer Architecture; VLSI System Design; Data Communication and Computer Networks; Real Time Systems; Project Risk Management; Random Processes in Communication and Control

Professional Experience:

Chief Science Officer: IGI Technologies Inc., Maryland Jan. 2013 – present

- Designed and implemented an OpenMP acceleration for the subvolume division algorithm for automatic medical image registration. The multi-core implementation achieves a near linear speedup of 3x on Intel's four cores i7 CPU. ***(OpenMP)***
- Assisted in business plan preparation and pitched to multiple angel investors and potential collaborators at leading technology conference (GTC 2014) and medical conference (AdvaMed 2014).
- Participated in the DC NIH I-Corps course and assisted in preparation of the business model canvas for an augmented reality technology in laparoscopic surgeries. During the course, I assisted in iterating the definition of the value proposition and customer discovery by participating in interviewing over 50 possible customers including surgeons, IP experts, and hospital department chairs.
- Accelerated and refactored the implementation of multiple modules for a state of the art medical image registration algorithm on Graphics Processing Units (GPUs) using CUDA. The accelerated modules reduced the total registration time by 50%. ***(CUDA)***
- Built and scheduled an automated parameters space exploration engine for a medical image registration algorithm in order to fine tune the engine to target different medical applications. ***(Python, Shell, CUDA)***
- Designed and implemented unit tests for different GPU accelerated modules. The unit tests facilitated correctness check and software bugs' discovery for multiple versions of the refactored code for these modules. **(CUDA, Shell)**
- Integrated the medical registration algorithm with clinical software with the collaboration of Johns Hopkins University Hospital. ***(Slicer)***
- Implemented different image processing utilities for different image and signal processing tasks. The new set of utilities facilitated the testing of different application and generated multiple performance metrics. ***(VTK, ITK, C++, Python)***
- Developed a server plugin for online job submission and scheduling to register medical images on demand. ***(PHP, SQL, Shell scripting, HTML)***

Adjunct Faculty (Part Time): University of Maryland, College Park Jan. 2014 – present

- Prepared and taught the digital system design course with the collaboration of the DSPCAD research group. The course was offered for professional master students enrolled with the office of advanced engineering education and Ph.D. students in the computer engineering department at UMD. ***(Embedded Systems, Verilog, CUDA, Multicore)***

Research Experience:

Graduate Research Assistant (*Texas Instruments Scholar*), University of Maryland Sept. 2008 – Jan. 2013

- Designed and scheduled an implementation model called the Partial Expansion Graphs (PEGs) for dynamic embedded system realization on multicore platforms. The model explores the design space to express the right amount of parallelism that exists in the application graph. The scheduler maps the PEG to the available cores to make use of data, task and pipeline parallelism and by taking into consideration the computation to communication ratio. (***JAVA, C***)

- Developed a workflow to vectorize and map software defined radio applications on heterogeneous multiprocessor platforms consisting of NVIDIA's GPU and Intel's GPP equipped with vector processing units. ***(JAVA, MathProg)***
- Used Data Flow Modeling to implement software defined radio systems on a NVIDIA's GPU architecture towards the goal of generalizing mapping to parallel platforms. ***(CUDA)***
- Developed a cross platform unit testing framework for the functional DIF data flow description language. The new package reduced the time required to test a complete project for High Energy Physics applications. (***C / C++, JAVA***)

Graduate Teaching and Research Assistant, Cairo University and the American University in Cairo
Oct. 2005 – Aug. 2008

- Developed a new algorithm for data routing for mobile sink wireless sensor networks. Increased the network lifetime and performed energy balancing by making the best decision of the optimum path. (***OPNET, MATLAB***)
- Guided a team of five to investigate the fault tolerance for the 802.3 protocol on board of train networks. Proved the coexistence of control data and entertainment traffic in terms of delay and throughput. (***C#, OPNET***)
- Implemented a face recognition / verification system on a FPGA. Used the HW / SW codesign methodology to partition the system functions between the embedded Nios processor and dedicated hardware module. Improved the system latency by 70% using 30% extra hardware. (***C, MATLAB, Verilog, VHDL***)

Additional Technical Skills: MPI, LINUX.

Additional Business Skills: Business Model, Pitch Preparation, Value Proposition, Customer Discovery, Lecturing, Assessment.

Awards:

- Clark School Future Faculty Fellow, Jan. 2012
- IEEE workshop on Signal Processing Systems SiPS 2011 Best Student Paper Award, Oct. 2011
- Texas Instruments Scholar, Jan. 2010-Jan. 2013
- Distinguished Teaching Assistant award, Department of Electrical and Computer Engineering University of Maryland College Park, 2009-2010
- Clark School of Engineering Distinguished Graduate Fellowship, University of Maryland College Park, 2008-2010
- First award of the IEDCS competition organized by the International Conference of Microelectronics ICM 2005
- IEEE Egypt student paper contest (First Place), 2005

Selected Publications:

- J. Tokuda, W. Plishker, M. Torabi, O. I. Olubiyi, **G. Zaki**, S. Tatli, S. G. Silverman, R. Shekher, and N. Hata. Graphics Processing Unit–Accelerated Nonrigid Registration of MR Images to CT Images During CT-Guided Percutaneous Liver Tumor Ablations. *Academic Radiology*, January 2015. DOI:10.1016/j.acra.2015.01.00
- **G. F. Zaki**, W. Plishker, S. Bhattacharyya, C. Clancy, and J. Kuykendall. Integration of Dataflow-based Heterogeneous Multiprocessor Scheduling Techniques in GNU Radio. *Journal of Signal Processing Systems*, *Springer*, 70(2):177-191, February 2013.
- **G. F. Zaki**, W. Plishker, S. Bhattacharyya, F. Fruth. Partial Expansion Graphs: Exposing Parallelism and Dynamic Scheduling Opportunities for DSP Applications. *In Proceedings of the International Conference on Application Specific Systems, Architectures and Processors*, Delft, Netherlands, July 2012.
- **G Zaki**, H. Elsayed, H. Amer and M. El-Soudani, Energy Balanced Model for Data Gathering in Wireless Sensor Networks with Fixed and Mobile Sinks, *In Proceeding of the International Conference on Computer Communication and Networks ICCCN 2009*, San Francisco, CA, August 2009.

Full list of publications are available on my website: http://www.ece.umd.edu/~gzaki/