Review For Second Midterm

Quine McCluskey.

1. Using Quine-McCluskey, obtain all the prime implicants for the following Boolean function $f(w,x,y,z) = \sum m(1,6,7,9,11,14,15) + dc(8,10)$

2. In 3−variable Quine−McClusky, how many comparisons are done in the first step of the algorithm assuming r number of minterms with zero 1's, s number of minterms with one 1, t number of minterms with two 1's and u number of minterms with three 1's.

Review For Second Midterm

MSI Components.

1. Consider the Boolean expression $f(w,x,y,z) = \sum m(1,2,4,5,9,12,13,15)$

Realize this Boolean expression using a 4-to-1 multiplexer and external gates. Let x, z appear on the select lines S_1, S_0 respectively.

2. Consider constructing a Borrow Lookahead Subtracter. I.e. precompute the borrow-out bit for the i-th digit.

Define the analogues of p_i, g_i for the Borrow Lookahead Subtracter. Give the formula for b_{i+1} in terms of $b_i, \mathrm{p_i}, \mathrm{g_i}$.

Review For Second Midterm

Implementing a Multiplexer Using a Decoder

Design a 4-to-1 multiplexer using a 2-to-4 decoder and additional logic gates.

- The circuit has four data inputs D_0, D_1, D_2, D_3, two select inputs S_1, S_0, and one output Y.
- The output should equal D_i when the binary value of S_1S_0 is i.

You may use one 2-to-4 decoder, AND gates, and OR gates. Draw the complete circuit, clearly labeling all connections.

Review For Second Midterm

Synthesis Problem. Design a 2-bit unsigned binary multiplier using one 4-bit adder and logic gates.

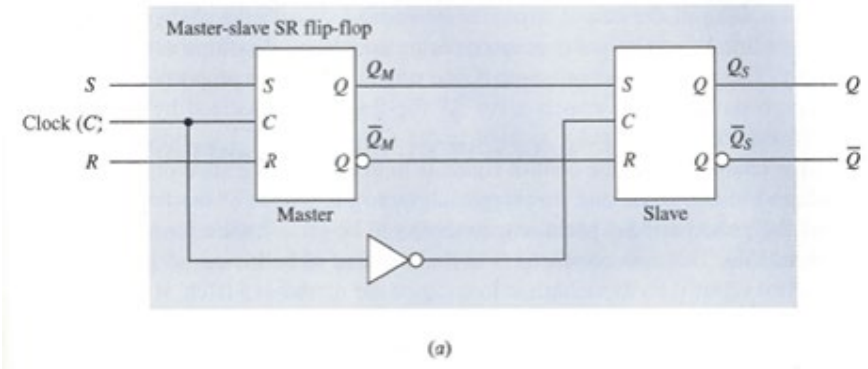
The circuit takes two 2-bit inputs, $A = (a_1, a_0)$ and $B = (b_1, b_0)$, and produces a 4-bit output $P = (p_3, p_2, p_1, p_0)$ representing their product.

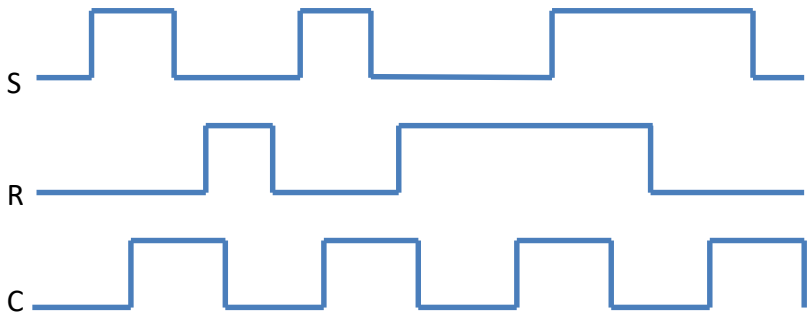
Draw a circuit diagram showing all logic gates, connections, and inputs to the 4-bit adder. You may assume that a 4-bit adder is available as a building block.

Review For Final

Latches and Flip-Flops.

1. The input signals below are applied to the leader-follower SR flip-flop (pictured below) when initially in its 0-state.Sketch the Q_M, $\overline{Q}_M$, Q_S and $\overline{Q}_S$ output signals. Assume all timing constraints are satisfied.





Review For Final

Latches and Flip-Flops.

2. The input signals below are applied to the leader-follower JK flip-flop (pictured below) when initially in its 0-state.Sketch the Q_M and Q_S output signals. Assume all timing constraints are satisfied.

