Digital Logic Design
ENEE 244-020x

Lecture 9

Announcements

- HW3 up on course webpage. Due on Saturday, Oct. 3 @11:59pm on Canvas/ELMS
- Release review problems by Friday 10/2
- Review session in class on Tuesday 10/6
- Exam 1 in class on Thursday 10/8

Agenda

- Last time
  - Using 3,4 variable K-Maps to find minimal expressions (3.2, 3.4)
  - Minimal expressions for incomplete Boolean functions (3.5)

- This time
  - 5 and 6 variable K-Maps
  - Gate Properties (2.8)

Five and Six Variable K-Maps

Five Variable K-Maps

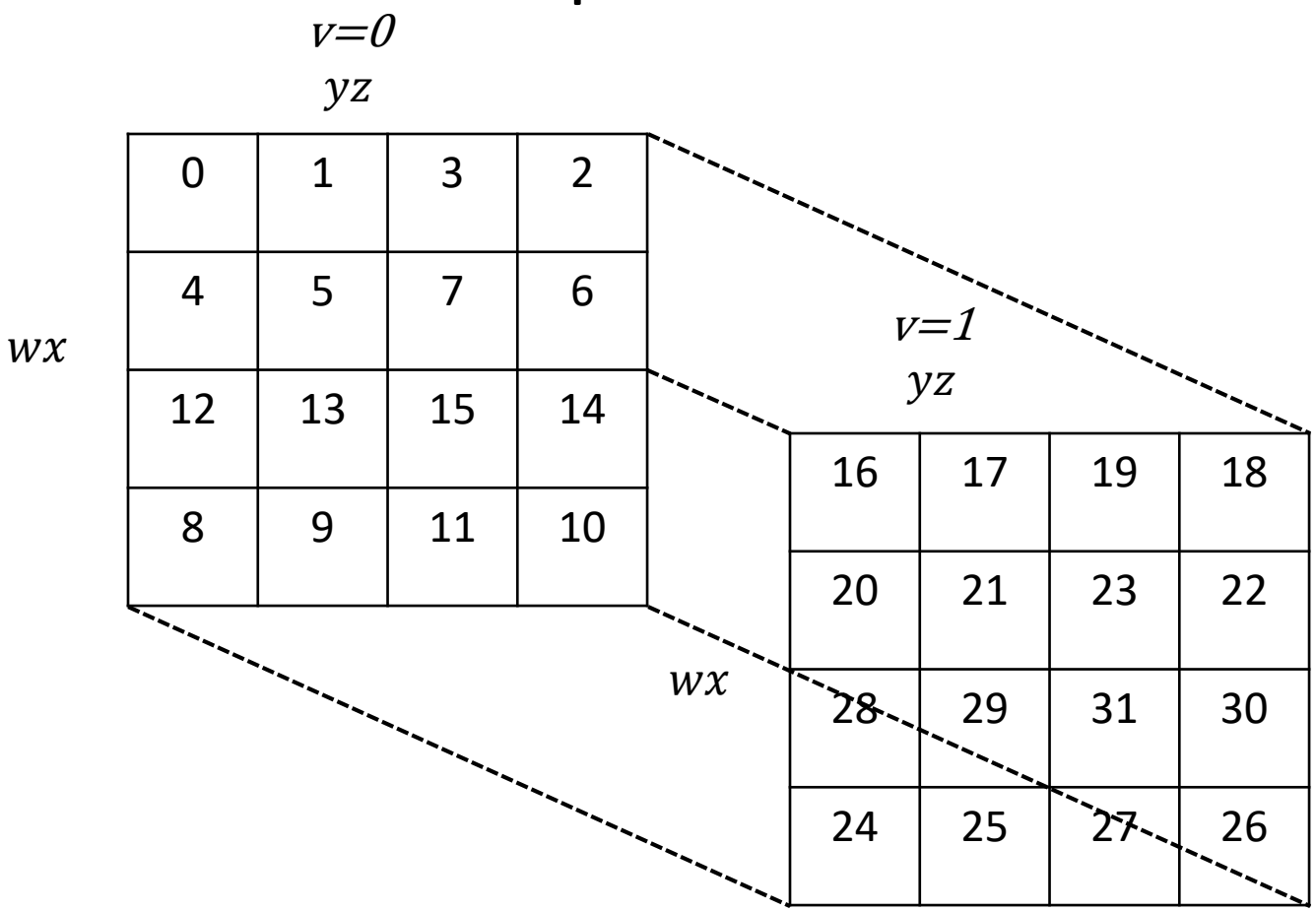
- We can visualize five-variable map in two different ways:

Five Variable K-Maps

vw \ xyz	000	001	011	010	110	111	101	100
00	0	1	3	2	6	7	5	4
01	8	9	11	10	14	15	13	12
11	24	25	27	26	30	31	29	28
10	16	17	19	18	22	23	21	20

Subcubes: Two subcubes are possible about the mirror-image line. If there are two rectangular groupings of the same $2^a \times 2^b$ dimensions on both halves and the two groupings are the mirror image of each other.

Five Variable K-Maps



Subcubes: If each layer contains a $2^a \times 2^b$ subcube such that they can be viewed as being directly above and below each other, then the two subcubes collectively form a single subcube consisting of 2^{a+b+1} cells.

Example

$$f(v,w,x,y,z) = \sum m(1,5,9,11,13,20,21,26,27,28,29,30,31)$$

v=0

yz

wx

0 0	1 1	3 0	2 0
4 0	5 1	7 0	6 0
12 0	13 1	15 0	14 0
8 0	9 1	11 1	10 0

v=1

yz

wx

16 0	17 0	19 0	18 0
20 1	21 1	23 0	22 0
28 1	29 1	31 1	30 1
24 0	25 0	27 1	26 1

Example

Step 1: Find all Prime Implicants.

$v=0$

yz

wx

0	1	0	0
0	1	0	0
0	1	0	0
0	1	1	0

$v=1$

yz

wx

0	0	0	0
1	1	0	0
1	1	1	1
0	0	1	1

Example

Step 2: Find all Essential Prime Implicants.

$v=0$

wx \ yz				
00	0	1	0	0
01	0	1	0	0
11	0	1	0	0
10	0	1	1	0

$v=1$

wx \ yz				
	0	0	0	0
	1	1	0	0
	1	1	1	1
	0	0	1	1

Essential Prime Implicants:

$v'y'z$

vxy'

vwy

Example

Step 2: Find all Essential Prime Implicants.

$v=0$

yz

wx

0	1	0	0
0	1	0	0
0	1	0	0
0	1	1	0

$v=1$

yz

wx

0	0	0	0
1	1	0	0
1	1	1	1
0	0	1	1

Essential Prime Implicants:

$v'y'z$

vxy'

vwy

Example

Step 2: Find all Essential Prime Implicants.

$v=0$

yz

wx

0	1	0	0
0	1	0	0
0	1	0	0
0	1	1	0

$v=1$

yz

0	0	0	0
1	1	0	0
1	1	1	1
0	0	1	1

wx

Final minimal DNF:

$v'y'z + vxy' + vwy + wx'yz$

Six Variable K-Maps

- We can visualize a six-variable map in two different ways:

Six Variable K-Maps

xyz

uvw	000	001	011	010	110	111	101	100
000	0	1	3	2	6	7	5	4
001	8	9	11	10	14	15	13	12
011	24	25	27	26	30	31	29	28
010	16	17	19	18	22	23	21	20
110	48	49	51	50	54	55	53	52
111	56	57	59	58	62	63	61	60
101	40	41	43	42	46	47	45	44
100	32	33	35	34	38	39	37	36

vwz

Subcubes: If each quadrant has a rectangular grouping of dimensions $2^a \times 2^b$ and each grouping is a mirror image of the other about both the horizontal and vertical mirror-image lines.

Six Variable K-Maps

uv=00

yz

0	1	3	2
4	5	7	6
12	13	15	14
8	9	11	10

wx

uv=01

yz

16	17	19	18
20	21	23	22
28	29	31	30
24	25	27	26

wx

uv=11

yz

48	49	51	50
52	53	55	54
60	61	63	62
56	57	59	58

wx

uv=10

yz

32	33	35	34
36	37	39	38
44	45	47	46
40	41	43	42

wx

$w'xy'z'$

Subcubes: Subcubes occurring in corresponding positions in consecutive layers collectively form a single subcube.

End of Exam 1 Material/
Beginning of Exam 2 Material

Gate Properties

Gate Properties

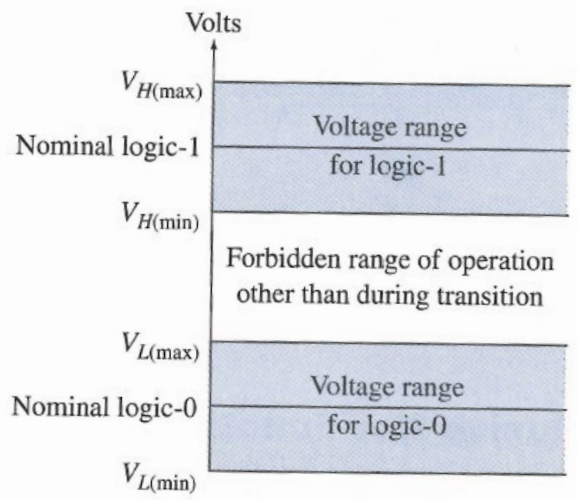
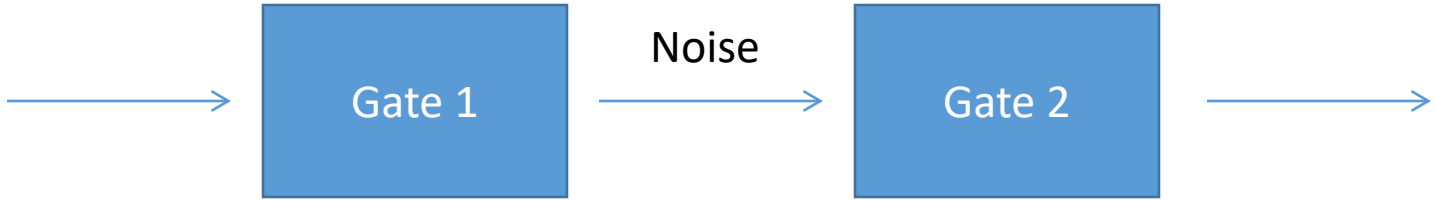


Figure 3.20 Voltage ranges of logic inputs for positive logic.

- The two signal values associated with logic-0 and logic-1 are actually ranges of values.
- If signal value is in some low-level voltage range between $V_{L(min)}$ and $V_{L(max)}$ then it is assigned to logic-0. When a signal value is in some high-level voltage range between $V_{H(min)}$ and $V_{H(max)}$ it is assigned to logic-1.

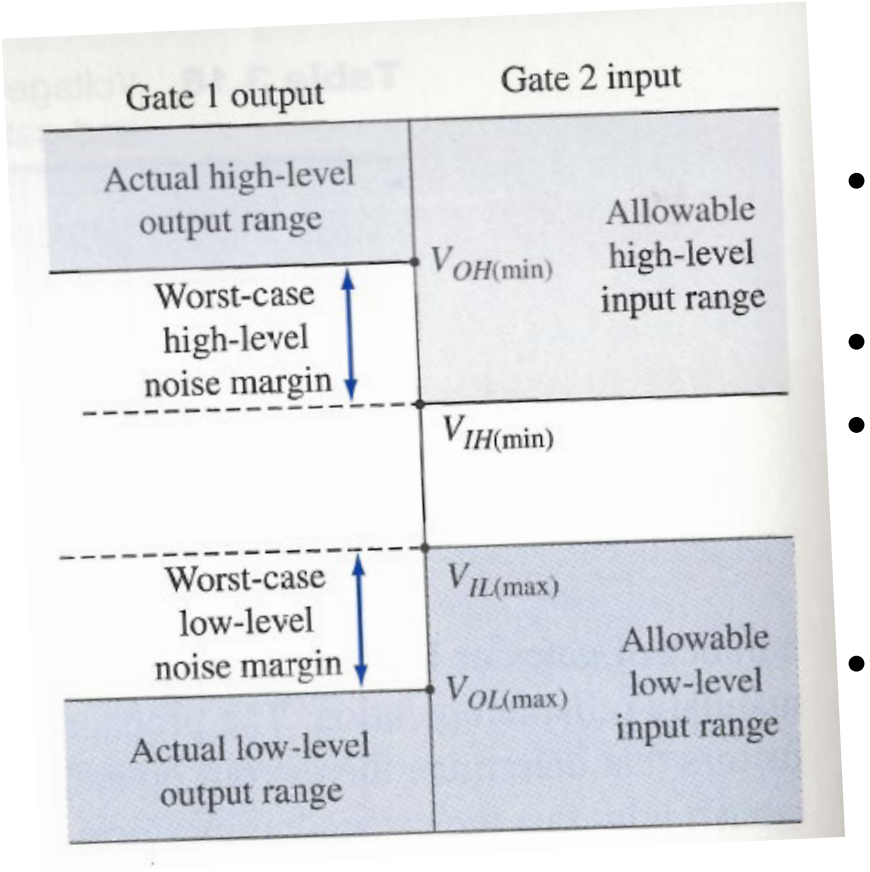
Noise Margins

- Noise: Random fluctuation in an electrical signal
- Must ensure circuit computes correctly even in the presence of noise.



- The minimal signal value that is acceptable as a logic-1 at the input to a gate is different from the minimal logic-1 signal value that a gate produces at its output.
- Assume output of Gate 1 is exactly at $V_{L(max)}$ and then noise increases the signal further. How will the signal be interpreted?
- Same situation with $V_{H(min)}$.

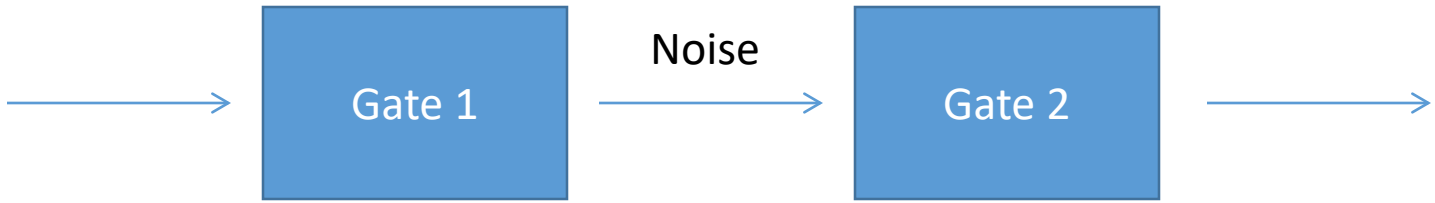
Noise Margins



- $V_{L(max)}$ is different for the input/output of a gate!
- Same situation with $V_{H(min)}$.
- Manufacturers normally state a $V_{IL(max)}, V_{IH(min)}, V_{OL(max)}, V_{OH(min)}$ in gate specifications.
- Where $V_{OL(max)} < V_{IL(max)} < V_{IH(min)}, < V_{OH(min)}$

Noise Margins

- Again consider connecting output of gate to another gate, where noise is induced between the two gates.



- Worst case low-level noise margin: Any noise less than $V_{IL(max)} - V_{OL(max)}$ does not affect behavior of Gate 2 on a low-level signal.
- Worst case high-level noise margin: Any noise less than $V_{OH(min)} - V_{IH(min)}$ does not affect behavior of Gate 2 on a high-level signal.

Fan-Out

- The signal value at the output of a gate is dependent upon the number of gates to which the output is connected.
- Limitation on number of gates output can connect to. This is known as the fan-out capability of the gate. Manufacturers specify this limitation.
- Circuits known as buffers serve as amplifiers for this purpose.

buffer

Propagation Delays

- Digital signals to not change instantaneously. Limitation to the overall speed of operation associated with a gate.
- These time delays are called propagation delays.
- Time required for output signal to change from high-level to low-level is t_{pHL}.
- Time required for output signal to change from low-level to high-level is t_{pLH}.
- t_{pHL} and t_{pLH} are, in general, not equal. Manufacturers give maximum times in gate specifications.
- General measure used is the average propagation delay time, t_{pd}

$$t_{pd} = \frac{t_{pHL}+t_{pLH}}{2}$$

Propagation Delay Times

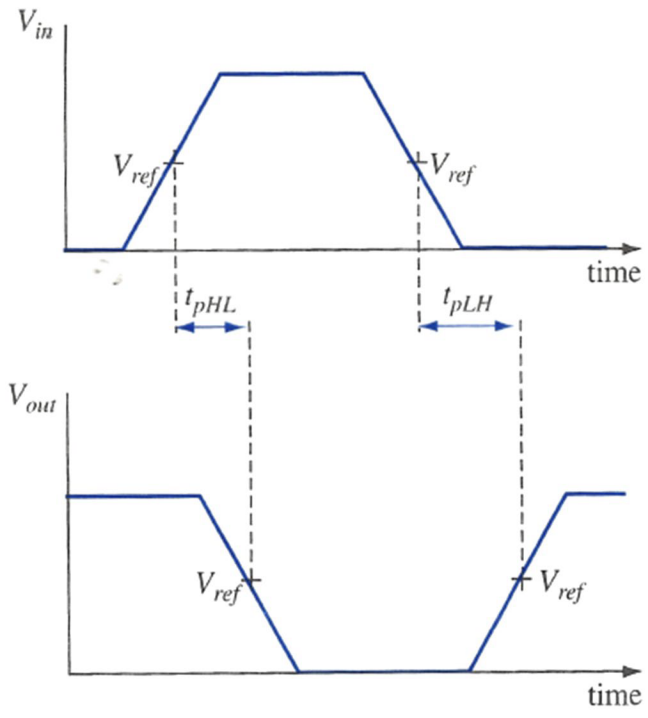


Figure 3.22 Propagation delay times.

t_{pHL}: Time required for output signal to change from high-level to low-level.

t_{pLH}: Time required for output signal to change from low-level to high-level.

Power Dissipation

- Digital circuit consumes power as a result of the flow of currents. Called power dissipation.
- Desirable to have low power dissipation and low propagation delay times.
- These two performance parameters are in conflict with each other.
- Common measure of gate performance is the product of the propagation delay and the power dissipation of the gate.
- This is known as the delay-power product.