Digital Logic Design
ENEE 244-020x

Lecture 16

Announcements

- Homework 5 due Sunday 11/8 @11:59pm
- Exam 2 postponed to Thursday, 11/12
  - Review sheet out, solutions posted by the end of the week.

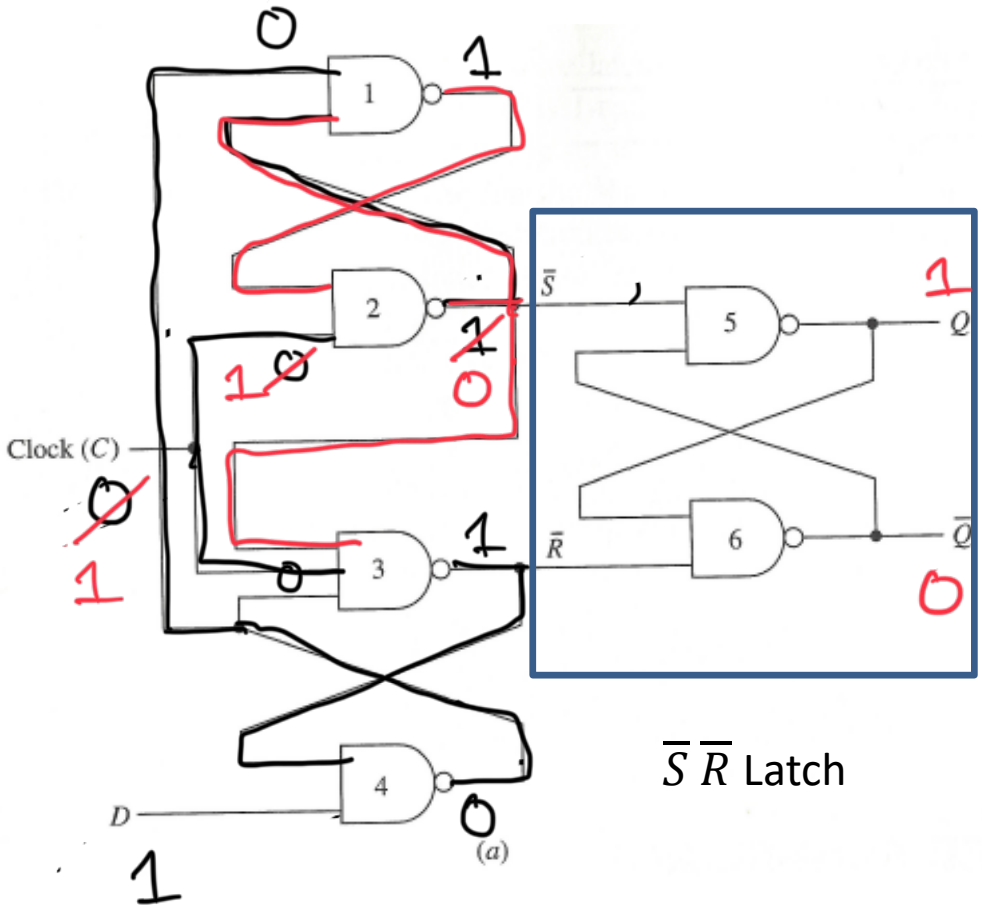
Agenda

- Last time:
  - Leader-Follower Flip-Flops (5.4)
- This time:
  - Edge-Triggered Flip-Flops (5.4)
  - Characteristic Equations (5.4)
- New topic: Synchronous Sequential Networks
  - Structure and Operation of Clocked Synchronous Sequential Networks (5.2)
  - Analysis of Clocked Synchronous Sequential Networks (5.5)
  - Modeling Clocked Synchronous Sequential Network Behavior (5.7-5.8)

Edge-Triggered Flip-Flops

- In basic leader-follower flip-flops, leader is enabled during the entire period the control input is 1.
  - This can result in 0's and 1's catching.
  - To avoid this, signals on information lines are restricted from changing during the time the leader is enabled.
  - Also a delay in the output since leader's state is established during the positive edge and transferred to the follower on the negative edge of clock.
- Edge-triggered flip-flops use just one of the edges of the clock signal.
  - This is referred to as the triggering edge.
- Response to triggering edge at the output of the flip-flop is almost immediate (depends only on propagation delay times).
- Once triggering occurs, flip-flop is unresponsive to information input changes until the next triggering edge.

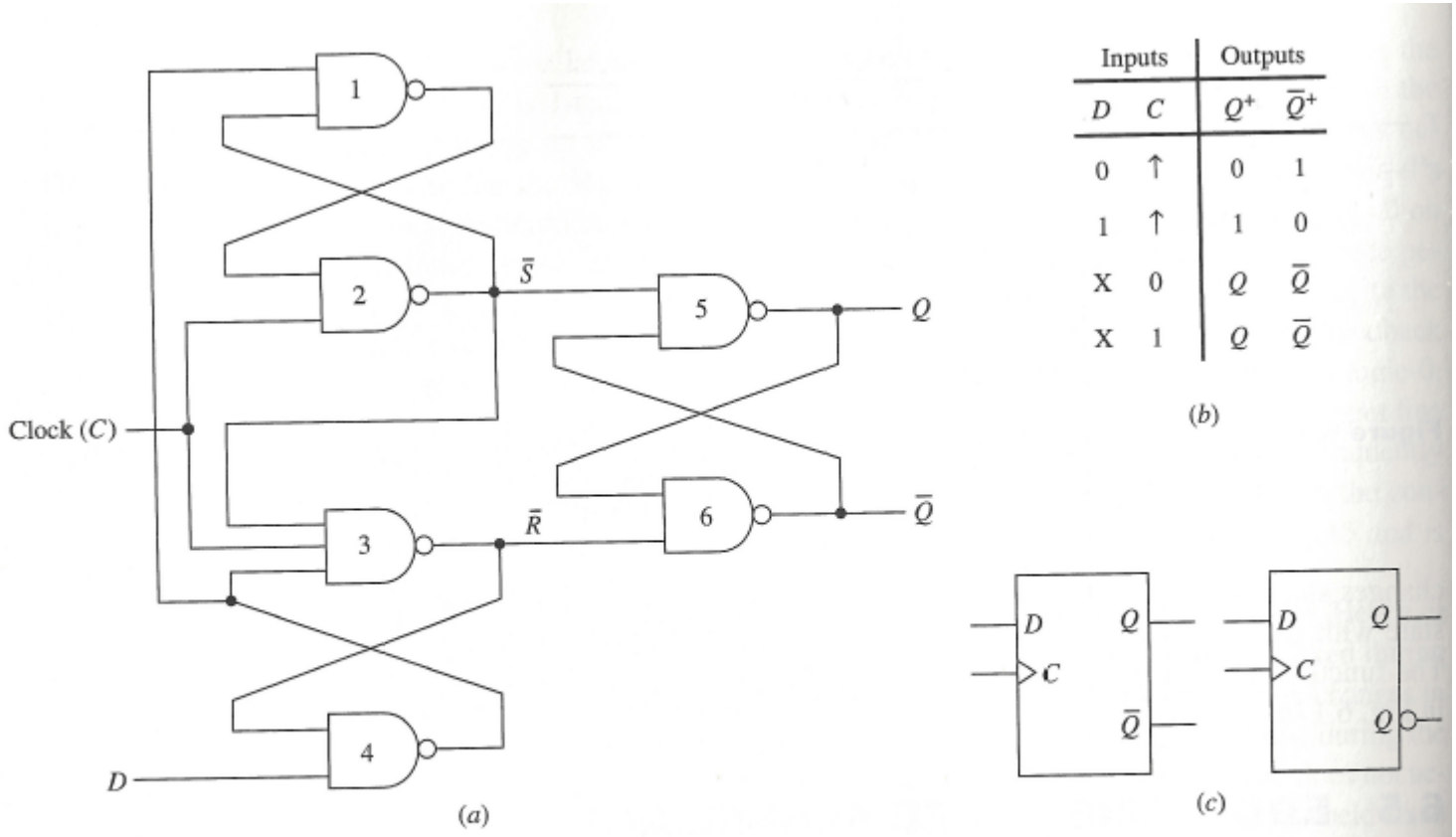
Edge-Triggered Flip-Flops



$\overline{S}\,\overline{R}$ Latch

1. C = 0. Regardless of input at D, outputs of gates 2,3 are 1. So $\overline{S} = \overline{R} = 1$. State of latch is held.
2. Assume D = 0: Output of gate 4 is 1, output of gate 1 is 0. When C goes to 1: all inputs to gate 3 are 1, output changes to 0. Output of gate 2 remains at 1 since output of gate 1 is 0. So $\overline{S} = 1, \overline{R} = 0$. Output of gate 3 (0) is fed to input of gate 4. Output of gate 4, gate 1 not affected by changes to D.
3. Assume C = 0, D = 1. Outputs of gates 2,3, are 1. Output of gate 4 is 0, output of gate 1 is 1. When C goes to 1: output of gate 2 is 0, output of gate 3 remains at 1. So $\overline{S} = 0, \overline{R} = 1$. Output from gate 2 is input to gates 1, 3 so their outputs remain at 1. Changes in D have no affect on state of flip-flop while C = 1.

Edge-Triggered Flip-Flops



Inputs		Outputs	
D	C	Q^+	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	Q	$\bar{Q}$
X	1	Q	$\bar{Q}$

Figure 6.18 Positive-edge-triggered D flip-flop. (*a*) Logic diagram.(*b*) Function table where Q^+ denotes the output Q in response to the inputs. (*c*) Two logic symbols.

Timing Diagram

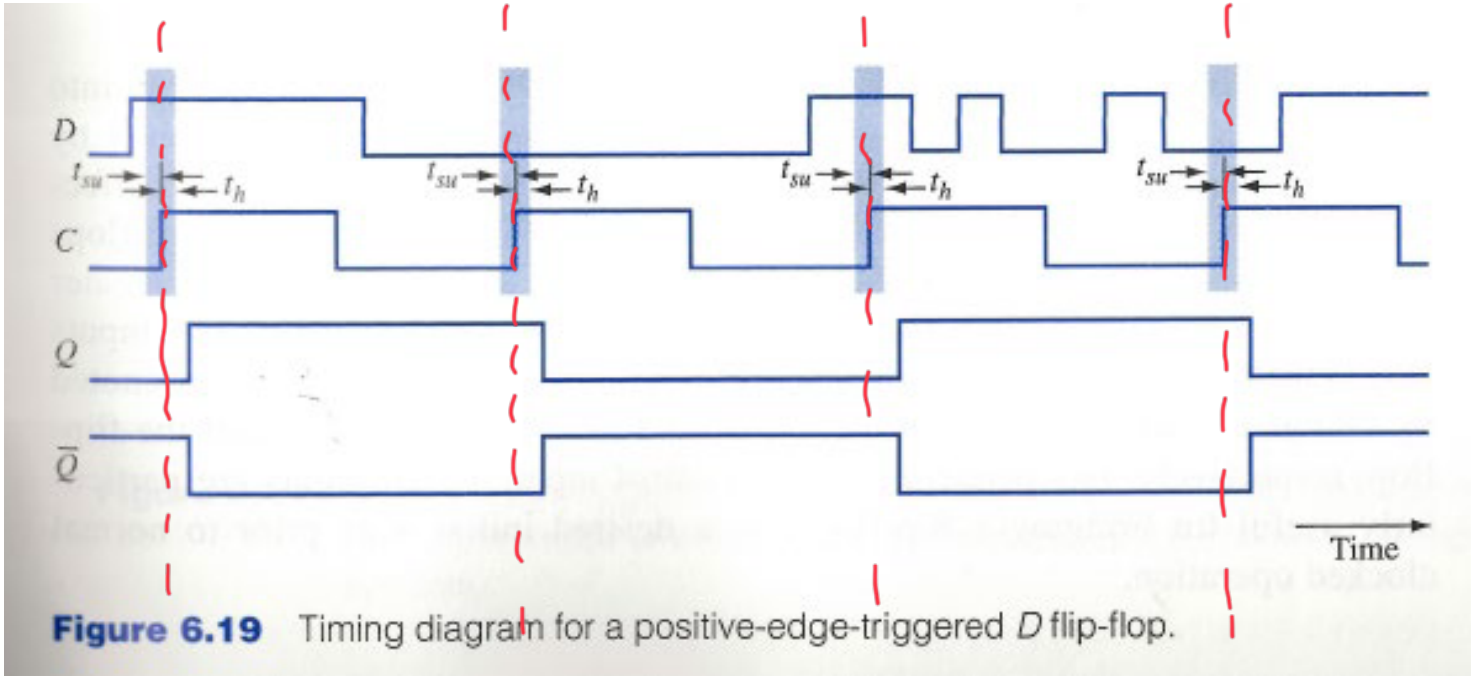
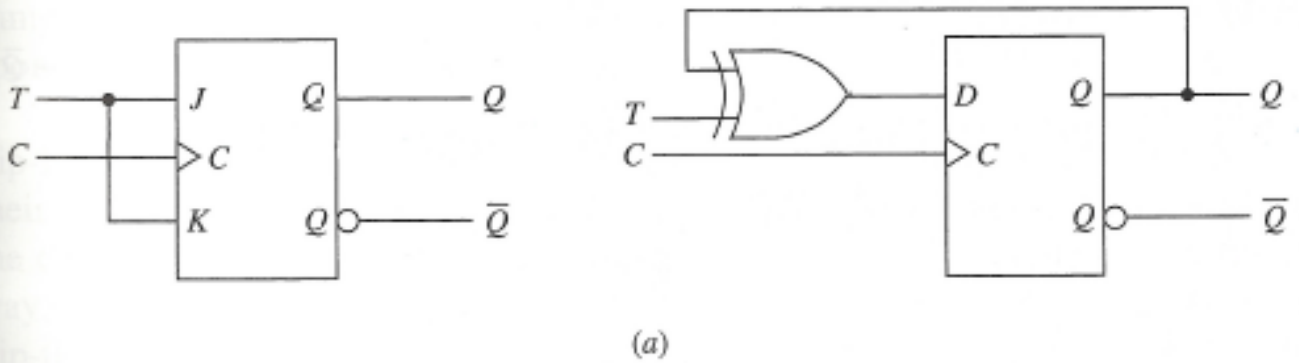


Figure 6.19 Timing diagram for a positive-edge-triggered *D* flip-flop.

During setup and hold times t_{su}, t_h with respect to the triggering edge of the clock, D input must not change.

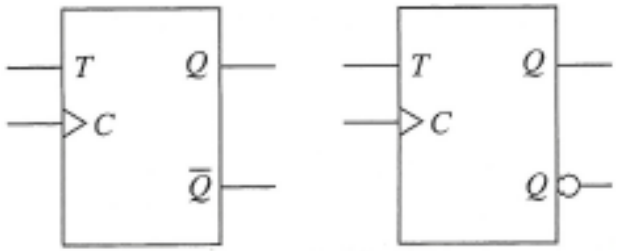
Positive-Edge Triggered T-Flip-Flop



(a)

Inputs		Outputs	
T	C	Q^+	$\overline{Q}^+$
0	↑	Q	$\overline{Q}$
1	↑	$\overline{Q}$	Q
X	0	Q	$\overline{Q}$
X	1	Q	$\overline{Q}$

(b)



(c)

Figure 6.23 Positive-edge-triggered T flip-flop. (*a*) Logic diagrams. (*b*) Function table where Q^+ denotes the output Q in response to the inputs. (*c*) Two logic symbols.

Characteristic Equations

- Next state table: Shows the value of the next state of the flip-flop for each combination of values to the present state of the flip-flops and their information lines.
- The algebraic description of the next-state table of a flip-flop is called the characteristic equation of the flip-flop.
- Obtained by constructing the K-map for Q^+ in terms of the present state and information input variables.

Next State Tables

Table 6.1 Simplified flip-flop function tables. Q denotes the current state and Q^+ denotes the resulting state as a consequence of the information inputs and the control signal. (*a*) *SR* flip-flop. (*b*) *D* flip-flop. (*c*) *JK* flip-flop. (*d*) *T* flip-flop.

S	R	Q^+
0	0	Q
0	1	0
1	0	1
1	1	–

(*a*)

D	Q^+
0	0
1	1

(*b*)

J	K	Q^+
0	0	Q
0	1	0
1	0	1
1	1	$\overline{Q}$

(*c*)

T	Q^+
0	Q
1	$\overline{Q}$

(*d*)

Table 6.2 Flip-flop next-state tables. Q denotes the current state and Q^+ denotes the resulting state as a consequence of the information inputs and the control signal. (*a*) *SR* flip-flop. (*b*) *D* flip-flop. (*c*) *JK* flip-flop. (*d*) *T* flip-flop.

S	R	Q	Q^+	
0	0	0	0	
0	0	1	1	
0	1	0	0	
0	1	1	0	
1	0	0	1	
1	0	1	1	
1	1	0	–	Inputs not allowed
1	1	1	–	

(*a*)

D	Q	Q^+
0	0	0
0	1	0
1	0	1
1	1	1

(*b*)

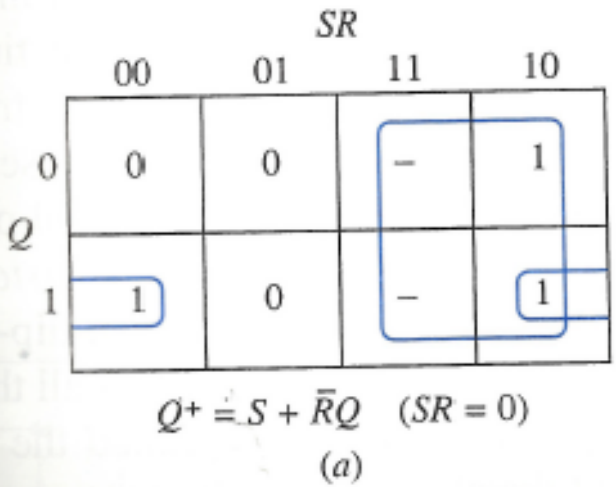
J	K	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(*c*)

T	Q	Q^+
0	0	0
0	1	1
1	0	1
1	1	0

(*d*)

Characteristic Equations



$Q^+ = S + \bar{R}Q \quad (SR = 0)$

(a)

Flip-flop type	Characteristic equation
SR	$Q^+ = S + \bar{R}Q \quad (SR = 0)$
JK	$Q^+ = J\bar{Q} + \bar{K}Q$
D	$Q^+ = D$
T	$Q^+ = T\bar{Q} + \bar{T}Q = T \oplus Q$

(b)

Figure 6.25 Characteristic equations. (*a*) Derivation of characteristic equation for an *SR* flip-flop. (*b*) Summary of characteristic equations.

End of Exam 2 Material

Clocked Synchronous Sequential Networks

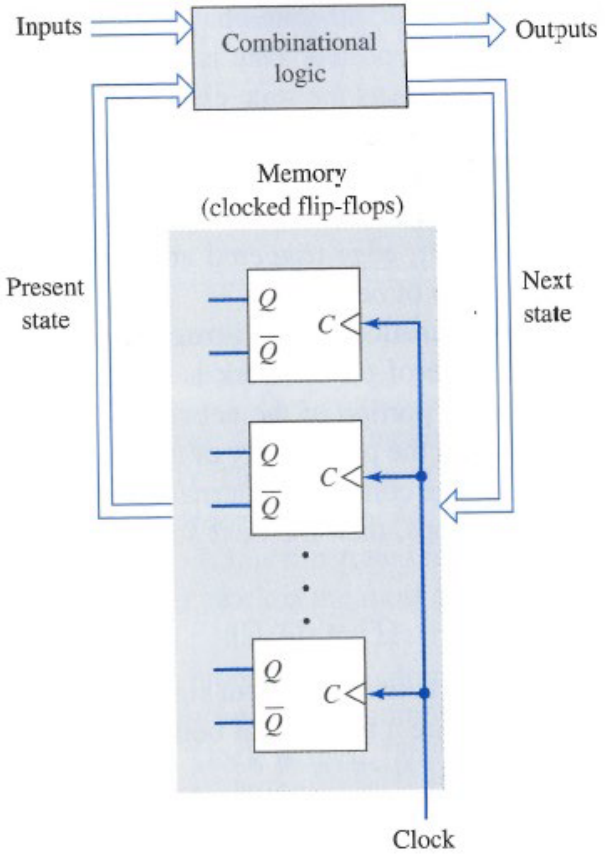


Figure 7.2 Structure of a clocked synchronous sequential network.

- Network behavior is defined at specific instants of time associated with a clock signal.
- Usually a master clock that appears at the control inputs of all the flip-flops.
- Combinational logic is used to generate the next-state and output signals.

Clocked Synchronous Sequential Networks

- Input and new present state signals are applied to the combinational logic.
- Effects of the signals must propagate through the network.
  - Final values at the flip-flop inputs occur at different times depending upon the number of gates involved in the signal paths.
- Only after final values are reached, active time of the clock signal is allowed to occur and cause any state changes.
- All state changes of the flip-flops occur at the same time.

Clocked Synchronous Sequential Networks

- Next state of the network: $Q^+ = f(X, Q)$
  - X denotes the collective external input signals
  - Q denotes the collective present states of the flip-flops.
- Z denotes the collective output signals of the network: $Z = g(X, Q)$.

Mealy model

- The general structure of a clocked synchronous sequential network.

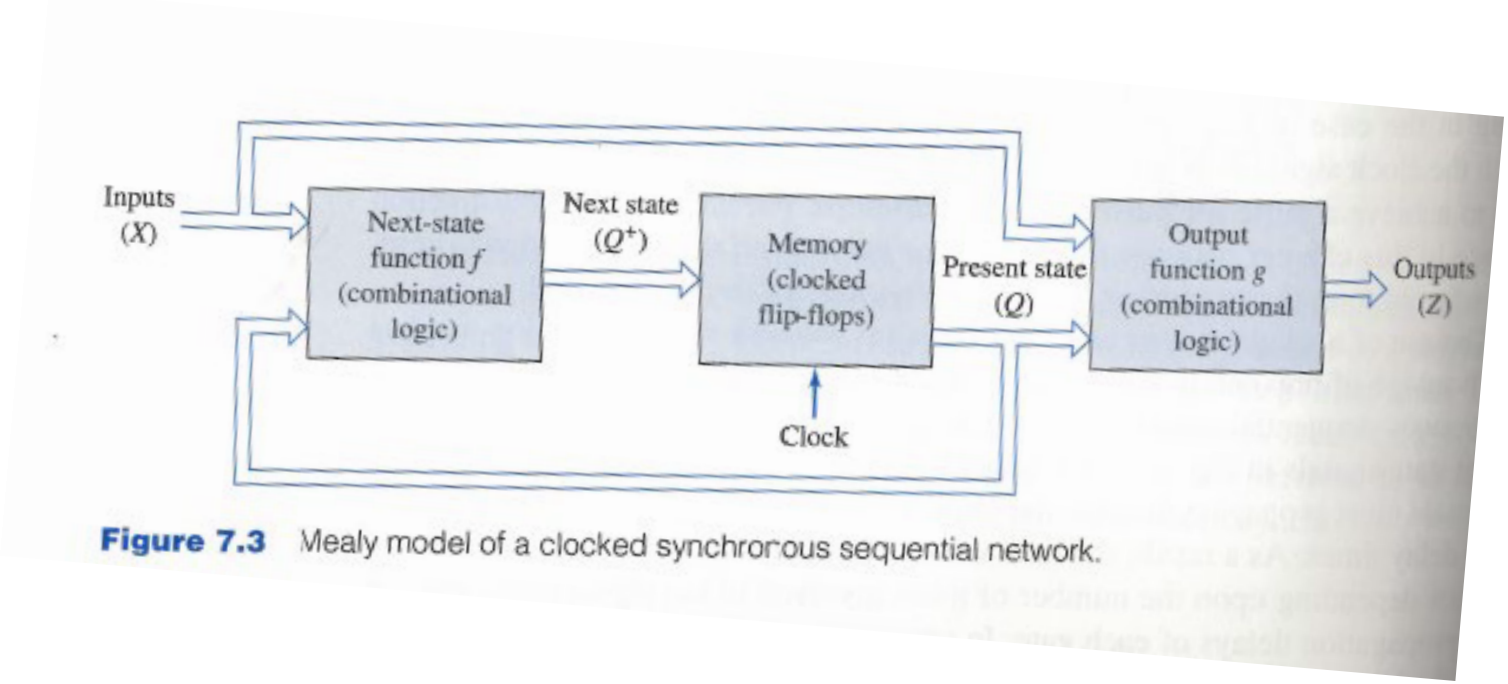
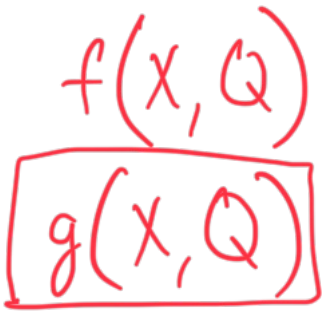


Figure 7.3 Mealy model of a clocked synchronous sequential network.

Moore Model



- Variation of Mealy model when the outputs are only a function of the present state and not of the external inputs: $Z = g(Q)$.

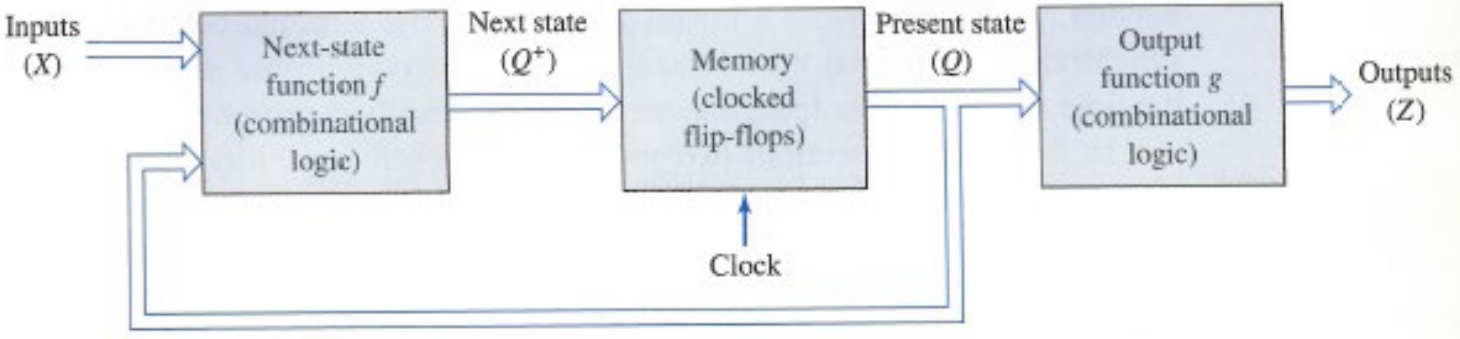
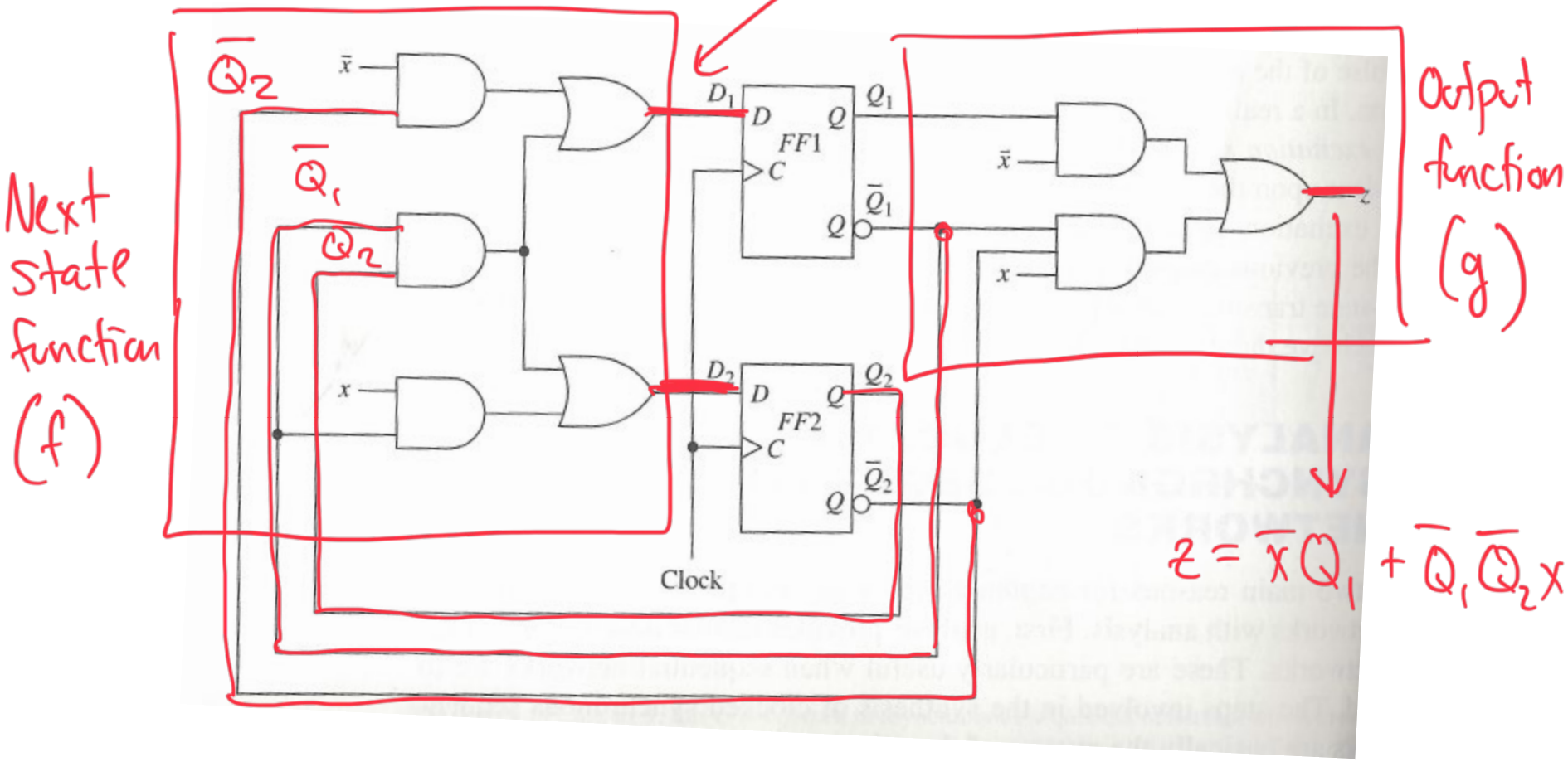


Figure 7.4 Moore model of a clocked synchronous sequential network.

Analysis of clocked Synchronous Sequential Network

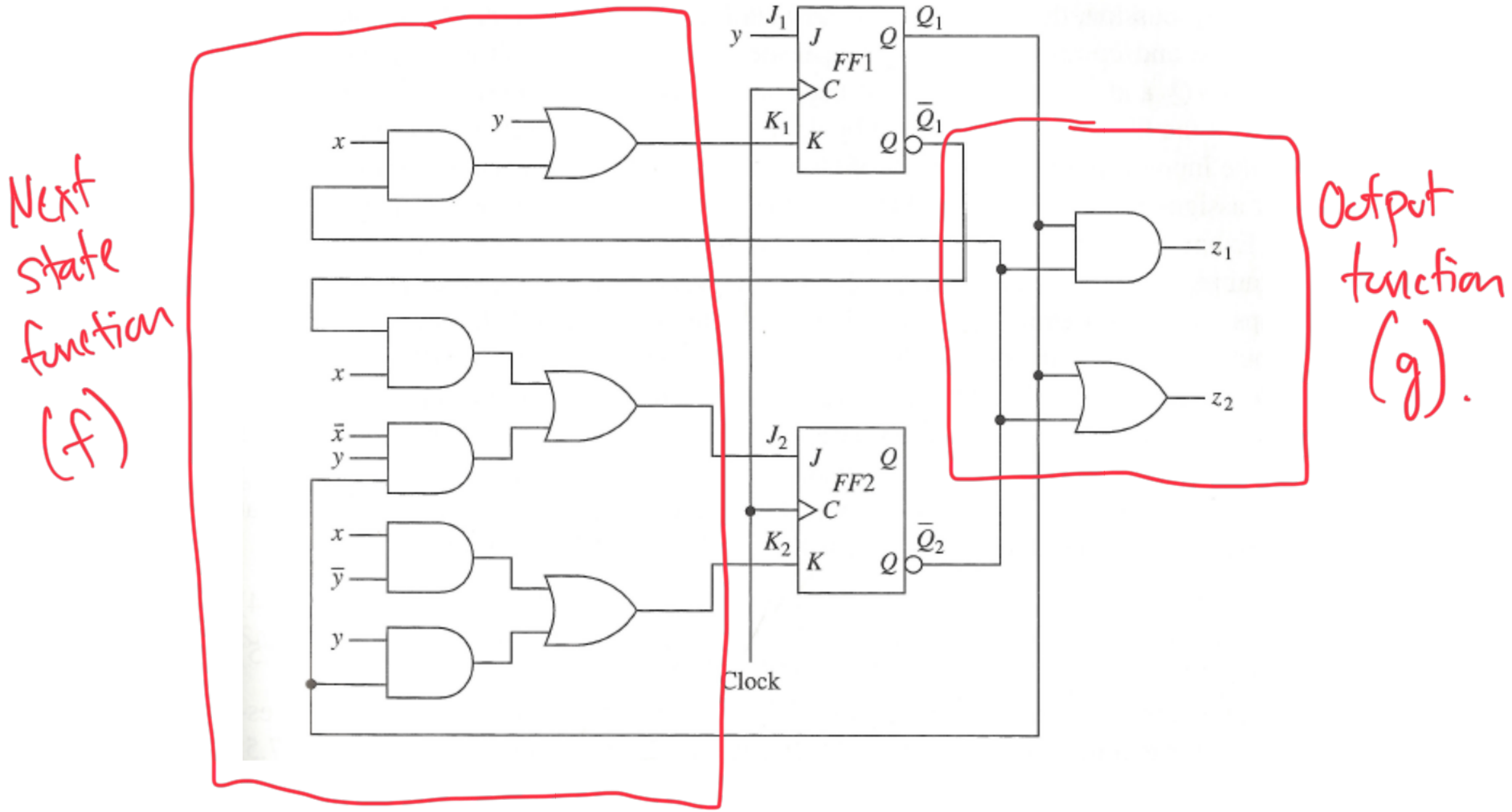
Two Examples

Figure 1: Mealy network



Two Examples

Figure 2: Moore network



Excitation and Output Expressions

- Assign variables to flip flop-states $Q_1, \overline{Q}_1, Q_2, \overline{Q}_2$
- Assign excitation variables to flip-flop inputs $D_1, D_2, J_1, K_1, J_2, K_2$

inputs to the flip flop

Excitation and output expressions for Fig. 1:

- $D_1 = \overline{x}\overline{Q}_2 + \overline{Q}_1 Q_2$
- $D_2 = x\overline{Q}_1 + \overline{Q}_1 Q_2$
- $z = \overline{x}Q_1 + x\overline{Q}_1\overline{Q}_2$

Excitation and output expressions for Fig 2:

- $J_1 = y$
- $K_1 = y + x\overline{Q}_2$
- $J_2 = x\overline{Q}_1 + \overline{x}yQ_1$
- $K_2 = x\overline{y} + yQ_1$
- $z_1 = Q_1\overline{Q}_2$
- $z_2 = Q_1 + \overline{Q}_2$

State

Transition Equations

Transition Equations for Figure 1:

- $Q^+_1 = D_1$
- $Q^+_2 = D_2$
- $Q^+_1 = \overline{x}\overline{Q}_2 + \overline{Q}_1 Q_2$
- $Q^+_2 = x\overline{Q}_1 + \overline{Q}_1 Q_2$

Transition Equations for Figure 2:

- $Q^+_1 = J_1\overline{Q}_1 + \overline{K}_1 Q_1$
- $Q^+_2 = \mathrm{J}_2\overline{Q}_2 + \overline{K}_2 Q_2$
- $Q^+_1 = \mathrm{y}\overline{Q}_1 + \overline{\left(y + x\overline{Q}_2\right)} Q_1 = \mathrm{y}\overline{Q}_1 + \overline{x}\,\overline{y} Q_1 + \overline{y} Q_1 Q_2$
- $Q^+_2 = \left(x\overline{Q}_1 + \overline{x} y Q_1\right)\overline{Q}_2 + \overline{(x\overline{y} + yQ_1)} Q_2 = \mathrm{x}\overline{Q}_1\overline{Q}_2 + \overline{x} y Q_1\overline{Q}_2 + \overline{x}\,\overline{y} Q_2 + \overline{x}\overline{Q}_1 Q_2 + y\overline{Q}_1 Q_2$

Excitation Table

- Excitation table consists of three parts:
  - Present-state section
  - Excitation section
  - Output section

Excitation Tables

Table 7.3 Excitation table for Example 7.1

Present state (Q_1Q_2)	Excitation (D_1D_2)		Output (z)	
	Input (x)		Input (x)	
	0	1	0	1
00	10	01	0	1
01	11	11	0	0
10	10	00	1	0
11	00	00	1	0

Table 7.4 Excitation table for Example 7.2

Present state (Q_1Q_2)	Excitation (J_1K_1,J_2K_2)				Output (z_1,z_2)
	Inputs (xy)				
	00	01	10	11	
00	00,00	11,00	01,11	11,10	01
01	00,00	11,00	00,11	11,10	00
10	00,00	11,11	01,01	11,01	11
11	00,00	11,11	00,01	11,01	01

Transition Tables

Rather than using algebraic descriptions can express the information in tabular form.

- Table consists of three sections
  - Present state variables
  - Next-state variables
  - Output variables
- Present state variables:
  - Lists all the possible combinations of values for the state variables.
  - If there are p state variables, then 2^p rows.
- Next-state section
  - One column for each combination of values of the external input variables.
  - If there are n external input variables, then 2^n columns.
  - Each entry is a p-tuple corresponding to the next state for each combination of present state and external input.
- Mealy network outputs:
  - One column for each combination of values of the external input variables.
  - Entries within the section indicate the outputs for each present-state/input combination.
- Moore network outputs:
  - Output section has only a single column.

State

Transition Tables

Table 7.3 Excitation table for Example 7.1

Present state (Q_1Q_2)	Excitation (D_1D_2)		Output (z)	
	Input (x)		Input (x)	
	0	1	0	1
00	10	01	0	1
01	11	11	0	0
10	10	00	1	0
11	00	00	1	0

Table 7.1 Transition table for Example 7.1

Present state (Q_1Q_2)	Next state $(Q_1^+Q_2^+)$		Output (z)	
	Input (x)		Input (x)	
	0	1	0	1
00	10	01	0	1
01	11	11	0	0
10	10	00	1	0
11	00	00	1	0

Transition Tables

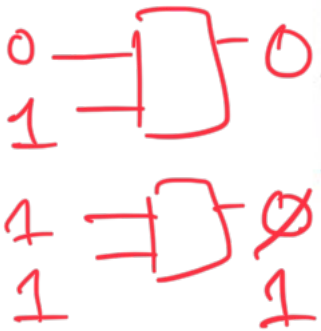


Table 7.4 Excitation table for Example 7.2

Present state (Q_1Q_2)	Excitation (J_1K_1,J_2K_2)				Output (z_1,z_2)
	Inputs (xy)				
	00	01	10	11	
00	00,00	11,00	01,11	11,10	01
01	00,00	11,00	00,11	11,10	00
10	00,00	11,11	01,01	11,01	11
11	00,00	11,11	00,01	11,01	01

Table 7.2 Transition table for Example 7.2

Present state (Q_1Q_2)	Next state $(Q_1^+Q_2^+)$				Output (z_1z_2)
	Inputs (xy)				
	00	01	10	11	
00	00	10	01	11	01
01	01	11	00	11	00
10	10	01	00	00	11
11	11	00	10	00	01

Constructing Transition Tables from Excitation Tables

- The transition table is constructed as the result of substituting excitation expressions into the flip-flop characteristic equations.
- An alternative approach:
  - First construct the excitation table directly from the excitation and output expressions.

Constructing Transition Tables from Excitation Tables

- Consider entry in fourth column, first row of 7.2 excitation table:
  - $J_1K_1, J_2K_2 = 11,10$
  - Present state: $Q_1Q_2 = 00$
  - So due to behavior of JK-flip-flop next state is: $Q^+{}_1 = 1, Q^+{}_2 = 1.$

State Tables

- State table consists of three sections:
  - Present state
  - Next state
  - Output
- Actual binary codes used to represent the states are not important.
- Alphanumeric symbols can be assigned to represent these states.
- State table is essentially a relabeling of the transition table.

State Tables

Table 7.1 Transition table for Example 7.1

Present state (Q_1Q_2)	Next state $(Q_1^+Q_2^+)$		Output (z)	
	Input (x)		Input (x)	
	0	1	0	1
00	10	01	0	1
01	11	11	0	0
10	10	00	1	0
11	00	00	1	0

Table 7.5 State table for Example 7.1

Present state	Next state		Output (z)	
	Input (x)		Input (x)	
	0	1	0	1
$00 \rightarrow A$	C	B	0	1
$01 \rightarrow B$	D	D	0	0
$10 \rightarrow C$	C	A	1	0
$11 \rightarrow D$	A	A	1	0

State Tables

Table 7.2 Transition table for Example 7.2

Present state (Q_1Q_2)	Next state $(Q_1^+Q_2^+)$				Output (z_1z_2)
	Inputs (xy)				
	00	01	10	11	
00	00	10	01	11	01
01	01	11	00	11	00
10	10	01	00	00	11
11	11	00	10	00	01

Table 7.6 State table for Example 7.2

Present state	Next state				Output (z_1z_2)
	Inputs (xy)				
	00	01	10	11	
$00 \rightarrow A$	A	C	B	D	01
$01 \rightarrow B$	B	D	A	D	00
$10 \rightarrow C$	C	B	A	A	11
$11 \rightarrow D$	D	A	C	A	01

State Diagrams

- Graphical representation of the state table.
  - Each state is represented by a labeled node.
  - Directed branches connect the nodes to indicate transitions between states.
  - Directed branches are labeled according to the values of the external input variables.
  - Outputs of the sequential network are also entered on a state diagram.
- Mealy network:
  - Outputs appear on the directed branches along with the external inputs.
- Moore network:
  - Outputs are included within the nodes along with their associated states.

State Diagrams

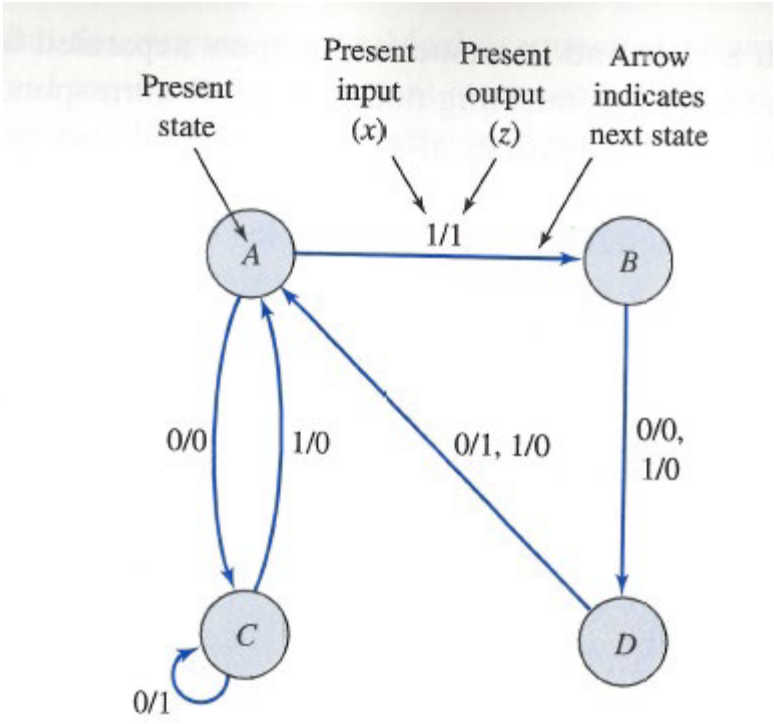


Figure 7.7 State diagram for Example 7.1.

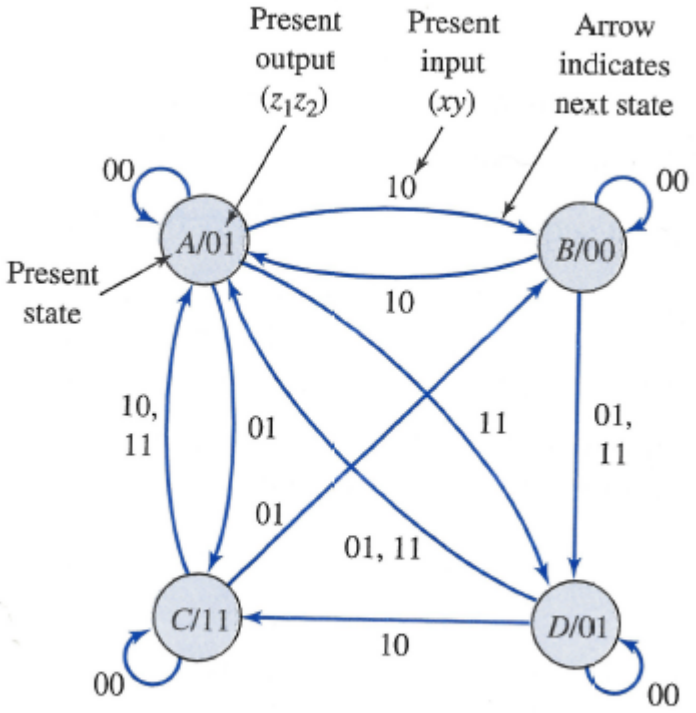


Figure 7.8 State diagram for Example 7.2.

Network Terminal Behavior

- Consider example from Figure 1:
  - Assume flip-flops are both in 0-states (state A)
  - Input sequence $x = 0011011101$ is applied

Input sequence x	=	0	0	1	1	0	1	1	1	0	1
State sequence	=	A	C	C	A	B	D	A	B	D	A	B
Output sequence z	=	0	1	0	1	0	0	1	0	1	1

- Note: For mealy sequential network, although outputs are shown on directed branches, this does not mean that the outputs are produced during the transition.
  - Outputs appearing on the branches are continuously available while in a present state and the indicated inputs are applied.

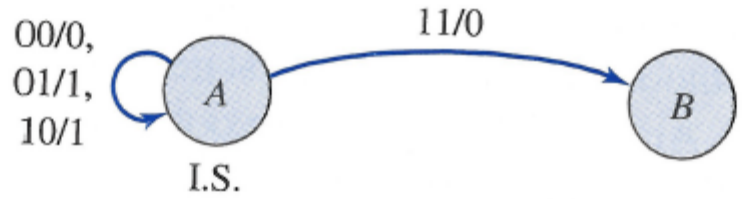
Modeling clocked synchronous sequential network behavior

- Approach for the synthesis of clocked synchronous sequential networks:
  - State table/state diagram is constructed from word specifications.
  - State reduction technique to obtain a state table with minimum number of states.
  - Transition table is formed by coding the states of the state table.
  - Excitation table is constructed based on the flip-flop types to be used.
  - From the excitation table, the excitation and output expressions for the network are determined.
  - Finally, the logic diagram is drawn.

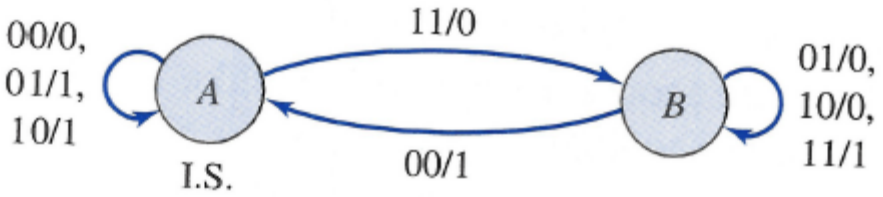
Examples of Modeling Step

Examples of Modeling Step

State Diagram for Mealy serial binary adder



(*a*)



(*b*)

Figure 7.12 Obtaining the state diagram for a Mealy serial binary adder. (*a*) Partial state diagram. (*b*) Completed state diagram.

State Diagram for Moore serial binary adder

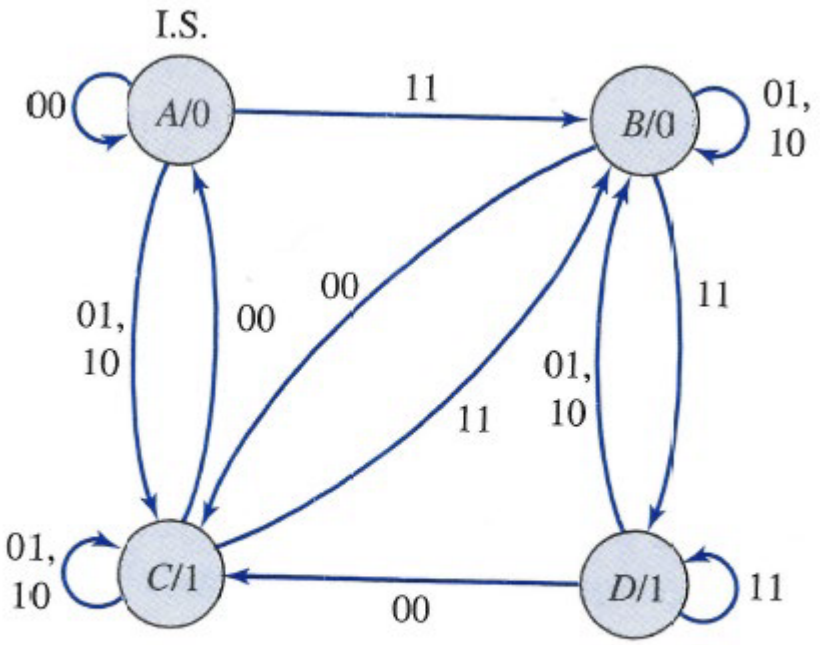


Figure 7.13 State diagram for a Moore serial binary adder.

False Outputs in a Mealy network

- The values of the external input variables may change at any time during the clock period.
- Although these input changes can continuously affect the network outpus, the consequences of these input changes do not appear in the listing of the output sequence.

Timing Diagrams to Illustrate False Outputs

