Digital Logic Design
ENEE 244-020x

Lecture 15

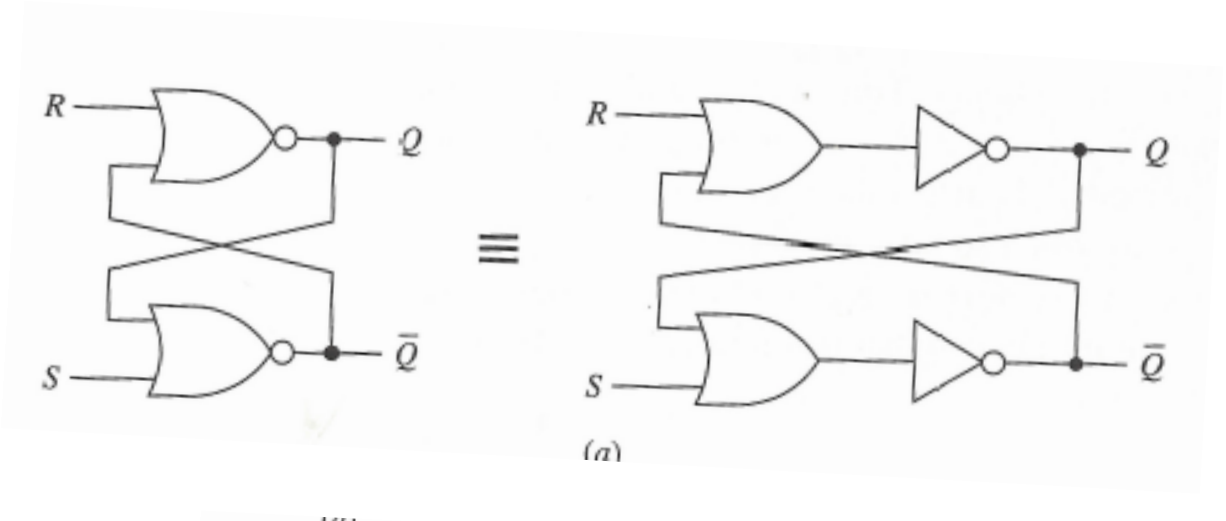
Announcements

- Homework 5 due Sunday 11/8 @11:59pm
- Exam 2 postponed to Thursday, 11/12

Agenda

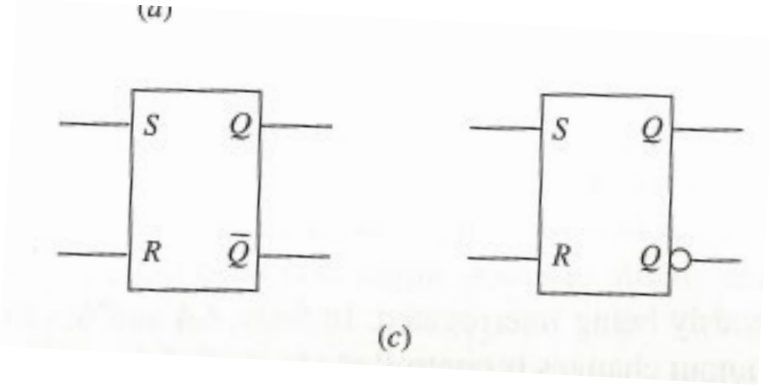
- Last time:
  - The Basic Bistable Element (5/3)
  - Latches (5.3)
  - Timing Considerations (5.3)
- This time:
  - Leader-Follower Flip-Flops (5.4)
  - Edge-Triggered Flip-Flops (5.4)
  - Characteristic Equations (5.4)

Review--The SR Latch



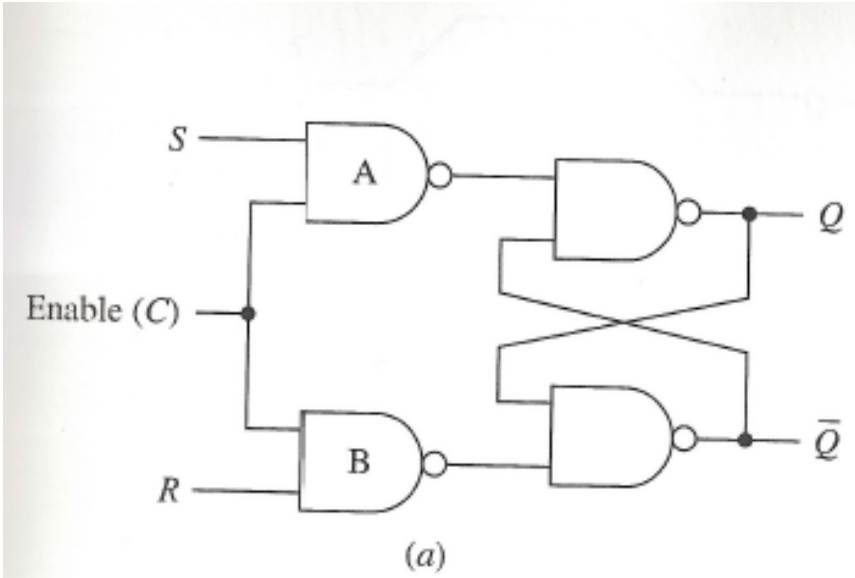
Inputs		Outputs	
S	R	Q^+	$\bar{Q}^+$
0	0	Q	$\bar{Q}$
0	1	0	1
1	0	1	0
1	1	0*	0*

*Unpredictable behavior will result if inputs return to 0 simultaneously



$Q^+, \overline{Q}^+$ indicates the response of the latch at the $Q, \overline{Q}$ output terminals as a consequence of applying the various inputs.
Q^+ is called the next state of the latch.

Review--The Gated SR Latch

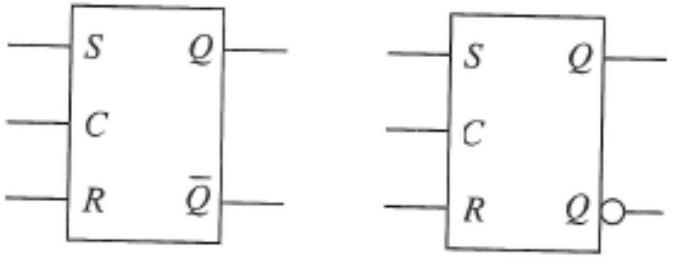


(a)

Inputs			Outputs	
S	R	C	Q^+	$\overline{Q}^+$
0	0	1	Q	$\overline{Q}$
0	1	1	0	1
1	0	1	1	0
1	1	1	1*	1*
X	X	0	Q	$\overline{Q}$

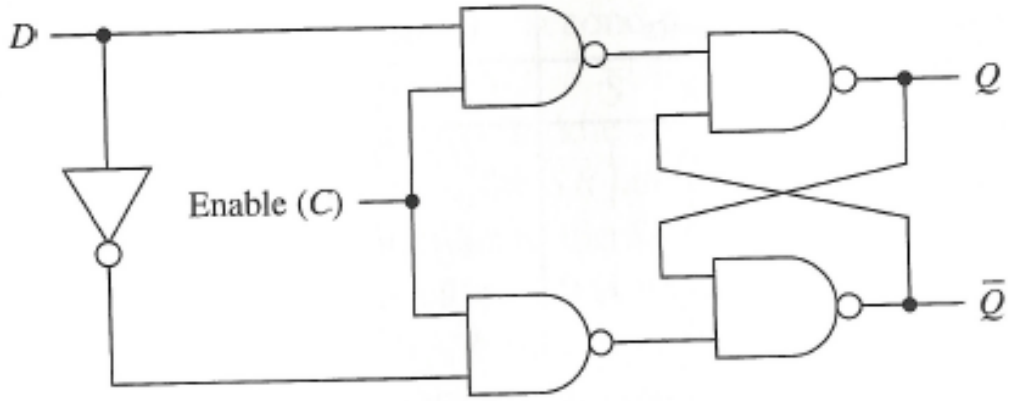
*Unpredictable behavior will result if S and R return to 0 simultaneously or C returns to 0 while S and R are 1

(b)



(c)

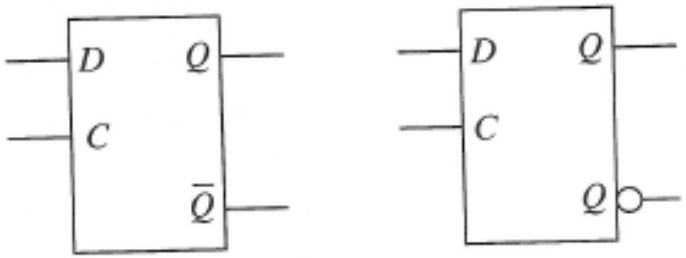
Review--The Gated D Latch



(a)

Inputs		Outputs	
D	C	Q^+	$\overline{Q}^+$
0	1	0	1
1	1	1	0
X	0	Q	$\overline{Q}$

(b)



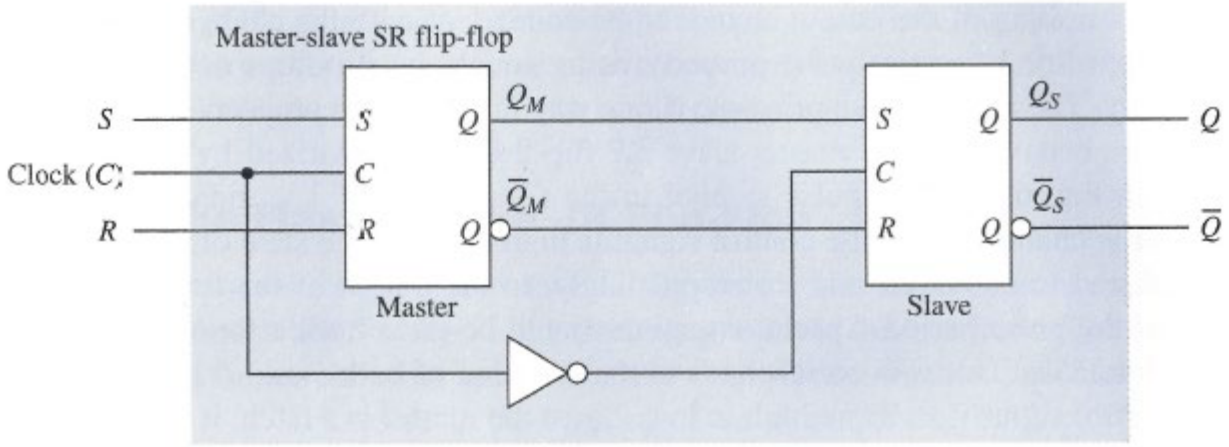
(c)

Leader-Follower Flip-Flops (Pulse Triggered Flip-Flops)

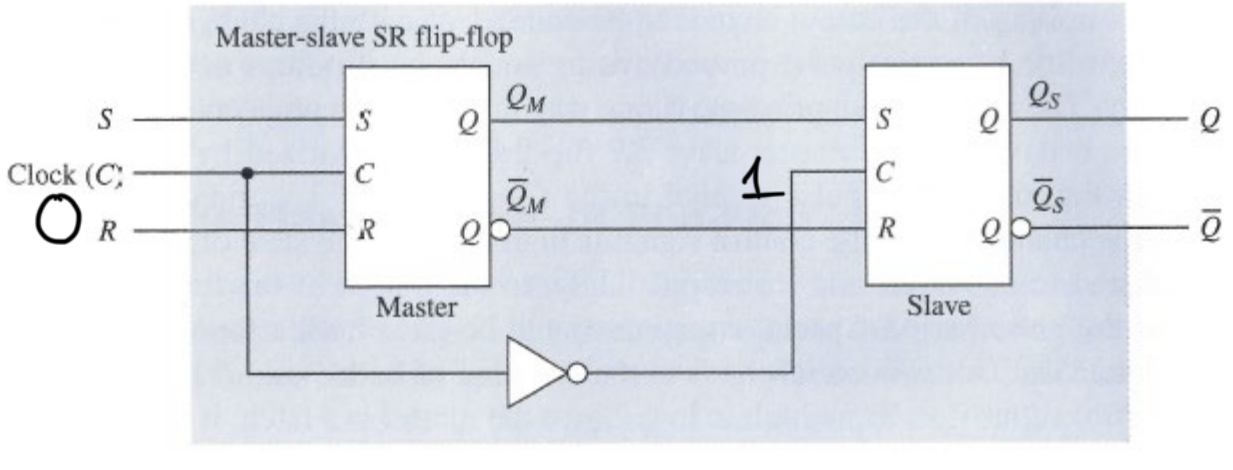
- Aside from latches, two categories of flip-flops.
  - Leader-follower flip-flops (pulse-triggered flip-flops, master-slave flip-flops)
  - Edge-triggered flip-flops
- Latches have immediate output response (known as transparency)
- May be undesirable:
  - May be necessary to sense the current state of a flip-flop while allowing new state information to be entered.

Leader-Follower SR Flip-Flop

- Two sections, each capable of storing a binary symbol.
- First section is referred to as the leader and the second section as the follower.
- Information is entered into the leader on one edge or level of a control signal and is transferred to the follower on the next edge or level of the control signal.
- Each section is a latch.

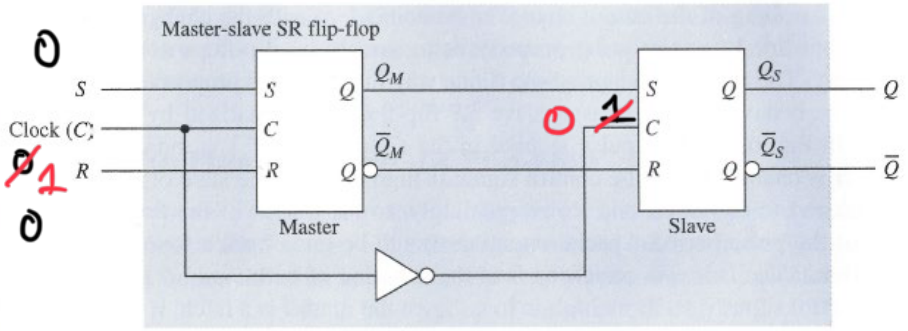


Leader-Follower SR Flip-Flop

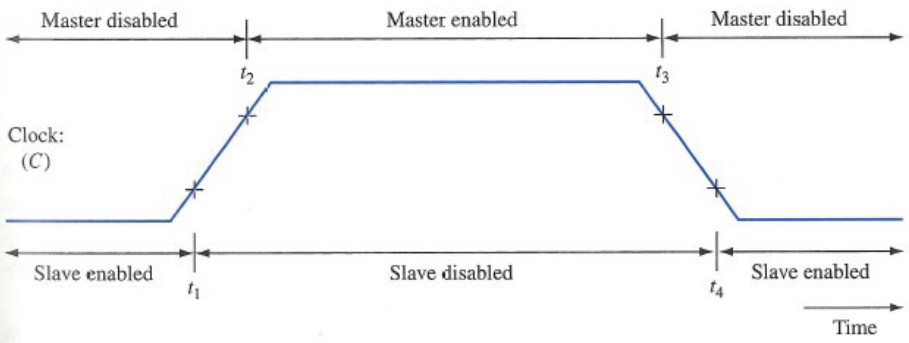


- C = 0:
  - Leader is disabled. Any changes to S,R ignored.
  - Follower is enabled. Is in the same state as the leader.
- C = 1:
  - Follower is disabled (retains state of master)
  - Leader is enabled, responds to inputs. Changes in state of leader are not reflected in disabled follower.
- C = 0:
  - Leader is disabled.
  - Follower is enabled and takes on new state of the leader.
- Important: For short periods during rising and falling edges, both leader and follower are disabled.

Leader-Follower SR Flip-Flop



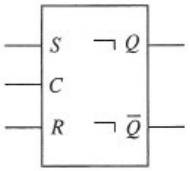
(a)

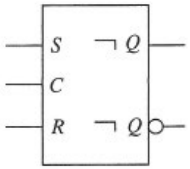


(b)

Inputs			Outputs	
S	R	C	Q^+	$\overline{Q}^+$
0	0	⊓	Q	$\overline{Q}$
0	1	⊓	0	1
1	0	⊓	1	0
1	1	⊓	Undefined	Undefined
X	X	0	Q	$\overline{Q}$

(c)





(d)

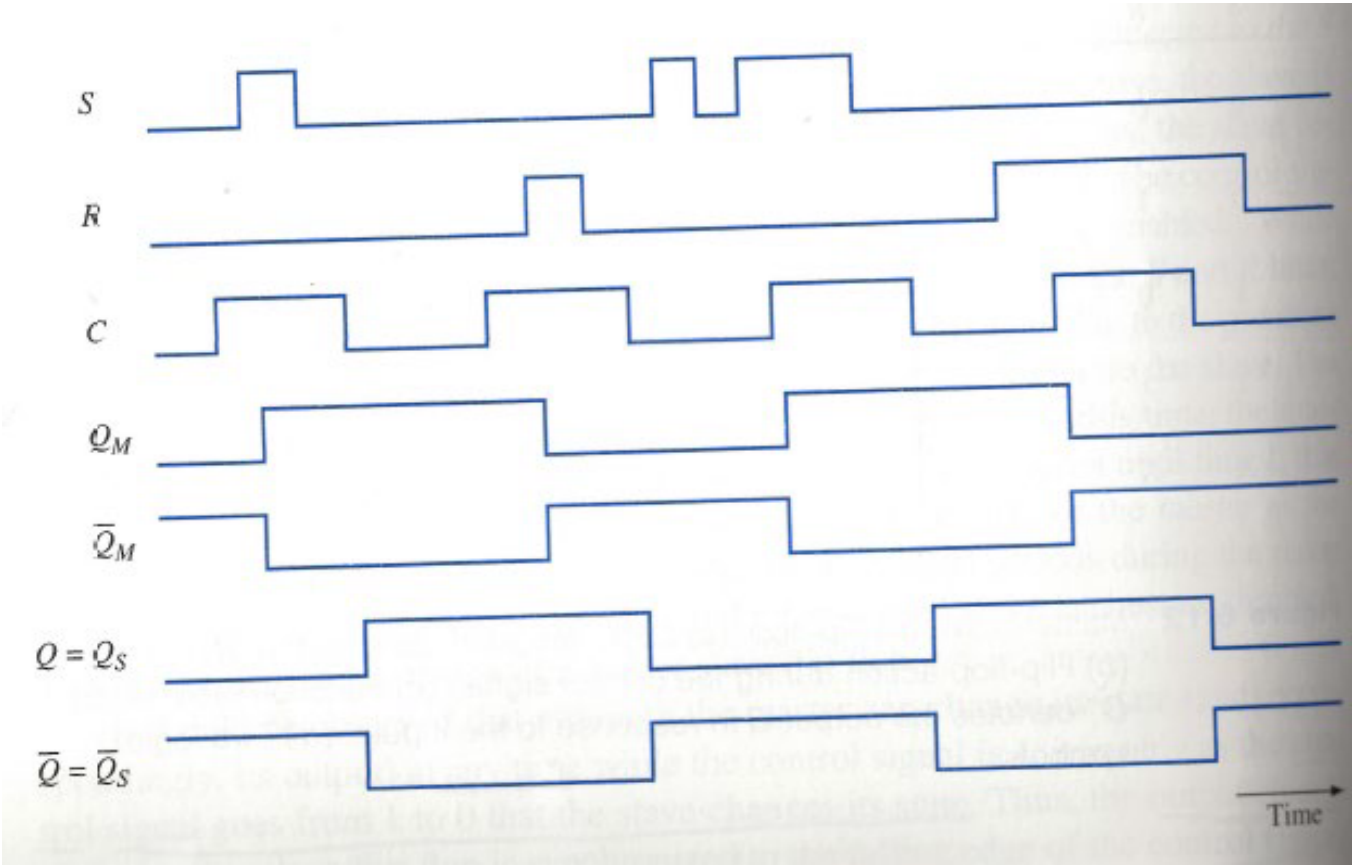
Pulse symbol indicates leader enabled when C = 1 and state of leader transferred to follower at the end of the pulse period.

Follower only takes on state of the leader at t_4.

Postponed output indicator: output change postponed until end of pulse

If S, R = 1 when control signal goes from high to low we are in an unpredicable state. Can cause metastable state.

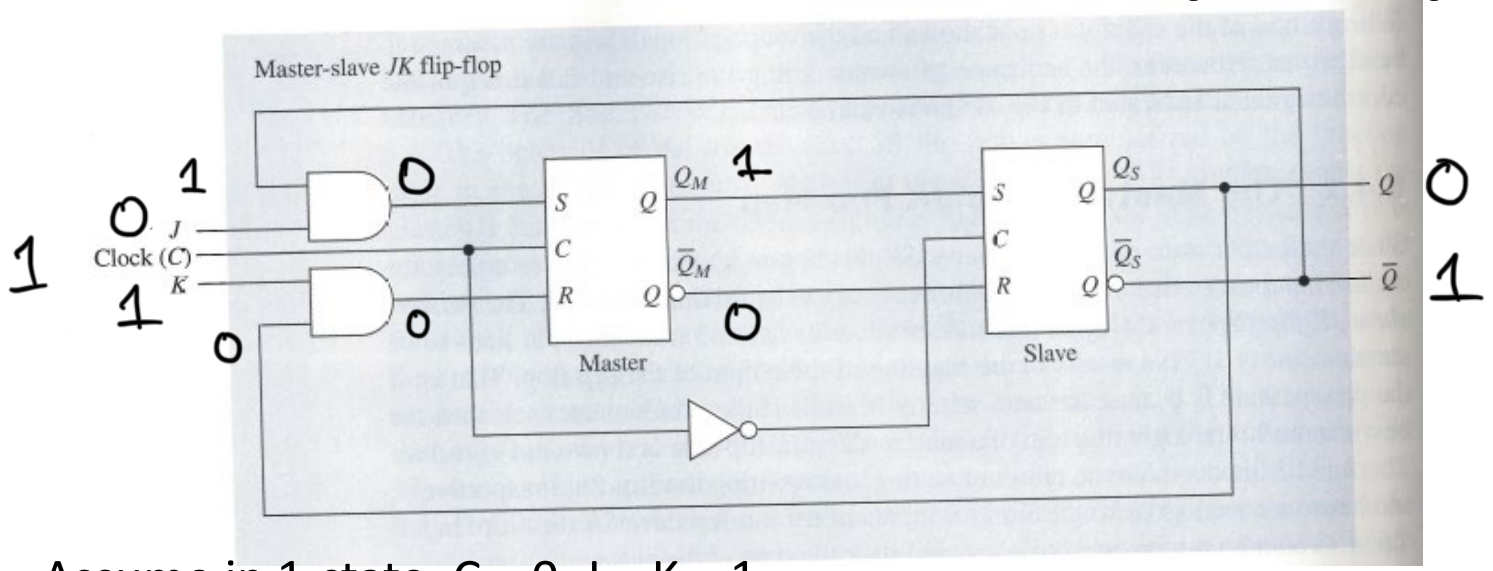
Timing Diagram for Leader-Follower SR flip-flop



Leader-Follower JK Flip-Flop

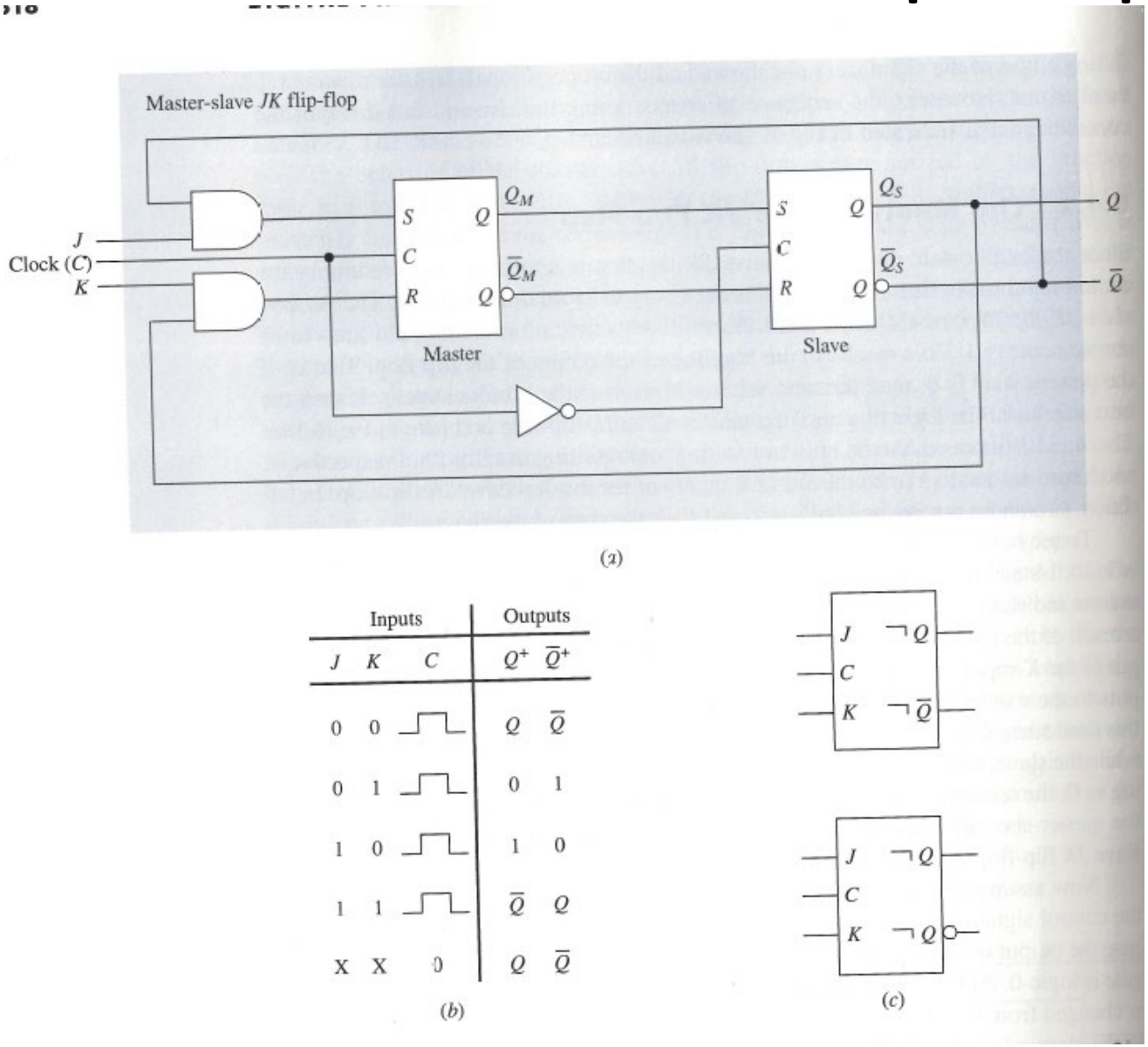
- The output state of a leader-follower SR flip-flop is undefined upon returning the control input to 0 when S = R = 1.
  - Necessary to avoid this condition.
- Leader-follower JK flip-flop allows its two information input lines to be simultaneously 1.
  - Results in toggling the output of the flip flop.

Leader-Follower JK Flip-Flop

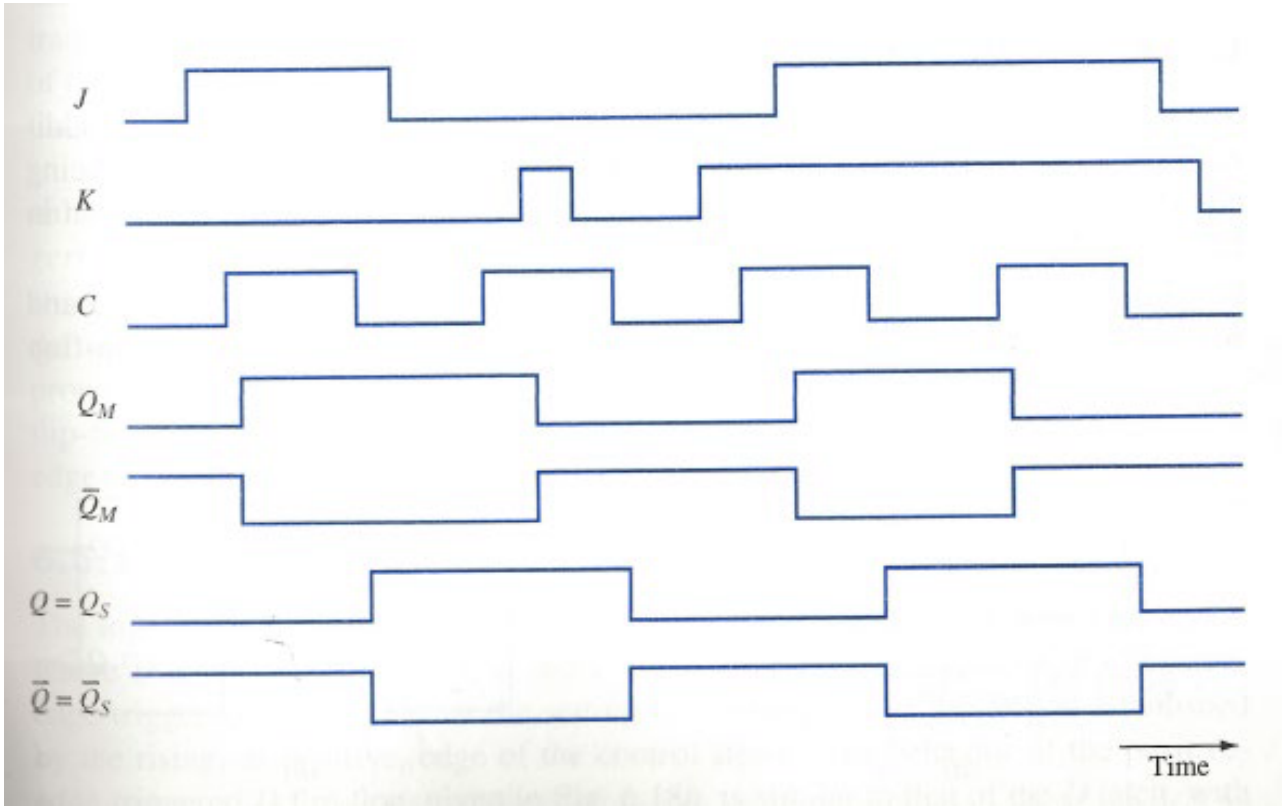


- Assume in 1-state, C = 0, J = K = 1.
  - Due to feedback, the output of the J-gate is 0, output of K-gate is 1.
  - If clock is changed to C = 1 then leader is reset.
- Assume in 0-state, C = 0, J = K = 1.
  - Due to feedback, the output of the J-gate is 1, output of K-gate is 0.
  - If clock is changed to C = 1 then leader is set.
- 1 on J input line, 0 on K input line sets the flip-flop.
  - If in 1-state, unchanged b/c S,R set to 0.
  - If in 0-state, S set to 1, R set to 0.
- 0 on J input, 1 on K input line resets the flip-flop. Why?

Leader-Follower JK Flip-Flop



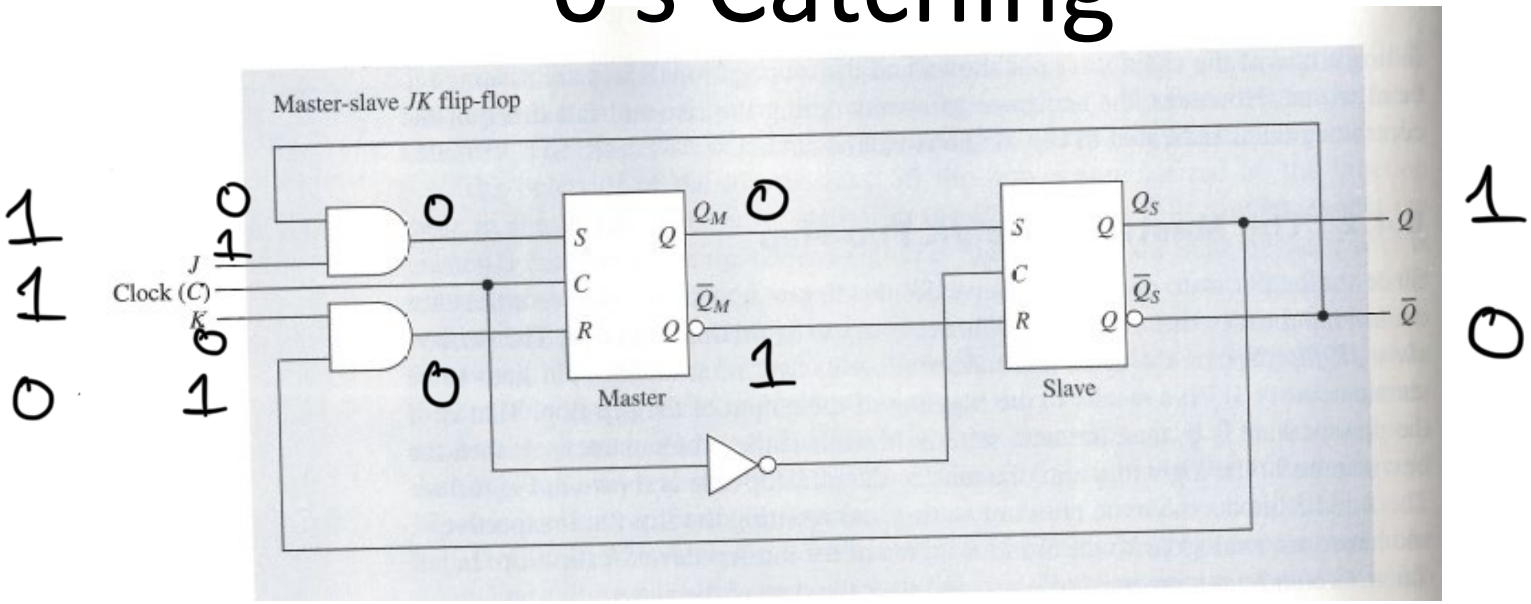
Timing Diagram for Leader-Follower JK Flip-Flop



0's and 1's Catching

- The leader is enabled during the entire period the control-signal is 1.
- If the follower latch is in its 1-state, then a logic-1 on K-input line causes the leader-latch to reset. Follower becomes reset when control signal returns to 0.
- This is known as 0's catching (2^{nd} pulse).
  - Note: if a subsequent 1-signal on J input line and C is still 1, leader does not become set again (due to feedback not changing).
- If follower latch is in 0-state, logic-1 on J input line while control signal is 1 causes the leader latch to be set and follower will be set upon occurrence of the falling edge.
- This is known as 1's catching (3^{rd} pulse).
- In many applications, 0's and 1's catching behavior is undesirable. Normally recommended that the J and K input values should be held fixed during the entire interval the leader is enabled.
- Any changes in J, K must occur while the control signal is 0.

0's Catching

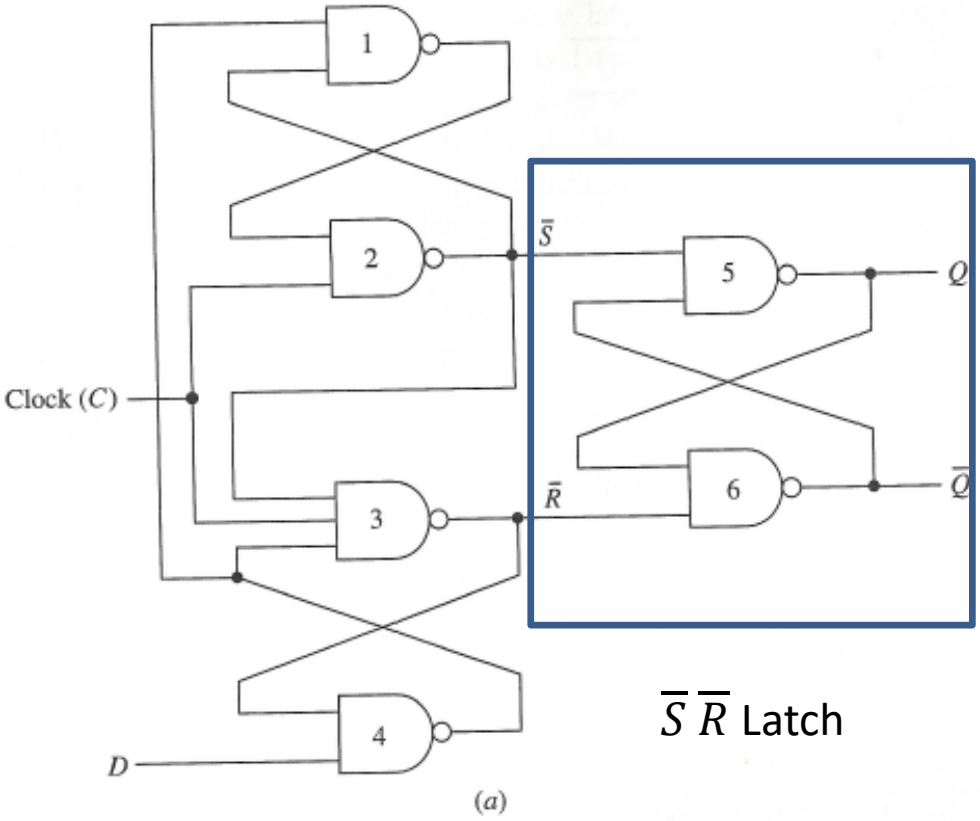


- Assume in 1-state $\left(Q = 1, \overline{Q} = 0\right), \mathrm{C} = 1, \mathrm{J} = 0, \mathrm{K} = 0$
- K gets set to 1 briefly.
  - Leader gets reset, Follower will become reset when Clock goes to 0.
- K goes to 0.
- J goes to 1. What happens? Nothing: Leader stays in same state
- Nothing! Follower will still become reset when Clock goes to 0.
- Why?

Edge-Triggered Flip-Flops

- In basic leader-follower flip-flops, leader is enabled during the entire period the control input is 1.
  - This can result in 0's and 1's catching.
  - To avoid this, signals on information lines are restricted from changing during the time the leader is enabled.
  - Also a delay in the output since leader's state is established during the positive edge and transferred to the follower on the negative edge of clock.
- Edge-triggered flip-flops use just one of the edges of the clock signal.
  - This is referred to as the triggering edge.
- Response to triggering edge at the output of the flip-flop is almost immediate (depends only on propagation delay times).
- Once triggering occurs, flip-flop is unresponsive to information input changes until the next triggering edge.

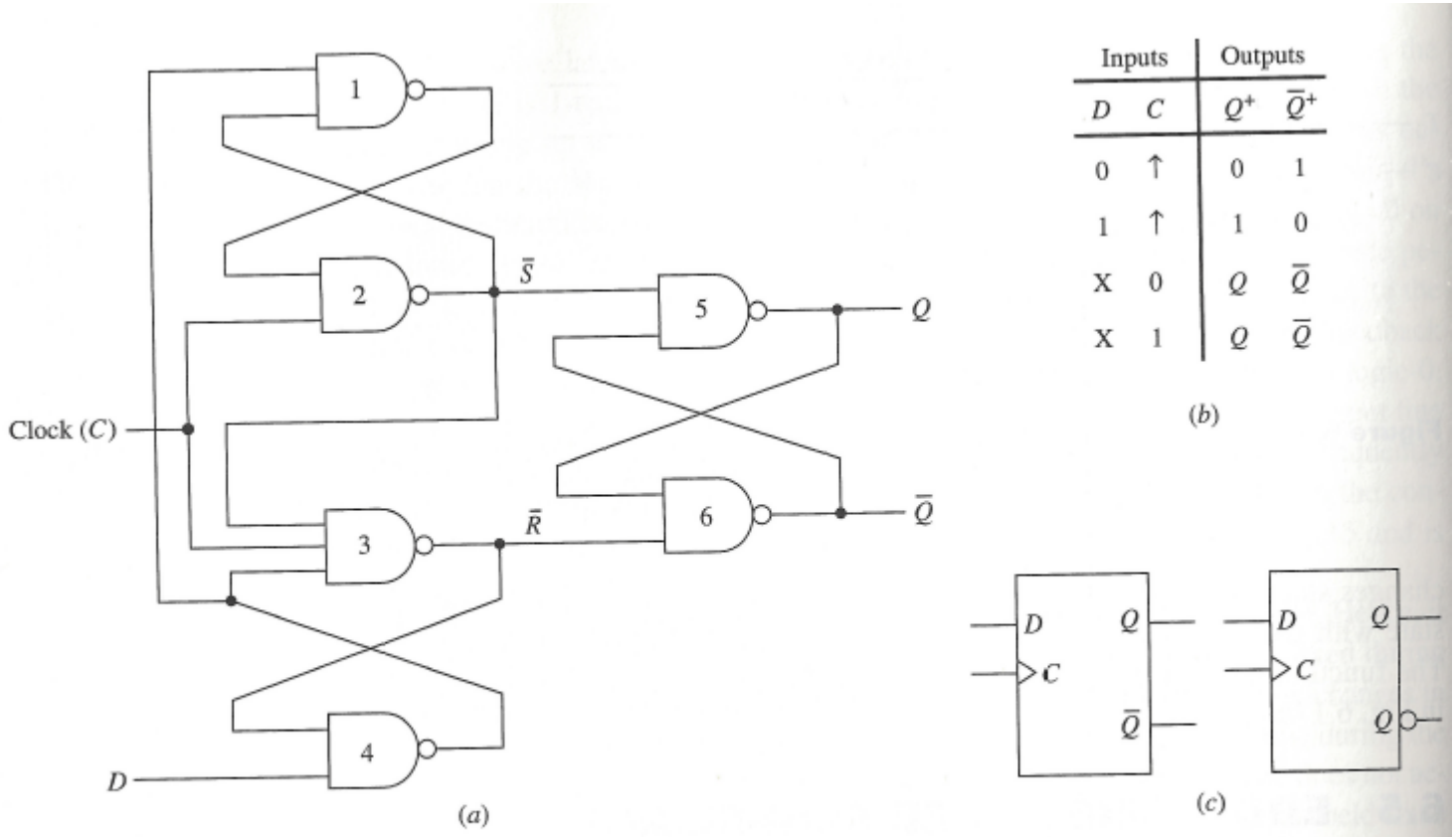
Edge-Triggered Flip-Flops



$\overline{S}\,\overline{R}$ Latch

1. C = 0. Regardless of input at D, outputs of gates 2,3 are 1. So $\overline{S} = \overline{R} = 1$. State of latch is held.
2. Assume D = 0: Output of gate 4 is 1, output of gate 1 is 0. When C goes to 1: all inputs to gate 3 are 1, output changes to 0. Output of gate 2 remains at 1 since output of gate 1 is 0. So $\overline{S} = 1, \overline{R} = 0$. Output of gate 3 (0) is fed to input of gate 4. Output of gate 4, gate 1 not affected by changes to D.
3. Assume C = 0, D = 1. Outputs of gates 2,3, are 1. Output of gate 4 is 0, output of gate 1 is 1. When C goes to 1: output of gate 2 is 0, output of gate 3 remains at 1. So $\overline{S} = 0, \overline{R} = 1$. Output from gate 2 is input to gates 1, 3 so their outputs remain at 1. Changes in D have no affect on state of flip-flop while C = 1.

Edge-Triggered Flip-Flops



Inputs		Outputs	
D	C	Q^+	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	Q	$\bar{Q}$
X	1	Q	$\bar{Q}$

Figure 6.18 Positive-edge-triggered D flip-flop. (*a*) Logic diagram.(*b*) Function table where Q^+ denotes the output Q in response to the inputs. (*c*) Two logic symbols.

Timing Diagram

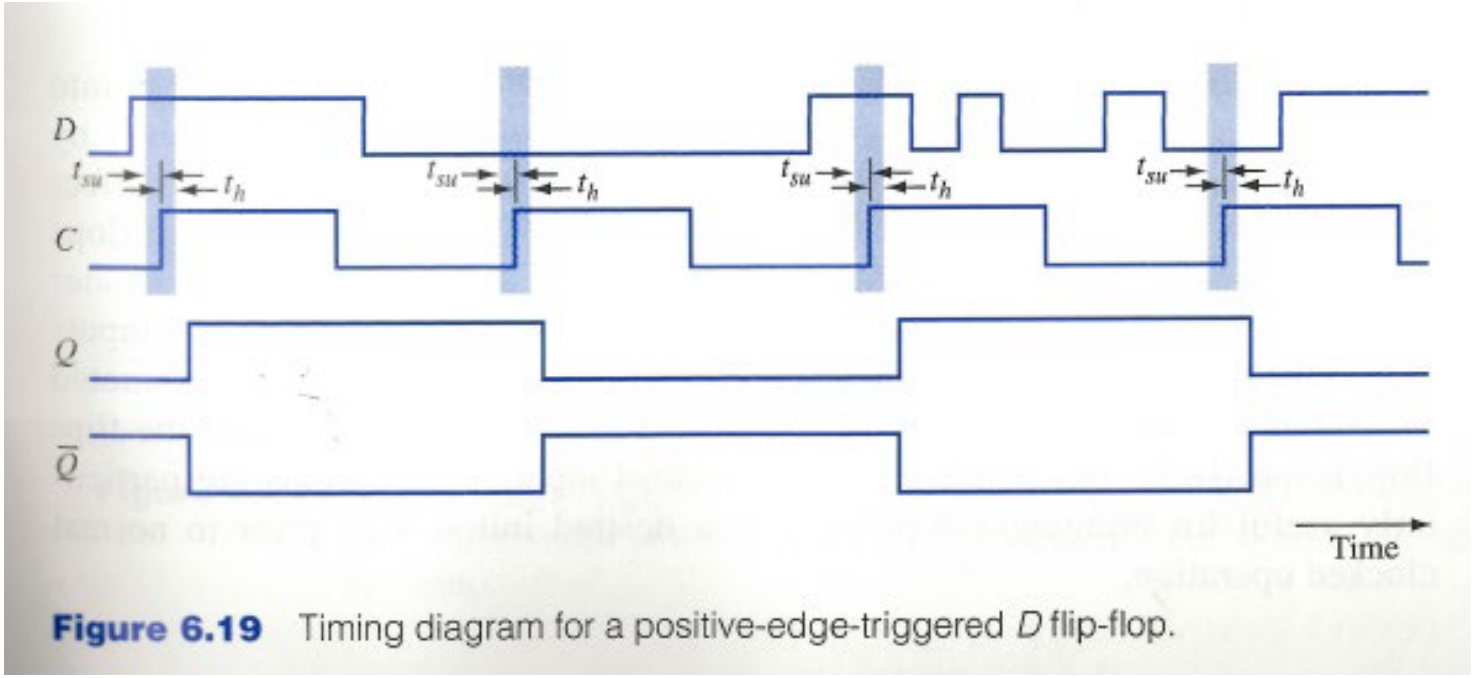
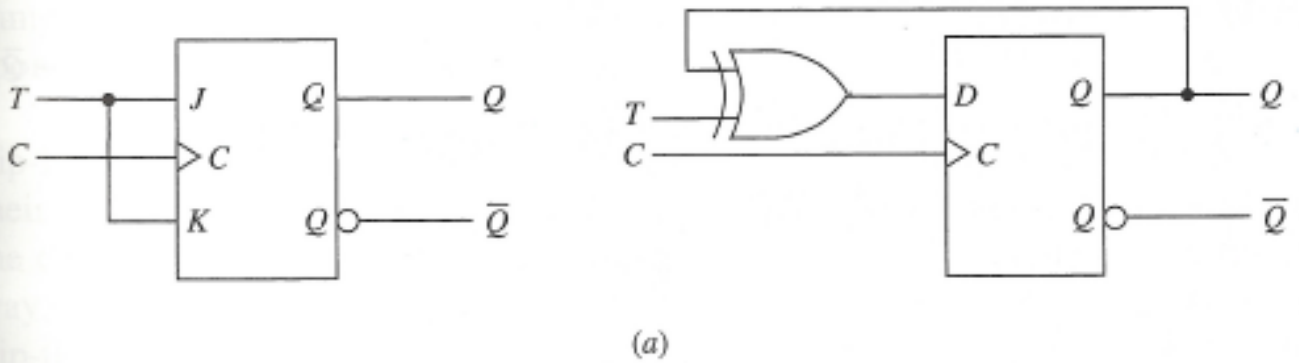


Figure 6.19 Timing diagram for a positive-edge-triggered *D* flip-flop.

During setup and hold times t_{su}, t_h with respect to the triggering edge of the clock, D input must not change.

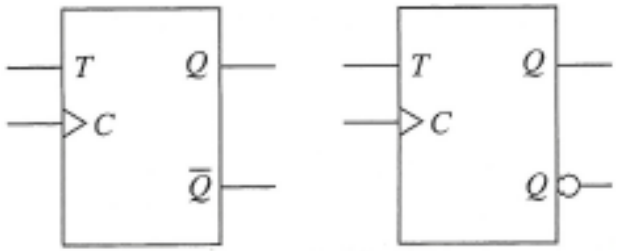
Positive-Edge Triggered T-Flip-Flop



(a)

Inputs		Outputs	
T	C	Q^+	$\overline{Q}^+$
0	↑	Q	$\overline{Q}$
1	↑	$\overline{Q}$	Q
X	0	Q	$\overline{Q}$
X	1	Q	$\overline{Q}$

(b)



(c)

Figure 6.23 Positive-edge-triggered T flip-flop. (*a*) Logic diagrams. (*b*) Function table where Q^+ denotes the output Q in response to the inputs. (*c*) Two logic symbols.

Characteristic Equations

- Next state table: Shows the value of the next state of the flip-flop for each combination of values to the present state of the flip-flops and their information lines.
- The algebraic description of the next-state table of a flip-flop is called the characteristic equation of the flip-flop.
- Obtained by constructing the K-map for Q^+ in terms of the present state and information input variables.

Next State Tables

Table 6.1 Simplified flip-flop function tables. Q denotes the current state and Q^+ denotes the resulting state as a consequence of the information inputs and the control signal. (*a*) *SR* flip-flop. (*b*) *D* flip-flop. (*c*) *JK* flip-flop. (*d*) *T* flip-flop.

S	R	Q^+
0	0	Q
0	1	0
1	0	1
1	1	–

(*a*)

D	Q^+
0	0
1	1

(*b*)

J	K	Q^+
0	0	Q
0	1	0
1	0	1
1	1	$\overline{Q}$

(*c*)

T	Q^+
0	Q
1	$\overline{Q}$

(*d*)

Table 6.2 Flip-flop next-state tables. Q denotes the current state and Q^+ denotes the resulting state as a consequence of the information inputs and the control signal. (*a*) *SR* flip-flop. (*b*) *D* flip-flop. (*c*) *JK* flip-flop. (*d*) *T* flip-flop.

S	R	Q	Q^+	
0	0	0	0	
0	0	1	1	
0	1	0	0	
0	1	1	0	
1	0	0	1	
1	0	1	1	
1	1	0	–	Inputs not allowed
1	1	1	–	

(*a*)

D	Q	Q^+
0	0	0
0	1	0
1	0	1
1	1	1

(*b*)

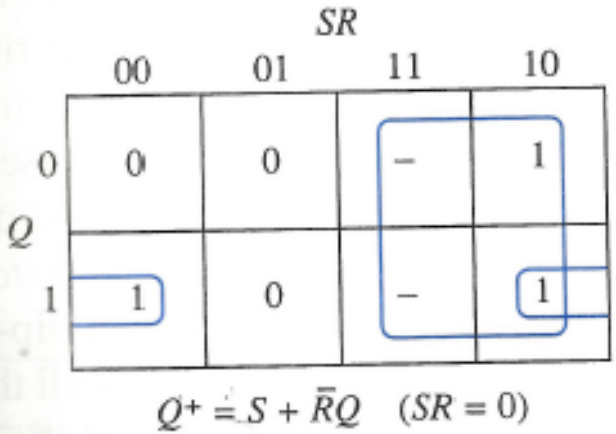
J	K	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(*c*)

T	Q	Q^+
0	0	0
0	1	1
1	0	1
1	1	0

(*d*)

Characteristic Equations



$Q^+ = S + \bar{R}Q \quad (SR = 0)$

(*a*)

Flip-flop type	Characteristic equation
SR	$Q^+ = S + \bar{R}Q \quad (SR = 0)$
JK	$Q^+ = J\bar{Q} + \bar{K}Q$
D	$Q^+ = D$
T	$Q^+ = T\bar{Q} + \bar{T}Q = T \oplus Q$

(*b*)

Figure 6.25 Characteristic equations. (*a*) Derivation of characteristic equation for an *SR* flip-flop. (*b*) Summary of characteristic equations.