Digital Logic Design
ENEE 244-020x

Lecture 14

Announcements

- Homework 4 due Sunday 11/1 @11:59pm

Agenda

- Last time:
  - Logic Design with Decoders and Multiplexers (4.9, 4.11)
- This time:
  - New topic: Flip-flops
    - The Basic Bistable Element (5/3)
    - Latches (5.3)
    - Timing Considerations (5.3)

Sequential Networks

- The logic networks studied so far are combinational networks:
  - The outputs at any instant depend only upon the inputs present at that instant.
- Sequential Network:
  - The outputs at any instant are dependent not only upon the inputs present at that instant but also upon the past history of inputs.
- Sequential networks have memory.
  - The information preserved is referred to as the internal state, secondary state, or state of the network.

Sequential Networks

- Synchronous sequential network
  - Behavior is determined by the values of the signals at only discrete instants of time.
  - Master-clock generator which produces a sequence of clock pulses that sample the input.
- Asynchronous sequential network
  - Behavior of the network is immediately affected by the input signal changes.

Flip-Flop

- The basic logic element that provides memory in many sequential networks.
- Flip-flop itself is a simple sequential network.
  - All sequential networks require the existence of feedback.
  - Feedback is present in flip-flop circuits.
- Flip-flop has two stable conditions.
  - Each of this is associated with a state or storage of a binary symbol.

The Basic Bistable Element

- Central to all flip-flop circuits.
- Has two outputs $Q, \overline{Q}$

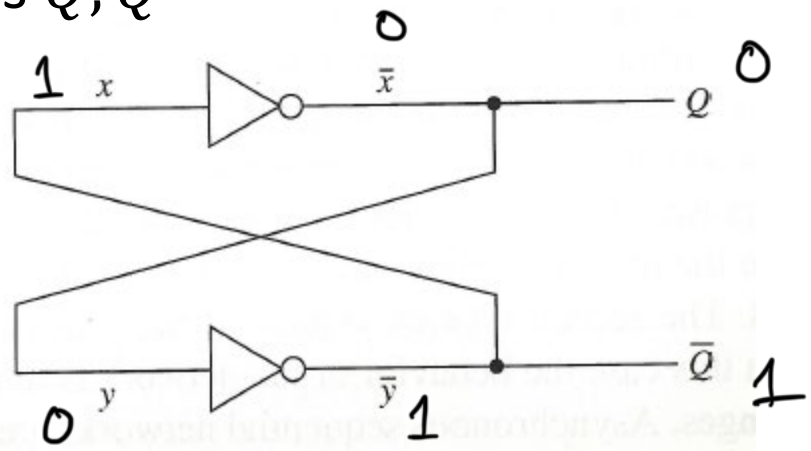


Figure 6.1 Basic bistable element.

- Two stable states:
  - $x = 0; x' = 1; Q = 1; y = 1; y' = 0; Q' = 0; x = 0;$
    - $Q' = x = y' = 0; Q = x' = y = 1$
  - $x = 1; x' = 0; Q = 0; y = 0; y' = 1; Q' = 1; x = 1;$
    - $Q' = x = y' = 1; Q = x' = y = 0$

The Basic Bistable Element

- When output line $Q = 1$ the element is storing a 1; when output line $Q = 0$ the element is storing a 0.

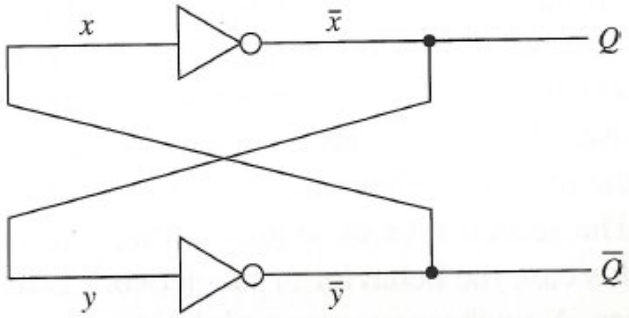


Figure 6.1 Basic bistable element.

- There is one more equilibrium condition that can exist. Occurs when the two output signals are halfway between logic-0 and logic-1.
- Known as metastable state.
  - Any small change causes the element to enter one of its two stable states.
  - Amount of time a device can stay in its metastable state is unpredictable.
  - Metastable state must be avoided.

The Basic Bistable Element

- Has no inputs.
- When power is applied, it becomes stable in one of its two stable states and remains in this state until power is removed.
- To be useful, must be able to force the device into a particular state.
- A flip-flop is a bistable device, with inputs, that remains in a given state as long as power is applied and until input signals are applied to cause its output to change.
- Inputs to flip-flops:
  - Asynchronous or direct input: a signal change produces an immediate change in the state of the flip-flop.
  - Synchronous input: A signal change does not immediately affect the state of the flip-flop. Affects it only when some control signal (clock) occurs.

latch

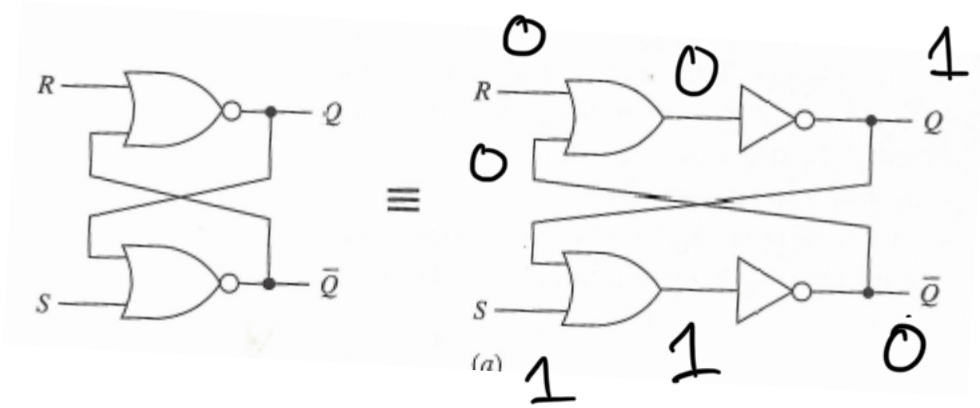
flip-flop

Latches

- Latches are similar to flip-flops
- The timing of the output changes is not controlled
  - The output responds immediately to changes on the input lines.
  - Input lines are continuously being interrogated.
- Section 5.4: flip-flops in which the timing of the output changes is controlled.

The SR (set-reset) Latch

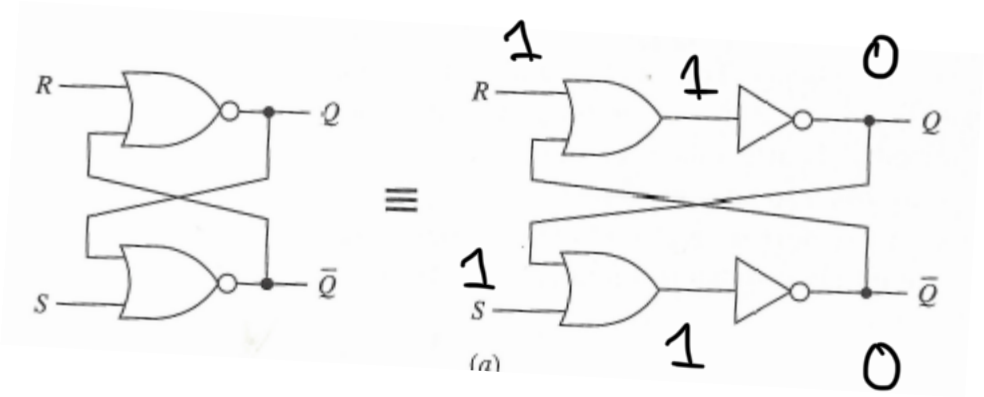
- Cross-coupling of two NOR gates.
- Two inputs: S, R referred to as the set and reset inputs
- Two outputs: $Q, \overline{Q}$



- S = R = 0 logic diagram simplifies to basic bistable element
- R = 1; S = 0—latch is “reset”
- If R is returned to 0 then latch retains its present state
- S = 1; R = 0—latch is “set”
- S,R are asynchronous inputs

The SR (set-reset) Latch

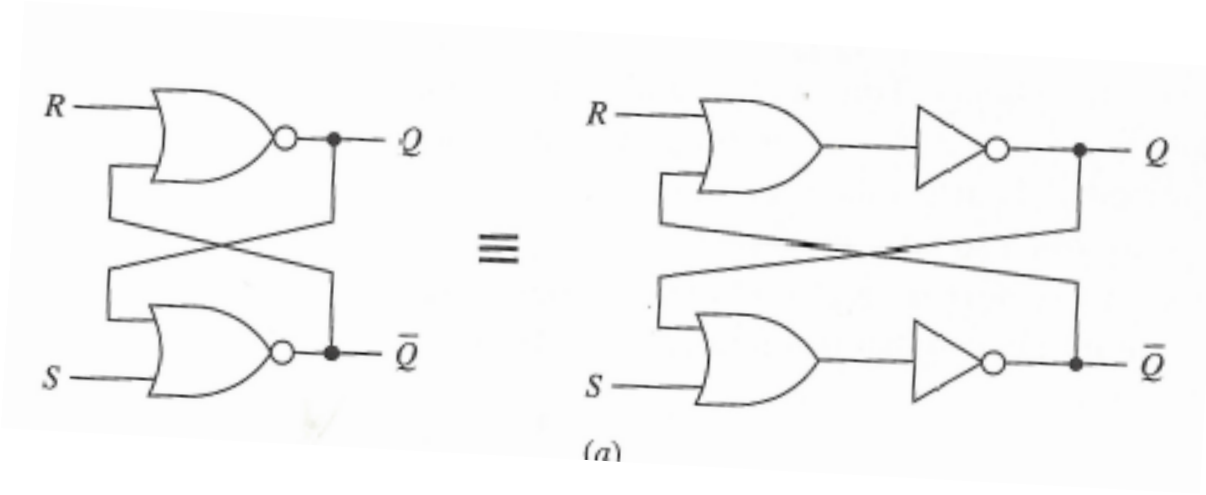
- Cross-coupling of two NOR gates.
- Two inputs: S, R referred to as the set and reset inputs
- Two outputs: $Q, \overline{Q}$



- Consider the case where S = R = 1
  - Output of both NOR gates becomes 0, not complementary
- When inputs return to 0:
  - If one input returns to 0 before the other, the last input to stay at 1 determines the final state.
  - If both inputs return to 0 simultaneously, the device may enter its metastable state. Final state is unpredictable.
- S = R = 1 regarded as “forbidden state”

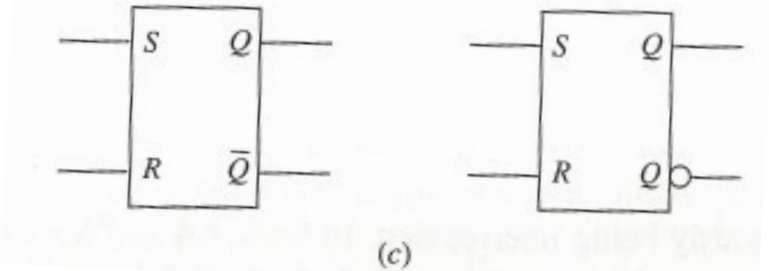
The SR Latch

Next state is the same as the previous state.



Inputs		Outputs	
S	R	Q^+	$\bar{Q}^+$
0	0	Q	$\bar{Q}$
0	1	0	1
1	0	1	0
1	1	0*	0*

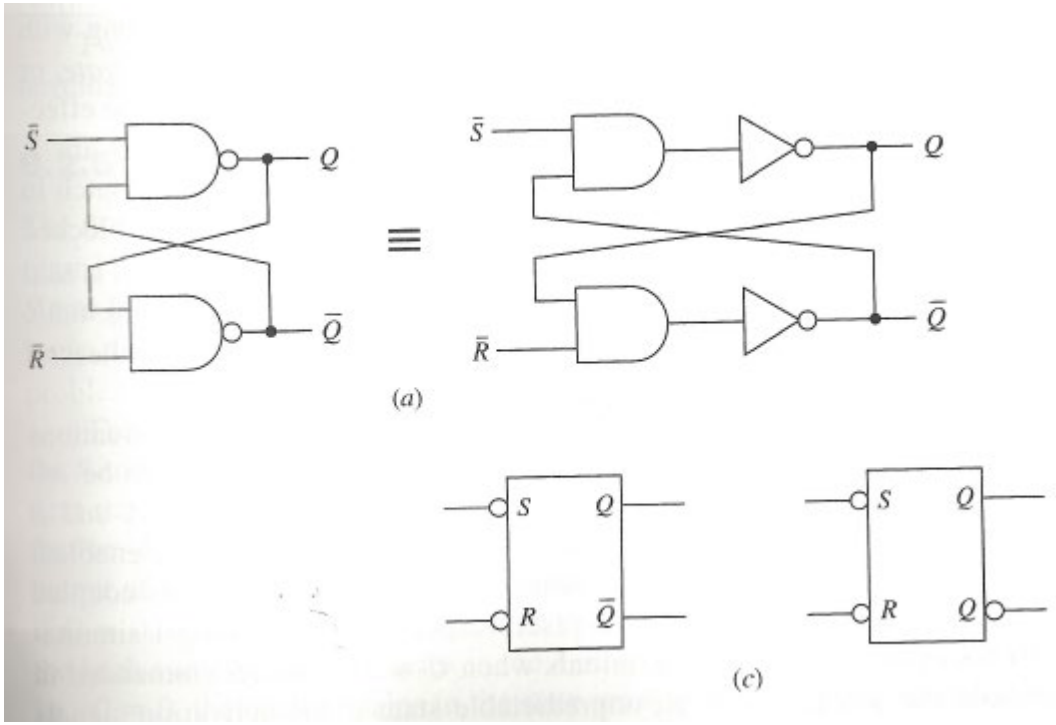
*Unpredictable behavior will result if inputs return to 0 simultaneously



$Q^+, \overline{Q}^+$ indicates the response of the latch at the $Q, \overline{Q}$ output terminals as a consequence of applying the various inputs.
Q^+ is called the next state of the latch.

The $\overline{S}\,\overline{R}$ Latch

- Cross-coupling of two nand-gates
- When $\overline{S} = \overline{R} = 1$ logic diagram reverts to the basic bistable element.
- Device has 2 stable states.



Inputs		Outputs	
$\bar{S}$	$\bar{R}$	Q^+	$\bar{Q}^+$
0	0	1*	1*
0	1	1	0
1	0	0	1
1	1	Q	$\bar{Q}$

*Unpredictable behavior will result if inputs return to 1 simultaneously

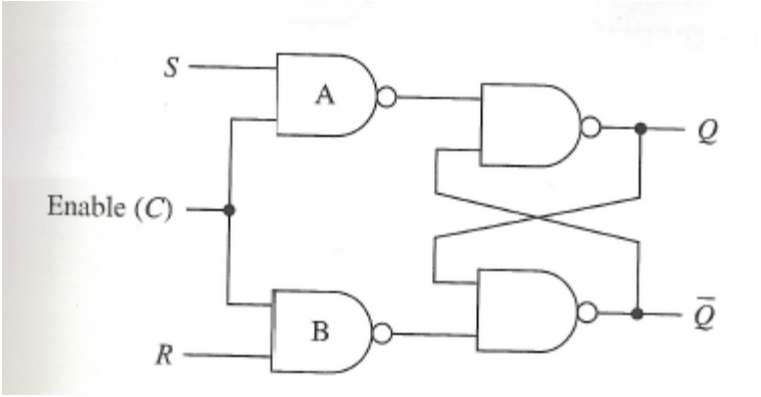
(b)

The Gated SR Latch

- Inputs for SR Latch and $\overline{S}\ \overline{R}$ Latch are asynchronous.
  - A change in the value of the inputs causes an immediate change of the outputs.
- Frequently desirable to prevent input activation signals from affecting the state of the latch immediately.
- "gated SR latch" or "SR latch with enable" is used.

The Gated SR Latch

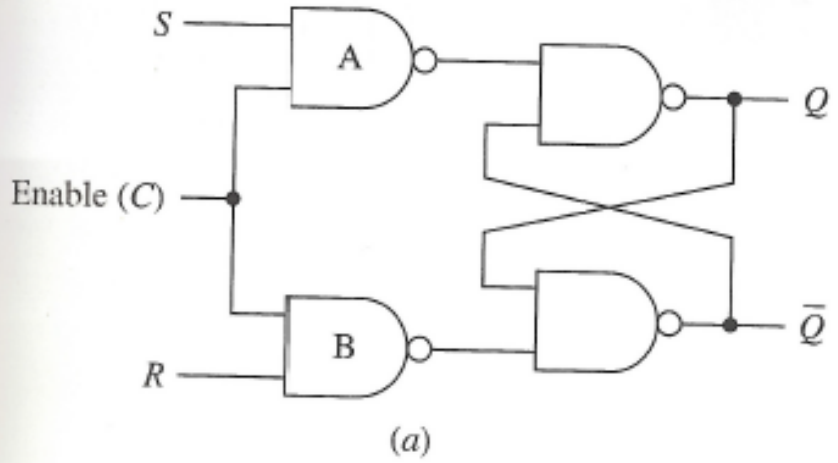
- $\overline{S}\,\overline{R}$ Latch along with 2 additional NAND gates and a control input C.
  - C is referred to as enable, gate or clock input.
- C determines when the S and R inputs become effective.



- As long as C input is 0, outputs of NAND gates are 1, keeps the $\overline{S}\,\overline{R}$ Latch in its current stable state.
  - Any changes to S,R are blocked.
  - Output is "latched" in its present state.
- When C is 1, the latch behaves as an SR Latch.
- If S = R = C = 1 then $Q = \overline{Q} = 1$.
  - If C then goes to 0, can enter metastable state.

The Gated SR Latch



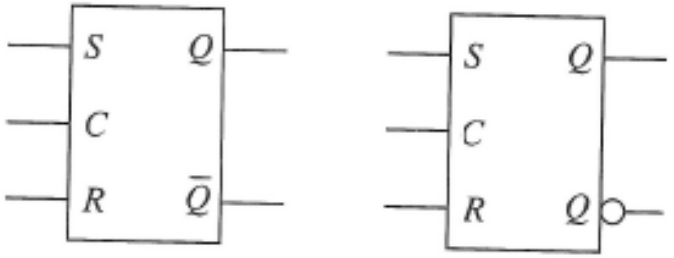


(a)

Inputs			Outputs	
S	R	C	Q^+	$\overline{Q}^+$
0	0	1	Q	$\overline{Q}$
0	1	1	0	1
1	0	1	1	0
1	1	1	1*	1*
X	X	0	Q	$\overline{Q}$

*Unpredictable behavior will result if S and R return to 0 simultaneously or C returns to 0 while S and R are 1

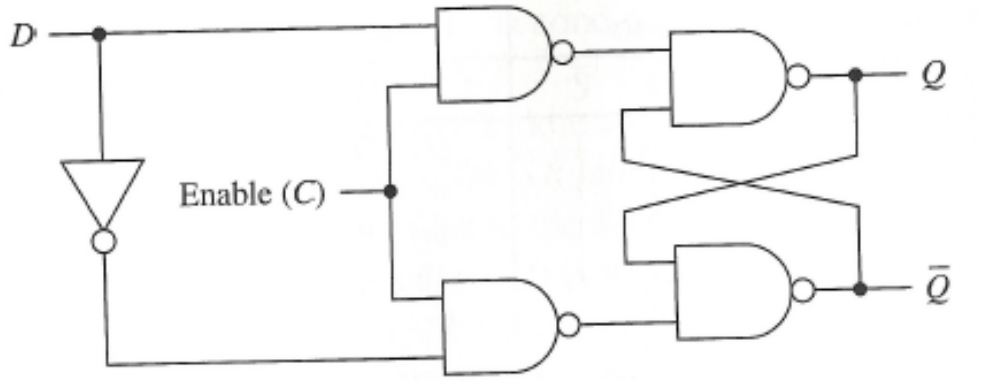
(b)



(c)

The Gated D Latch

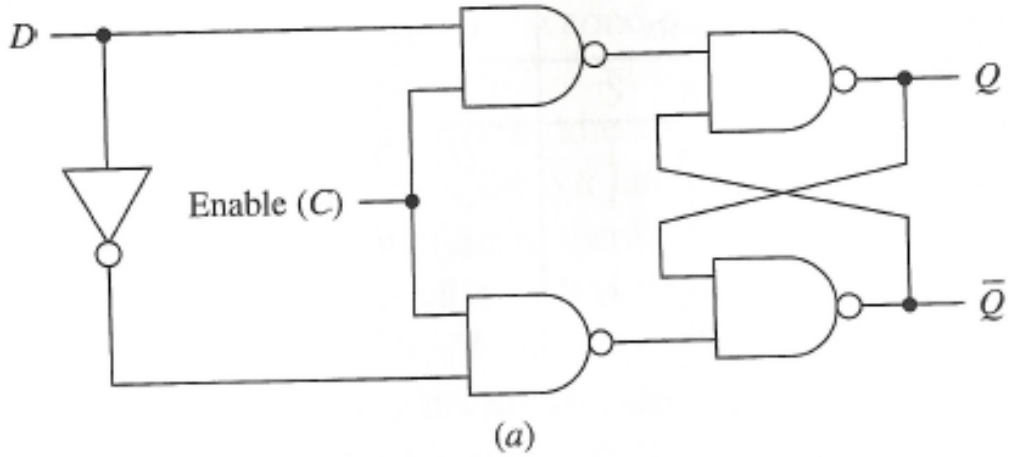
- The latches discussed thus far each has an input combination that is not recommended.
- The gated D (data) latch does not have this problem.
- Gated SR-latch in which a not-gate is connected between the S and R terminals.



(a)

- Why does this help?

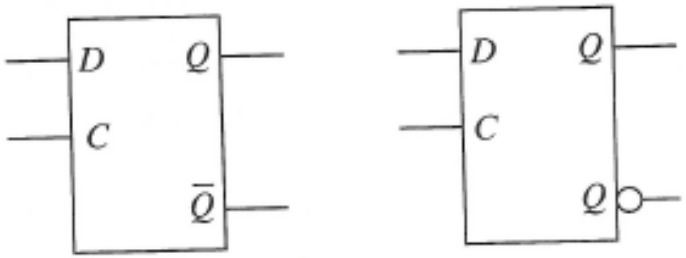
The Gated D Latch



(a)

Inputs		Outputs	
D	C	Q^+	$\overline{Q}^+$
0	1	0	1
1	1	1	0
X	0	Q	$\overline{Q}$

(b)



(c)

Timing Considerations

- Responses to inputs are not really immediate, but occur after some appropriate time delay.
- To achieve desired responses, certain timing constraints must be satisfied.

Propagation Delays

- The propagation delay is the time it takes a change in an input signal to produce a change in an output signal.
- Propagation delay from low to high: t_{pLH}
- Propagation delay from high to low: t_{pHL}

In general, these may be different.

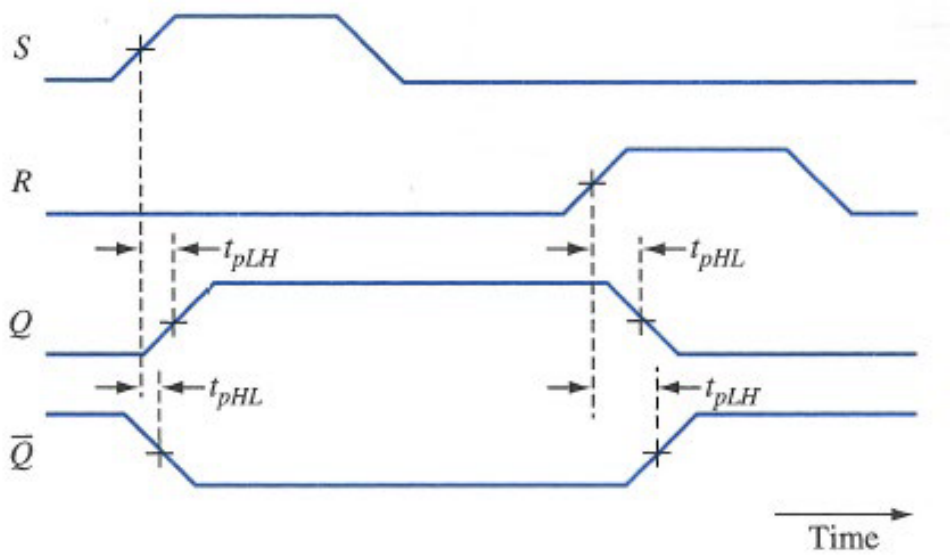


Figure 6.7 Propagation delays in an *SR* latch.

Timing Diagram

- Propagation delays from high-low, low-high assumed equal.
- When S = R = 1, both $Q, \overline{Q}$ become 0.
- t_{15}, signals on S, R are simultaneously changed from 1 to 0.
  - Response of latch is unpredictable. Can be in 0-state, 1-state or metastable state.
  - Application of 1 on the set input terminal returns the latch to predictable.

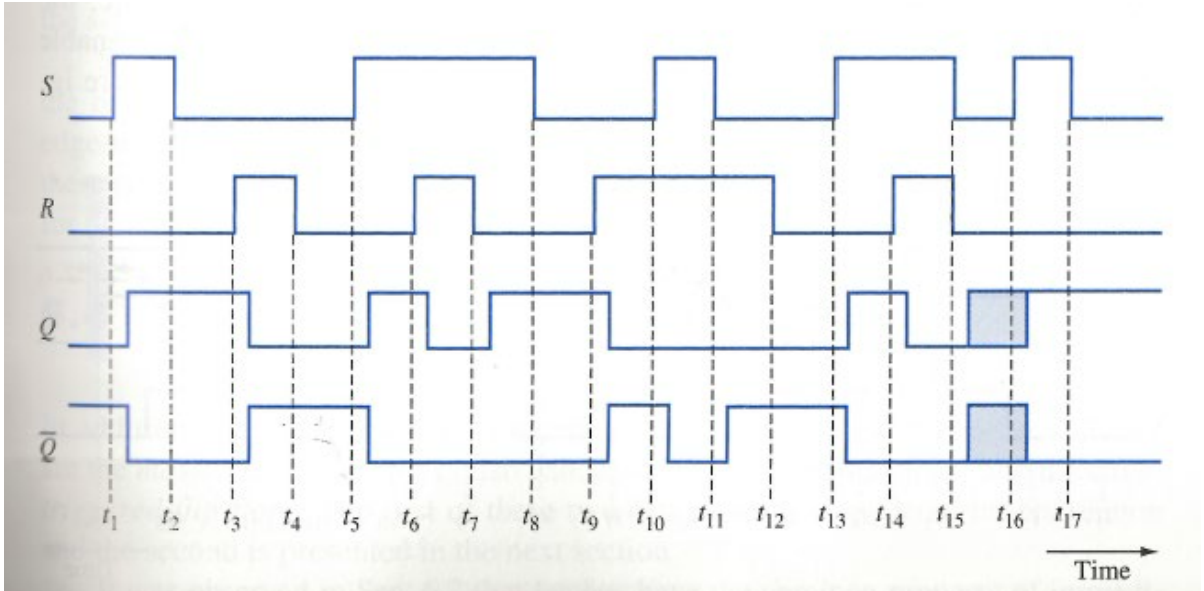
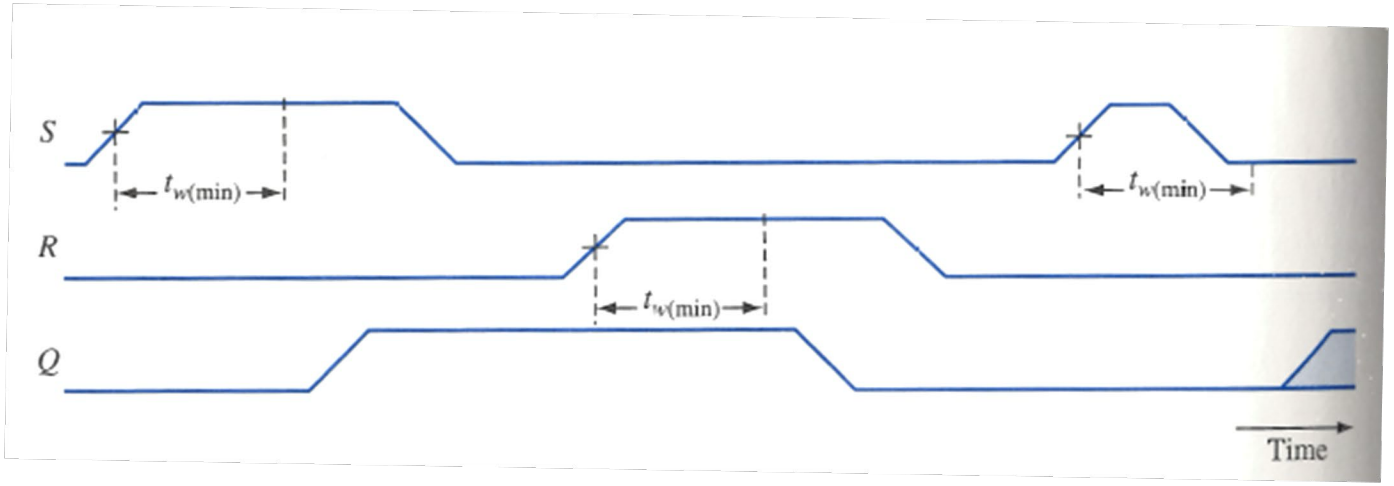


Figure 6.8 Timing diagram for an *SR* latch.

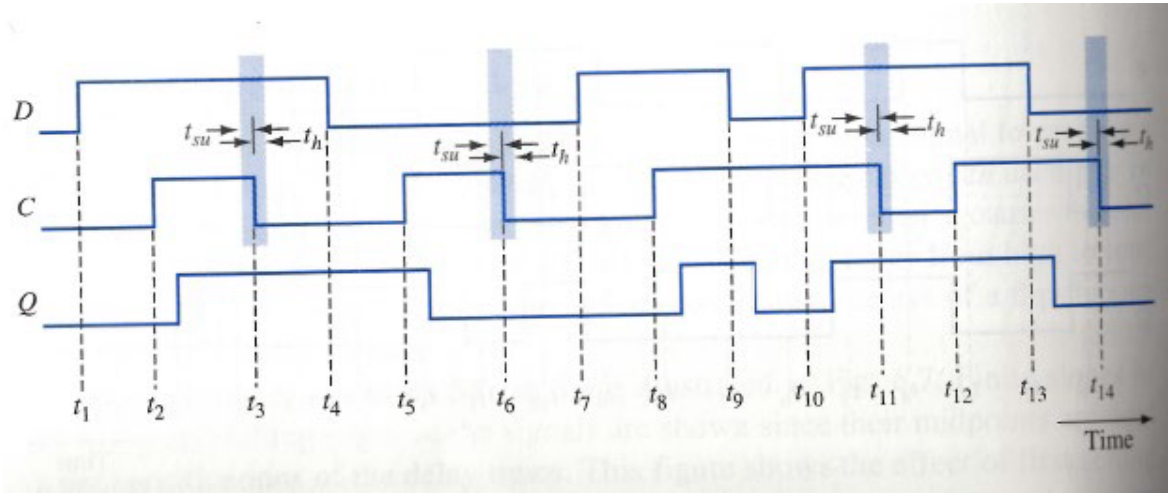
Minimum Pulse Width

- Another specification stated by the manufacturers of latches is that of a minimum pulse width $t_{w(min)}$.
  - Minimum amount of time a signal must be applied in order to produce a desired result.
- Failure to satisfy the constraint may cause unintended change or have the latch enter its metastable state.



Setup and Hold Times

- Consider timing diagram for a gated D latch
- Q-output follows the input signal at D whenever the enable signal C = 1.
- When C = 0, changes are ignored.



- Consider times t_3, t_6, t_{11}, t_{14}.
  - C is returned to 0. Output latches onto its current state.
  - To guarantee latching action: constraint is placed on D signal. Must not change right before and after C goes from 1 to 0.
- Setup time: minimum time t_{su} that D signal must be held fixed before the latching action.
- Hold time: minimum time t_h that D signal must be held fixed after the latching action.

Unpredictable Response in a gated D latch

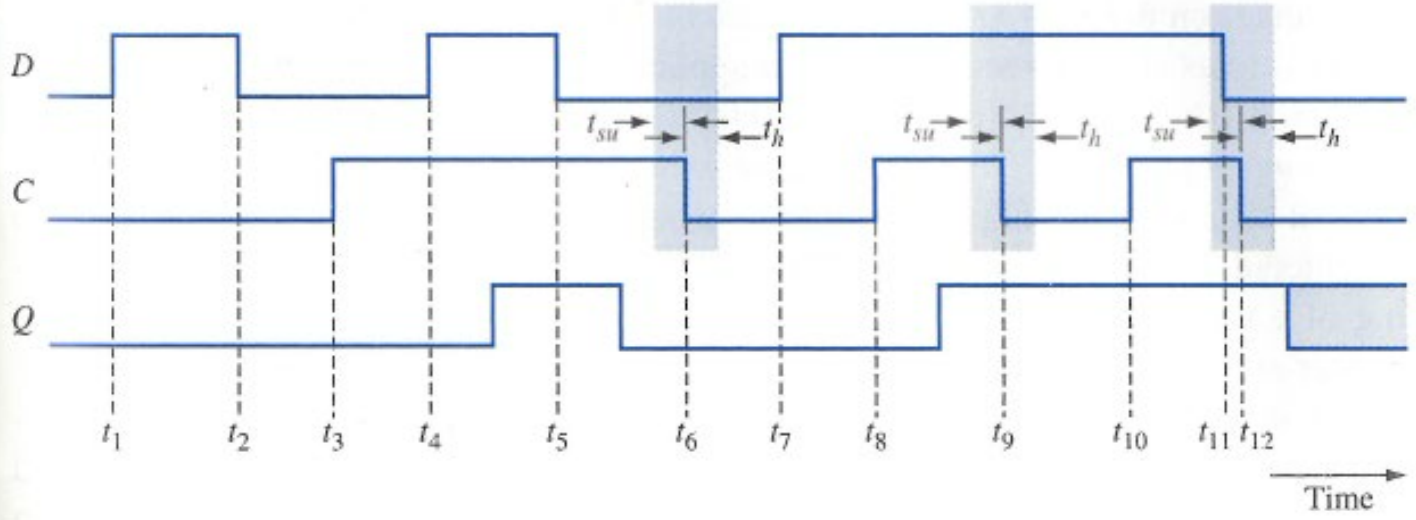


Figure 6.11 Illustration of an unpredictable response in a gated *D* latch.