ENEE244-010x
Digital Logic Design

Lecture 8

Announcements

- Midterm on Wednesday, Oct. 7.
- List of topics for Midterm already up on course webpage.
  - Review sheet will be posted by end of week.
- Review session with UTF’s Bryan and Frank in class on Monday, Oct. 5.

Agenda

- Last time:
  - NAND/NOR Gate Realizations (3.9.4-3.9.6)
  - Some examples of Synthesis Procedure
- This time:
  - Gate Properties (3.10)
  - The simplification problem (4.1)
  - Prime Implicants (4.2)
  - Prime Implicates (4.3)

Gate Properties

Gate Properties

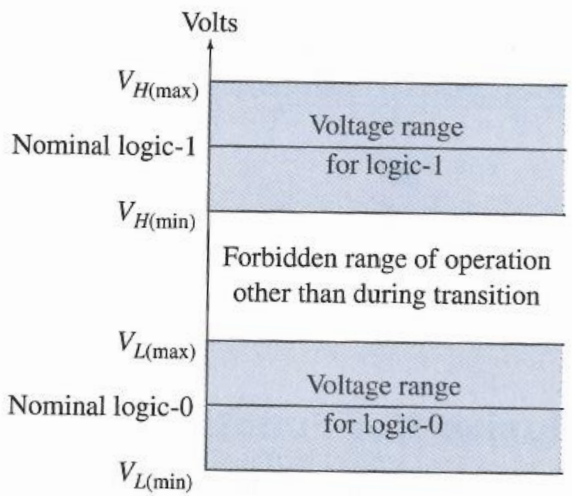
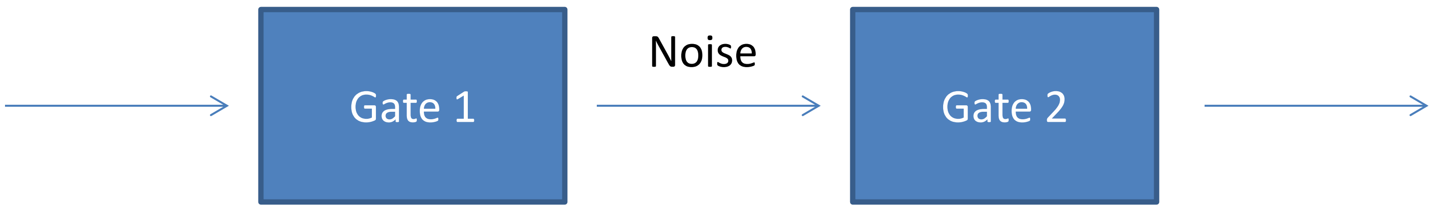


Figure 3.20 Voltage ranges of logic inputs for positive logic.

- The two signal values associated with logic-0 and logic-1 are actually ranges of values.
- If signal value is in some low-level voltage range between $V_{L(min)}$ and $V_{L(max)}$ then it is assigned to logic-0. When a signal value is in some high-level voltage range between $V_{H(min)}$ and $V_{H(max)}$ it is assigned to logic-1.

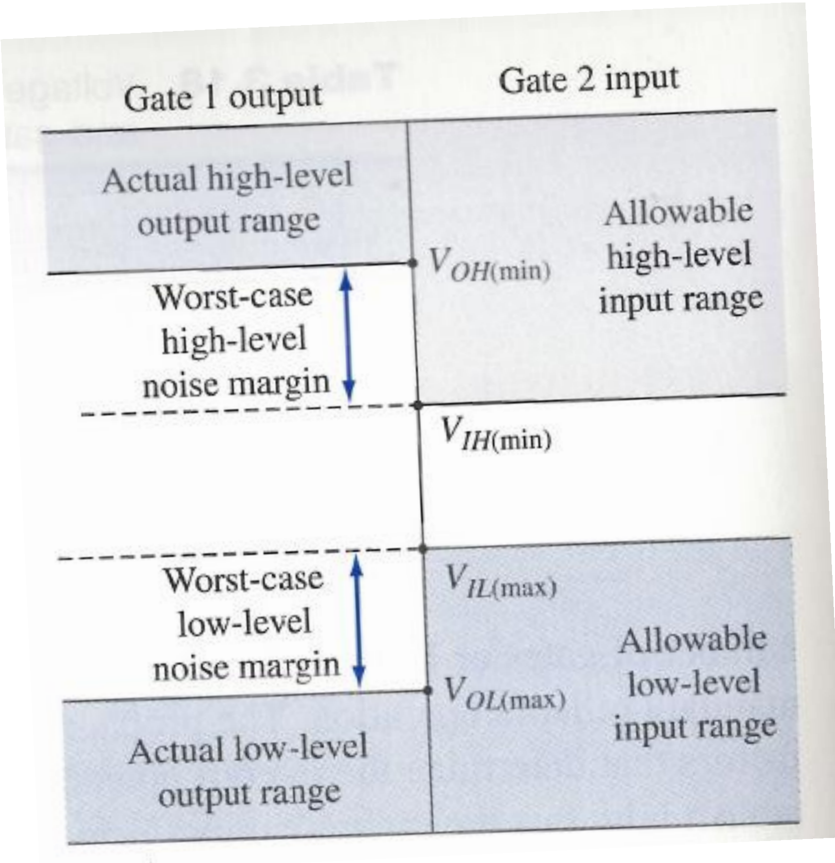
Noise Margins

- Noise: Random fluctuation in an electrical signal
- Must ensure circuit computes correctly even in the presence of noise.



- The minimal signal value that is acceptable as a logic-1 at the input to a gate is different from the minimal logic-1 signal value that a gate produces at its output.
- Assume output of Gate 1 is exactly at $V_{L(max)}$ and then noise increases the signal further. How will the signal be interpreted?
- Same situation with $V_{H(min)}$.

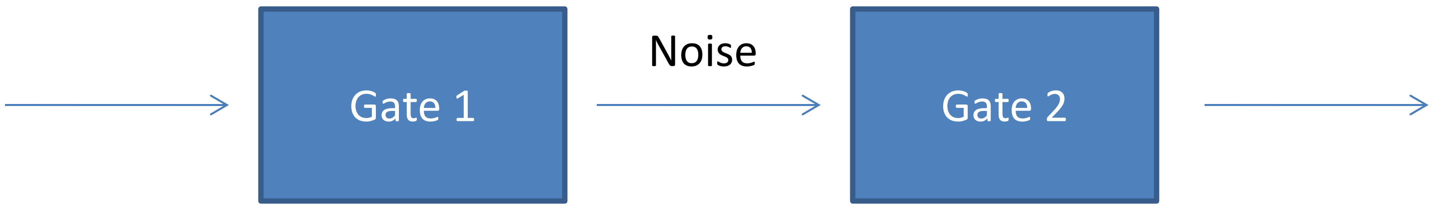
Noise Margins



- $V_{L(max)}$ is different for the input/output of a gate!
- Same situation with $V_{H(min)}$.
- Manufacturers normally state a $V_{IL(max)}, V_{IH(min)}, V_{OL(max)}, V_{OH(min)}$ in gate specifications.
- Where $V_{OL(max)} < V_{IL(max)} < V_{IH(min)}, < V_{OH(min)}$

Noise Margins

- Again consider connecting output of gate to another gate, where noise is induced between the two gates.



- Worst case low-level noise margin: Any noise less than $V_{IL(max)} - V_{OL(max)}$ does not affect behavior of Gate 2 on a low-level signal.
- Worst case high-level noise margin: Any noise less than $V_{OH(min)} - V_{IH(min)}$ does not affect behavior of Gate 2 on a high-level signal.

Fan-Out

- The signal value at the output of a gate is dependent upon the number of gates to which the output is connected.
- Limitation on number of gates output can connect to. This is known as the fan-out capability of the gate. Manufacturers specify this limitation.
- Circuits known as buffers serve as amplifiers for this purpose.

Propagation Delays

- Digital signals to not change instantaneously. Limitation to the overall speed of operation associated with a gate.
- These time delays are called propagation delays.
- Time required for output signal to change from high-level to low-level is t_{pHL}.
- Time required for output signal to change from low-level to high-level is t_{pLH}.
- t_{pHL} and t_{pLH} are, in general, not equal. Manufacturers give maximum times in gate specifications.
- General measure used is the average propagation delay time, t_{pd}

$$t_{pd} = \frac{t_{pHL}+t_{pLH}}{2}$$

Propagation Delay Times

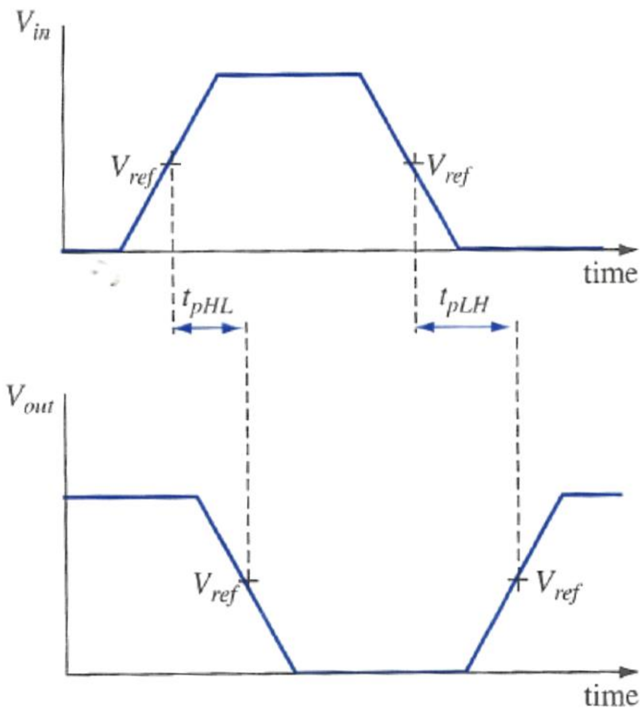


Figure 3.22 Propagation delay times.

t_{pHL}: Time required for output signal to change from high-level to low-level.
t_{pLH}: Time required for output signal to change from low-level to high-level.

Power Dissipation

- Digital circuit consumes power as a result of the flow of currents. Called power dissipation.
- Desirable to have low power dissipation and low propagation delay times.
- These two performance parameters are in conflict with each other.
- Common measure of gate performance is the product of the propagation delay and the power dissipation of the gate.
- This is known as the delay-power product.

Beginning of Exam 2 Material

Simplification of Boolean Expressions

Formulation of the Simplification Problem

- What evaluation factors for a logic network should be considered?
  - Cost (of components, design, construction, maintenance)
  - Reliability (highly reliable components, redundancy)
  - Time it takes for network to respond to changes at its inputs.

Minimal Response Time

- Achieved by minimizing the number of levels of logic that a signal must pass through.
- Always possible to construct any logic network with at most two levels under the double-rail logic assumption.
  - Why?

Minimal Component Cost

- Assume this is the only other factor influencing the merit evaluation of a logic network.
- In general, there are many two-level realizations.
- Determine the normal formula with minimal component cost.
- Number of gates is one greater than the number of terms with more than one literal in the expression.
  - Example: $xy + \overline{x}\,\overline{y}\,\overline{z} + xyz$
  - # of gates: 4
- Number of gate inputs is equal to the number of literals in the expression plus the number of terms containing more than one literal.
  - Example: $xy + \overline{x}\,\overline{y}\,\overline{z} + xyz$
  - # of gate inputs: 11
- Using these criteria can obtain a measure of a Boolean expression's complexity called the cost of the expression.

The Simplification Problem

- The determination of Boolean expressions that satisfy some criterion of minimality is the simplification or minimization problem.
- We will assume cost is determined by number of gate inputs.

Fundamental Terms

- A product or sum of literals in which no variable appears more than once.
- Can obtain a fundamental term by noting:

$$x + \overline{x} = 1$$

$$x \cdot \overline{x} = 0$$

$$x + x = x$$

$$x \cdot x = x$$

- Example: $\overline{x}yx = 0, \overline{x}y\overline{x} = \overline{x}y$
- Example: $\overline{x} + y + x = 1, \overline{x} + y + \overline{x} = \overline{x} + y$

Prime Implicants

- $f_1$implies f_2 $(f_1 \to f_2)$
  - There is no assignment of values to the n variables that makes f_1 equal to 1 and f_2 equal to 0.
  - Whenever f_1 equals 1, then f_2 must also equal 1.
  - Whenever f_2 equals 0, then f_1 must also equal 0.
- Example:
  - $f_1(x, y, z) = 1$ if and only if binary number xyz is divisible by 4.
  - $f_2(x, y, z) = 1$ if and only if binary number xyz is divisible by 2.
  - $f_1 \to f_2$
- Concept can be applied to terms and formulas.

Examples

- $f_1(x, y, z) = xy + yz,$
$$f_2(x, y, z) = xy + yz + \overline{x}\mathrm{z}$$
$$f_1 \rightarrow f_2$$

- $f_3(x, y, z) = (x + y)(y + z)(\overline{x} + z),$
$$f_4(x + y)(y + z)$$
$$f_3 \rightarrow f_4$$

Examples

- Case of Disjunctive Normal Formula
  - Sum-of-products form: E.g. $f(x, y, z) = xyz + \overline{x}yz + x\overline{y}z$
  - Each of the product terms implies the function being described by the formula: E.g. $xyz \rightarrow f(x, y, z)$
  - Whenever product term has value 1, function must also have value 1.
- Case of Conjunctive Normal Formula
  - Product-of-sums form: E.g. $f(x, y, z) = (x + y + z)(\overline{x} + y + \overline{z})$
  - Each sum term is implied by the function: E.g. $f(x, y, z) \rightarrow (x + y + z)$
  - Whenever the sum term has value 0, the function must also have value 0.

Subsumes

- A term t_1 is said to subsume a term t_2 iff all the literals of the term t_2 are also literals of the term t_1.
- Example: $x\overline{y}\,\overline{z}, x\overline{z}$

  $x + \overline{y} + \overline{z}, x + \overline{z}$
- If a product term t_1 subsumes a product term t_2, then t_1 implies t_2.
  - Why?
- If a sum term t_3 subsumes a sum term t_4, then t_4 implies t_1.
  - Why?

Subsumes

- Theorem:
  - If one term subsumes another in an expression, then the subsuming term can always be deleted from the expression without changing the function being described.
- CNF: $(x + y)(x \ + \ y \ + \ z)$
  - $(x + y) \rightarrow (x + y + z)$
- DNF: $xy + xyz$
  - $xyz \rightarrow xy$

Implicants and Prime Implicants

- A product term is said to be an implicant of a complete function if the product term implies the function.
- Each of the minterms in minterm canonical form is an implicant of the function.
- An implicant of a function is a prime implicant if the implicant does not subsume any other implicant with fewer literals.

Example

x	y	z	f
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

$\overline{x}\,\overline{y}z$ is also an implicant

$x\overline{y}z$ is an implicant. Is it a prime implicant?

$\overline{y}z$ is an implicant.
Is it a prime implicant?
Yes. $\overline{y}, z$ are not implicants