Announcements

• Homework 8 up on course webpage. Due Monday, 11/23
Agenda

• Last time:
  – The Basic Bistable Element (6.1)
  – Latches (6.2)
  – Timing Considerations (6.3)

• This time:
  – Review of 6.2-6.3
  – Master-Slave Flip-Flops (6.4)
  – Edge-Triggered Flip-Flops (6.5)
  – Characteristic Equations (6.6)
Review--The SR Latch

\( Q^+, \overline{Q}^+ \) indicates the response of the latch at the \( Q, \overline{Q} \) output terminals as a consequence of applying the various inputs. \( Q^+ \) is called the next state of the latch.
Review--The Gated SR Latch

(a) Diagram of the gated SR latch with inputs $S$, $R$, and $C$, and outputs $Q$ and $\bar{Q}$, along with an enable input $C$.

(b) Truth table for the gated SR latch:

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S$</td>
<td>$R$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>$X$</td>
<td>$X$</td>
</tr>
</tbody>
</table>

*Unpredictable behavior will result if $S$ and $R$ return to 0 simultaneously or $C$ returns to 0 while $S$ and $R$ are 1.

(c) Different representations of the gated SR latch circuit.
Review--The Gated D Latch
Propagation Delays

- The propagation delay is the time it takes a change in an input signal to produce a change in an output signal.
- Propagation delay from low to high: $t_{pLH}$
- Propagation delay from high to low: $t_{pHL}$

In general, these may be different.
Timing Diagram

- Propagation delays from high-low, low-high assumed equal.
- When $S = R = 1$, both $Q$, $\overline{Q}$ become 0.
- $t_{15}$, signals on $S$, $R$ are simultaneously changed from 1 to 0.
  - Response of latch is unpredictable. Can be in 0-state, 1-state or metastable state.
  - Application of 1 on the set input terminal returns the latch to predictable.
Minimum Pulse Width

• Another specification stated by the manufacturers of latches is that of a minimum pulse width $t_w(min)$.
  
  – Minimum amount of time a signal must be applied in order to produce a desired result.

• Failure to satisfy the constraint may cause unintended change or have the latch enter its metastable state.
Setup and Hold Times

- Consider timing diagram for a gated D latch
- Q-output follows the input signal at D whenever the enable signal C = 1.
- When C = 0, changes are ignored.

- Consider times $t_3, t_6, t_{11}, t_{14}$.
  - C is returned to 0. Output latches onto its current state.
  - To guarantee latching action: constraint is placed on D signal. Must not change right before and after C goes from 1 to 0.

- Setup time: minimum time $t_{su}$ that D signal must be held fixed before the latching action.
- Hold time: minimum time $t_h$ that D signal must be held fixed after the latching action.
Unpredictable Response in a gated D latch

Figure 6.11 Illustration of an unpredictable response in a gated D latch.
Master-Slave Flip-Flops
(Pulse Triggered Flip-Flops)

• Aside from latches, two categories of flip-flops.
  – Master-slave flip-flops (pulse-triggered flip-flops)
  – Edge-triggered flip-flops

• Latches have immediate output response (known as transparency)

• May be undesirable:
  – May be necessary to sense the current state of a flip-flop while allowing new state information to be entered.
Master-Slave SR Flip-Flop

- Two sections, each capable of storing a binary symbol.
- First section is referred to as the master and the second section as the slave.
- Information is entered into the master on one edge or level of a control signal and is transferred to the slave on the next edge or level of the control signal.
- Each section is a latch.
Master-Slave SR Flip-Flop

- **C = 0:**
  - Master is disabled. Any changes to S,R ignored.
  - Slave is enabled. Is in the same state as the master.

- **C = 1:**
  - Slave is disabled (retains state of master)
  - Master is enabled, responds to inputs. Changes in state of master are not reflected in disabled slave.

- **C = 0:**
  - Master is disabled.
  - Slave is enabled and takes on new state of the master.

- **Important:** For short periods during rising and falling edges, both master and slave are disabled.
Master-Slave SR Flip-Flop

Slave only takes on state of the master at $t_4$.

Postponed output indicator: output change postponed until end of pulse.

If $S, R = 1$ when control signal goes from high to low we are in an unpredictable state. Can cause metastable state.

Pulse symbol indicates master enabled when $C = 1$ and state of master transferred to slave at the end of the pulse period.
Timing Diagram for Master-Slave SR flip-flop
Master-Slave JK Flip-Flop

• The output state of a master-slave SR flip-flop is undefined upon returning the control input to 0 when $S = R = 1$.
  – Necessary to avoid this condition.

• Master-slave JK flip-flop allows its two information input lines to be simultaneously 1.
  – Results in toggling the output of the flip flop.
• Assume in 1-state, $C = 0$, $J = K = 1$.
  – Due to feedback, the output of the J-gate is 0, output of K-gate is 1.
  – If clock is changed to $C = 1$ then master is reset.
• Assume in 0-state, $C = 0$, $J = K = 1$.
  – Due to feedback, the output of the J-gate is 1, output of K-gate is 0.
  – If clock is changed to $C = 1$ then master is set.
• 1 on J input line, 0 on K input line sets the flip-flop.
  – If in 1-state, unchanged b/c $S,R$ set to 0.
  – If in 0-state, $S$ set to 1, R set to 0.
• 0 on J input, 1 on K input line resets the flip-flop. Why?
Master-Slave JK Flip-Flop

Master-slave JK flip-flop

Clock \( C \)

\( J \)

\( K \)

\( S \)

\( C \)

\( R \)

\( Q_\text{M} \)

\( \overline{Q_\text{M}} \)

\( Q_\text{S} \)

\( \overline{Q_\text{S}} \)

\( Q \)

\( \overline{Q} \)

Inputs

\( J \)

\( K \)

\( C \)

Outputs

\( Q^+ \)

\( \overline{Q}^+ \)

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td>0  \overline{\overline{Q}}</td>
</tr>
<tr>
<td>0 1 1</td>
<td>0  \overline{1}</td>
</tr>
<tr>
<td>1 0 0</td>
<td>1  \overline{0}</td>
</tr>
<tr>
<td>1 1 1</td>
<td>\overline{\overline{Q}}  2</td>
</tr>
<tr>
<td>X X 0</td>
<td>0  \overline{\overline{Q}}</td>
</tr>
</tbody>
</table>

(a)

(b)

(c)
Timing Diagram for Master-Slave JK Flip-Flop
0’s and 1’s Catching

- The master is enabled during the entire period the control-signal is 1.
- If the slave latch is in its 1-state, then a logic-1 on K-input line causes the master-latch to reset. Slave becomes reset when control signal returns to 0.
- This is known as 0’s catching (2\textsuperscript{nd} pulse).
  - Note: if a subsequent 1-signal on J input line and C is still 1, master does not become set again (due to feedback not changing).
- If slave latch is in 0-state, logic-1 on J input line while control signal is 1 causes the master latch to be set and slave will be set upon occurrence of the falling edge.
- This is known as 1’s catching (3\textsuperscript{rd} pulse).
- In many applications, 0’s and 1’s catching behavior is undesirable. Normally recommended that the J and K input values should be held fixed during the entire interval the master is enabled.
- Any changes in J, K must occur while the control signal is 0.
0’s Catching

- Assume in 1-state ($Q = 1, \overline{Q} = 0$), $C = 1, J = 0, K = 0$
- $K$ gets set to 1 briefly.
  - Master gets reset, Slave will become reset when Clock goes to 0.
- $K$ goes to 0.
- $J$ goes to 1. What happens?
- Nothing! Slave will still become reset when Clock goes to 0.
- Why?