SR-Latch

Logic Diagram

Truth Table

Symbol

Gated SR-Latch
Gated D-Latch

Master-Slave SR Flip-Flop
Master-Slave JK Flip-Flop

Positive Edge Triggered D Flip-Flop

Figure 6.18 Positive-edge-triggered D flip-flop. (a) Logic diagram, (b) Function table where $Q'$ denotes the output $Q$ in response to the inputs. (c) Two logic symbols.
Positive Edge-Triggered T Flip-Flop

**Figure 6.23** Positive-edge-triggered T flip-flop. (a) Logic diagrams. (b) Function table where $Q^*$ denotes the output $Q$ in response to the inputs. (c) Two logic symbols.