

References

- S. G. Abraham, R. A. Sugumar, D. Windheiser, B. R. Rau, and R. Gupta. 1993. "Predictability of load/store instruction latencies." In Proc. 26th Ann. Int. Symp. on Microarchitecture (MICRO 1993), pp. 139–152, Austin, TX, December 1993.
- M. Accetta, R. Baron, W. Bolosky, D. Golub, R. Rashid, A. Tevanian, and M. Young. 1986. "Mach: A new kernel foundation for UNIX development." In USENIX Technical Conference Proceedings, 1986.
- M. Adiletta, M. Rosenbluth, D. Bernstein, G. Wolrich, and H. Wilkinson. 2002. "The next generation of Intel IXP Network processors." *Intel Technol. J.*, 6(3), Aug. 2002. <http://developer.intel.com/technology/itj/2002/volume06issue03/>.
- S. V. Adve, A. L. Cox, S. Dwarkadas, R. Rajamony, and W. Zwaenepoel. 1996. "A comparison of entry consistency and lazy release consistency implementations." In Proc. Second High Performance Computer Architecture Symp. (HPCA 2), pp. 26–37, San Jose, CA, February 1996.
- A. Agarwal, J. Hennessy, and M. Horowitz. 1989. "An analytical cache model." *ACM Trans. Comput. Syst.*, 7(2), 184–215, May 1989.
- A. Agarwal et al. 2003. "A single-Vt low-leakage gated-ground cache for deep submicron." *IEEE J. Solid-State Circuits*, 38(2), 319–328, Feb. 2003.
- A. V. Aho, R. Sethi, and J. D. Ullman. 1988. *Compilers: Principles, Techniques, and Tools*. Addison-Wesley, Reading, MA, 1988.
- A. Aiken and A. Nicolau. 1988. "A development environment for horizontal microcode." *IEEE Trans. Software Eng.*, 14(5), 584–594, May 1988.
- J. Alakarhu. 2002. "A comparison of precharge policies with modern DRAM architectures." Proc. 9th Int. Conf. Eletronics, Circuits and Systems, vol. 2, pp. 823–826, Sept. 2002.
- K. Albayraktaroglu, A. Jaleel, X. Wu, M. Franklin, B Jacob, C. Tseng, and D. Yeung. 2005. "BioBench: A benchmark suite of bioinformatics applications." In Proc. 2005 IEEE Int. Symp. Performance Analysis of Systems and Software (ISPASS 2005). Austin, TX, March 2005.
- T. R. Albrecht, J. U. Bu, M. Despont, E. Eleftheriou, and T. Hirano. 2004. Chapter 6: MEMS in mass storage systems. In Baltès, H., Brand, O., Fedder, G. K., Hierold, C., Korvink, J. G., and Tabata, O., Eds., *Enabling Technologies for MEMS and Nanodevices*. John Wiley & Sons, Hoboken, NJ, 2004.
- T. Alexander and G. Kedem. 1996. "Distributed predictive cache design for high performance memory systems." In Second Int. Symp. High-Performance Computer Architecture (ISCA 1996), pp. 254–263, February 1996.
- A. Allara, C. Brandolese, W. Fornaciari, F. Salice, and D. Sciuto. 1998. "System-level performance estimation strategy for SW and HW." In Int. Conf. Computer Design (ICCD 1998), Austin, TX, October 1998.
- B. Amrutur and M. Horowitz. 1994. "Techniques to reduce power in fast wide memories." in Dig. Tech. Papers 1994 Symp. Low Power Electronics, 1994, pp. 92–93.
- B. Amrutur and M. Horowitz. 1998. "A replica technique for wordline and sense control in low-power SRAMs." *IEEE J. Solid State Circuits*, 33, 1208–1219, Aug. 1998.
- B. Amrutur and M. Horowitz. 2000. "Speed and power scaling of SRAMs." *IEEE J. Solid-State Circuits*, 35(2), Feb. 2000.
- B. Amrutur and M. Horowitz. 2001. "Fast low-power decoders for RAMs." *IEEE J. Solid State Circuits*, 36(10), 1506–1515, Oct. 2001.
- Analog Devices. 1996. ADSP-21xx 16-bit DSP Family. <http://www.analog.com/processors/processors/ADSP/index.html>.

- Analog Devices. 2001. SHARC ADSP-21160M 32-bit Embedded CPU. <http://www.analog.com/processors/processors/sharc/index.html>.
- Analog Devices. 2004. TigerSharc ADSP-TS201S 32-bit DSP. Revised Jan. 2004. <http://www.analog.com/processors/processors/tigersharc/index.html>.
- D. Anderson, F. Sparacio, and R. Tomasulo. 1967. "The IBM System/360 Model 91: Machine philosophy and instruction-handling." *IBM J. Res. Dev.*, vol. 11, no. 1, pp. 8–24, Jan. 1967.
- D. Anderson, J. Dykes, and E. Riedel. 2003. "More than an interface—SCSI vs. ATA." In Proc. 2nd Ann. Conf. File and Storage Technology (FAST), San Francisco, CA, 2003.
- T. Anderson, H. M. Levy, B. N. Bershad, and E. D. Lazowska. 1991. "The interaction of architecture and operating system design." In Proc. Fourth Int. Conf. Architectural Support for Programming Languages and Operating Systems (ASPLOS-4), pp. 108–120, 1991.
- F. Angiolini, L. Benini, and A. Caprara. 2003. "Polynomial-time algorithm for on-chip scratchpad memory partitioning." In Proc. 2003 Int. Conf. Compilers, Architectures, and Synthesis for Embedded Systems (CASES 2003), pp. 318–326. ACM Press, New York, 2003.
- F. Angiolini, F. Menichelli, A. Ferrero, L. Benini, and M. Olivieri. 2004. "A postcompiler approach to scratchpad mapping of code." In Proc. 2004 Int. Conf. Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2004), pp. 259–267. ACM Press, New York, 2004.
- M. Anis. 2003. "Subthreshold leakage current: Challenges and solutions." In Proc. 15th Int. Conf. on Microelectronics (ICM 2003), pp. 77–80, 2003.
- A. W. Appel. 1987. "Garbage collection can be faster than stack allocation." *Inf. Process. Lett.*, 25(4), 275–279, June 1987.
- A. W. Appel. 1989. "Simple generational garbage collection and fast allocation." *Software—Practice and Experience*, 19(2), 171–183, Feb. 1989.
- A. W. Appel and K. Li. 1991. "Virtual memory primitives for user programs." In Proc. Fourth Int. Conf. Architectural Support for Programming Languages and Operating Systems (ASPLOS-4), pp. 96–107, 1991.
- Apple Computer, Inc. 1992. *Technical Introduction to the Macintosh Family, 2nd Edition*. Addison-Wesley Publishing Company, Reading, MA, 1992.
- J. Archibald and J. Baer. 1986. "Cache coherence protocols: Evaluation using a multiprocessor simulation model." *ACM Trans. Comput. Syst.* 4(4), 273–298, Sept. 1986.
- ARM. 2004. ARM968E-S 32-bit Embedded Core. Arm, Revised March 2004. <http://www.arm.com/products/CPUs/ARM968E-S.html>.
- K. G. Ashar. 1997. *Magnetic Disk Drive Technology*. IEEE Press, New York, 2004.
- Atmel. 2004. AT91C140 16/32-bit Embedded CPU. Atmel, Revised May 2004. http://www.atmel.com/dyn/resources/prod_documents/doc6069.pdf.
- O. Avissar, R. Barua, and D. Stewart. 2001. "Heterogeneous memory management for embedded systems." In Proc. ACM 2nd Int. Conf. Compilers, Architectures, and Synthesis for Embedded Systems (CASES), November 2001.
- O. Avissar, R. Barua, and D. Stewart. 2002. "An optimal memory allocation scheme for scratch-pad based embedded systems." *ACM Trans. Embedded Systems (TECS)*, 1(1), Sept. 2002.
- J. Y. Babonneau, M. S. Achard, G. Morisset, and M. B. Mounajjed. 1977. "Automatic and general solution to the adaptation of programs in a paging environment." In Proc. Sixth ACM Symp. Operating Systems Principles (SOSP '77), West Lafayette, IN, November 16–18, 1977. ACM Press, New York, 109–116, 1977.
- M. J. Bach. 1986. *The Design of the UNIX Operating System*. Prentice Hall, Inc., Englewood Cliffs, NJ, 1986.
- J.-L. Baer and T.-F. Chen. 1991. "An effective on-chip preloading scheme to reduce data access penalty." In Proc. 1991 ACM/IEEE Conf. Supercomputing (ICS 1991), pp. 176–186, Albuquerque, NM, November 1991.
- J.-L. Baer and G. R. Sager. 1976. "Dynamic improvement of locality in virtual memory systems." *IEEE Trans. Software Eng.*, 2(1), 54–62. Mar. 1976.
- R. J. Baker, H. W. Li, and D. E. Boyce. 1998. *CMOS: Circuit Design, Layout, and Simulation*. IEEE Press, New York, 1998.
- J. Baker. 2002. Personal communication.
- R. J. Baker. 2005. *CMOS: Circuit Design, Layout, and Simulation, 2nd Ed.* IEEE Press and Wiley-Interscience, New York, 2005.
- H. E. Bal, M. F. Kaashoek, and A. S. Tanenbaum. 1992. "Orca: A language for parallel programming of

- distributed systems." *IEEE Trans. Software. Eng.*, 18(3), 190–205, Mar. 1992.
- K. Bala, M. F. Kaashoek, and W. E. Weihl. 1994. "Software prefetching and caching for translation lookaside buffers." In Proc. First USENIX Symp. Operating Systems Design and Implementation (OSDI-1), pp. 243–253, November 1994.
- R. Balan and K. Gollhardt. 1992. "A scalable implementation of virtual memory HAT layer for shared memory multiprocessor machines." In USENIX Technical Conference Proceedings, 1992.
- S. R. Ball. 1996. *Embedded Microprocessor Systems: Real World Design*. Newnes, Butterworth–Heinemann, Boston, MA, 1996.
- R. Banakar, S. Steinke, B.-S. Lee, M. Balakrishnan, and P. Marwedel. 2002. "Scratchpad memory: A design alternative for cache on-chip memory in embedded systems." In Tenth Int. Symp. Hardware/Software Codesign (CODES), pp. 73–78, Estes Park, Colorado, May 2002.
- D. Barrett and B. Zorn. 1993. "Using lifetime predictors to improve memory allocation performance." SIGPLAN'93—Conference on Programming Language Design and Implementation, pp. 187–196, Albuquerque, New Mexico, June 1993.
- L. A. Barroso et al. 1998. "Memory system characterization of commercial workloads." Int. Symp. Computer Architecture (ISCA-25) 3–14, June 1998.
- K. Baynes, C. Collins, E. Fiterman, C. Smit, T. Zhang, and B. Jacob. 2000. "The performance and energy consumption of embedded real-time operating systems." Tech. Rep. UMD-SCA-2000-4, U. Maryland Systems & Computer Architecture Group, November 2000.
- K. Baynes, C. Collins, E. Fiterman, B. Ganesh, P. Kohout, C. Smit, T. Zhang, and B. Jacob. 2001. "The performance and energy consumption of three embedded real-time operating systems." In Proc. Int. Conf. Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2001), pp. 203–210, Atlanta, GA, November 2001.
- K. Baynes, C. Collins, E. Fiterman, C. Smit, T. Zhang, and B. Jacob. 2003. "The performance and energy consumption of embedded real-time operating systems." *IEEE Trans. Computers*, 52(11), 1454–1469, Nov. 2003.
- H. Becker. 2002. Personal communication.
- L. A. Belady. 1966. "A study of replacement algorithms for virtual storage." *IBM Syst. J.*, 5(2), 78–101, 1966.
- T. Bell, I. H. Witten, and J. G. Cleary. 1989. "Modeling for text compression." *ACM Comput. Surv.*, 21(4), 557–591, Dec. 1989.
- L. Benini and G. D. Micheli. 1998. "System-level power optimization: Techniques and tools." In Int. Symp. Low Power Electronics and Design (ISLPED), pp. 288–293, Monterey CA, August 1998.
- J. K. Bennett, J. B. Carter, and W. Zwaenepoel. 1990a. "Adaptive software cache management for distributed shared memory architectures." In Proc. 17th Int. Symp. Computer Architecture (ISCA), pp. 148–159, May 1990.
- J. K. Bennett, J. B. Carter, and W. Zwaenepoel. 1990b. "Adaptive software cache management for distributed shared memory architectures." In Proc. 17th Annual Int. Symp. Computer Architecture (ISCA'90), pp. 125–135, 1990.
- J. K. Bennett, J. B. Carter, and W. Zwaenepoel. 1990c. "Munin: Distributed shared memory based on type-specific memory coherence." In Proc. 2nd ACM Symp. Principles and Practice of Parallel Programming (PPoPP), pp. 168–177, March 1990.
- A. Bensoussan, C. T. Clingen, and R. C. Daley. 1972. "The Multics virtual memory: Concepts and design." *Commun. ACM*, 15(5), 308–318, May 1972.
- B. Bershad and M. Zekauskas. 1991. Shared Memory Parallel Programming with Entry Consistency for Distributed Memory Multiprocessors, CMU Technical Report CMU-CS-91-170, September 1991.
- B. Bershad, M. Zekauskas, and W. Sawdon. 1993. "The Midway distributed shared memory system." In Proc. IEEE CompCon Conference, 1993.
- B. Bershad, D. Lee, T. Romer, and J. Chen. 1994a. "Avoiding conflict misses dynamically in large direct-mapped caches." In Proc. Sixth Int. Conf. Architectural Support for Programming Languages and Operating Systems (ASPLOS'94), pp. 158–170, San Jose, CA, 1994.
- B. Bershad, C. Chambers, S. Eggers, C. Maeda, D. McNamee, P. Pardyak, S. Savage, and E. Sirer. 1994b. SPIN—An Extensible Microkernel for Application-Specific Operating System Services, Technical Report 94-03-03, University of Washington, 1994.
- H. N. Bertram. 1994. *Theory of Magnetic Recording*. Cambridge University Press, Cambridge, UK, 1994.
- A. Bestavros, R. L. Carter, M. E. Crovella, C. R. Cunha, A. Beddaya, and S. A. Mirdad. 1990. "Application-level

- document caching in the internet." In Proc. Second Int. Workshop on Services in Distributed and Networked Environments (SDNE)'95, pp. 125–135, 1990.
- D. Bhandarkar and J. Ding. 1997. "Performance characterization of the Pentium Pro processor." Int. Symp. High Performance Computer Architecture (HPCA-3), pp. 288–297, February 1997.
- S. S. Bhattacharyya, P. K. Murthy, and E. A. Lee. 1996. *Software Synthesis from Dataflow Graphs*. Kluwer Academic, Dordrecht/Norwell, MA, 1998.
- S. S. Bhattacharyya, P. K. Murthy, and E. A. Lee. 1998. "Synthesis of embedded software from synchronous dataflow specifications (invited paper)." *J. VLSI Signal Processing*, 1998.
- B. Bhushan, M. Dominiak, and J. P. Lazzari. 1992. "Contact-start-stop studies with silicon planar head sliders against thin-film disks." *IEEE Trans. Magnetics*, 28(5), 2874–2876, 1992.
- L. Birkedal, M. Tofte, and M. Vejlstrup. 1996. "From region inference to von neumann machines via region representation inference." In Proc. 23rd ACM SIGPLAN-SIGACT Symp. Principles of Programming Languages, pp. 171–183, ACM Press, New York, 1996.
- K. Birman and T. Joseph. 1987. "Exploiting virtual synchrony in distributed systems." In Proc. Eleventh ACM Symp. Operating Systems Principles (SOSP '87), Austin, Texas, United States, November 08–11, 1987, pp. 123–128, ACM Press, New York, 1987.
- B. Blanchet. 1998. "Escape analysis: Correctness proof, implementation and experimental results." In Proc. 25th ACM SIGPLAN-SIGACT Symp. Principles of Programming Languages, pp. 25–37, ACM Press, New York, 1998.
- B. Blanchet. 1999. "Escape analysis for object-oriented languages: Application to Java." In Proc. 14th ACM SIGPLAN Conf. Object-Oriented Programming, Systems, Languages, and Applications, pp. 20–34, ACM Press, New York, 1999.
- M. Blaum, J. Brady, J. Bruck, and J. Menon. 1995. "EVENODD: An optimal scheme for tolerating double disk failures in RAID architecture." *IEEE Trans. Computers*, 44(2), 192–201, 1995.
- L. Bloom, M. Cohen, and S. Porter. 1962. "Considerations in the design of a computer with high logic-to-memory speed ratio." In Gigacycle Computing Systems, Proc. Sessions on Gigacycle Computing Systems Presented at the AIEE Winter General Meeting, pp. 53–63. New York, January 1962.
- S. Blumson, P. Honeyman, T. E. Ragland, and M. T. Stolarchuk. 1993. AFS Server Logging, Tech. Rep. CITI-93-10, University of Michigan, November 1993.
- Bochs. 2006. The Bochs IA-32 Emulator Project. <http://bochs.sourceforge.net>.
- E. M. Boehm and T. B. Steel, Jr. 1959. "The Share 709 System: Machine implementation of symbolic programming." *J. ACM (JACM)*, 6(2), 134–140, April 1959.
- S. Borkar. 2004. "Circuit techniques for subthreshold leakage avoidance, control and tolerance." *IEDM* 2004.
- D. Bossen. 1970. "b-Adjacent error correction." *IBM J. Res. Dev.*, July 1970.
- N. Bowman et al. 1997. "Evaluation of existing architectures in IRAM systems." Workshop on Mixing Logic and DRAM, June 1997.
- D. Brash. 2002. The ARM architecture Version 6 (ARMv6). ARM Ltd., January 2002. White Paper.
- H. Bratman and I. V. Boldt, Jr. 1959. "The Share 709 System: Supervisory control." *J. ACM (JACM)*, 6(2), 152–155, April 1959.
- A. Braunstein, M. Riley, and J. Wilkes. 1989. "Improving the efficiency of UNIX file buffer caches." In Proc. Twelfth ACM Symp. Operating Systems Principles (SOSP), pp. 71–82, December 1989.
- B. S. Brawn, F. G. Gustavson, and E. S. Mankin, 1970. "Sorting in a paging environment." *Commun. ACM*, 13(8), 483–494, Aug. 1970.
- J. M. Bray, V. P. Nelson, P. A. D. de Maine, and J. D. Irwin. 1985. "Data-compression techniques ease storage problems." *Computer Design*, 1985.
- L. Breuer and D. Baum. 2006. *An Introduction to Queueing Theory and Matrix-Analytic Methods*. Springer, Berlin, 2006.
- E. Briggs, M. Cekleov, K. Creta, M. Khare, S. Kulick, A. Kumar, L. Looi, C. Natarajan, S. Radhakrishnan, and L. Rankin. 2002. "Intel 870: A building block for cost-effective, scalable servers." *IEEE Micro*, 22(2), Mar. 2002.
- R. A. Bringmann. 1995. "Compiler-Controlled Speculation." PhD thesis, University of Illinois, Urbana, IL, Department of Computer Science, 1995.

- D. Brooks and M. Martonosi. 1999. "Dynamically exploiting narrow width operands to improve processor power and performance." In Proc. 5th Int. Symp. High Performance Computer Architecture (HPCA), pp. 13–22, Orlando, FL, January 1999.
- D. M. Brooks, P. Bose, S. E. Schuster, H. Jacobson, P. N. Kudva, A. Buyuktosunoglu, J.-D. Wellman, V. Zyuban, M. Gupta, and P. W. Cook. 2000a. "Power-aware microarchitecture: Design and modeling challenges for next-generation microprocessors." *IEEE Micro*, 20(6), 26–44, November/December 2000.
- D. Brooks, V. Tiwari, and M. Martonosi. 2000b. "Wattch: A framework for architectural-level power analysis and optimizations." In Proc. 27th Annual International Symposium on Computer Architecture (ISCA'00), pp. 83–94, Vancouver BC, June 2000.
- D. Brooks and M. Martonosi. 2000. "Value-based clock gating and operation packing: Dynamic strategies for improving processor power and performance." *ACM Trans. Comput. Syst.*, 18(2), 89–126, 2000.
- W. R. Bryg, K. K. Chan, and N. S. Fiduccia. 1996. "A high-performance, low-cost multiprocessor bus for workstations and midrange servers." *The Hewlett-Packard J.*, 47(1), February 1996.
- D. Burger et al. 1996a. "Memory bandwidth limitations of future microprocessors." In Proc. Int. Symp. Computer Architecture (ISCA) 23, 78–89, May 1996.
- D. Burger, J. R. Goodman, and A. Kagi. 1996b. "Memory bandwidth limitations of future microprocessors." In Proc. 23rd Annual Int. Symp. Computer Architecture (ISCA'96), pp. 78–89, Philadelphia, PA, May 1996.
- D. Burger and T. M. Austin. 1997. The SimpleScalar Tool Set, version 2.0, Tech. Rep. CS-1342, University of Wisconsin-Madison, June 1997.
- W. P. Burleson et al. 1998. "Wave-pipelining: A tutorial and research survey," *IEEE Trans. VLSI Systems*, 6(5), Sept. 1998.
- M. Burrows, C. Jerian, B. Lampson, and T. Mann. 1992. "On-line data compression in a log-structured file system." In Proc. Fifth Int. Conf. Architectural Support For Programming Languages and Operating Systems (ASPLOS-V), pp. 2–9, Boston, Massachusetts, October 1992), R. L. Wexelblat, Ed., ACM Press, New York, 1992.
- J. A. Butts and G. S. Sohi. 2000. "A static power model for architects." In Proc. 33rd Ann. Int. Symp. Microarchitecture (MICRO-33), pp. 191–201, Monterey, CA, December 2000.
- B. Calder and D. Grunwald. 1995. "Next cache line and set prediction." In Proc. 22nd Ann. Int. Symp. Computer Architecture (ISCA '95), S. Margherita Ligure, Italy, June 22–24, 1995, pp. 287–296, ACM Press, New York, 1995.
- B. Calder, C. Krintz, S. John, and T. Austin. 1998. "Cache-conscious data placement." In Proc. Eighth Int. Conf. Architectural Support for Programming Languages and Operating Systems (ASPLOS'98), pp. 139–149, San Jose, CA, 1998.
- D. Callahan, K. Kennedy, and A. Porterfield. 1991. "Software prefetching." In Proc. 4th Int. Conf. Architectural Support for Programming Languages and Operating Systems (ASPLOS), pp. 40–52, April 1991.
- P. Cao, E. W. Felten, and K. Li. 1994a. "Application-controlled file caching policies." In Proc. USENIX Summer 1994 Technical Conf., pp. 171–182, Boston, MA, June 1994.
- P. Cao, E. W. Felten, and K. Li. 1994b. "Implementation and performance of application-controlled file caching." In Proc. 1st USENIX Symp. Operating Systems Design and Implementation (OSDI), pp. 165–178. Monterey, CA, November 1994.
- P. Cao, E. W. Felten, A. R. Karlin, and K. Li. 1995. "A study of integrated prefetching and caching strategies." In Proc. 1995 ACM SIGMETRICS Joint Int. Conf. Measurement and Modeling of Computer Systems SIGMETRICS '95/PERFORMANCE '95, (Ottawa, Ontario, Canada, May 15–19, 1995, B. D. Gaither, Ed., pp. 188–197, ACM Press, New York, 1995.
- P. Cao, E. W. Felten, A. R. Karlin, and K. Li. 1996. "Implementation and performance of integrated application-controlled file caching, prefetching, and disk scheduling." *ACM Trans. Comput. Syst.*, 14(4), 311–343, Nov. 1996.
- Y. Cao et al. 2000. "New paradigm of predictive MOSFET and interconnect modeling for early circuit design." Proc. of CICC, pp. 201–204, 2000.
- L. R. Carley, G. R. Ganger, and D. F. Nagle. 2000. "Mems-based integrated-circuit mass-storage systems." *Commun. the ACM*, 43(11), 73–80, 2000.
- M. C. Carlisle and A. Rogers. 1996. "Software caching and computation migration in Olden." *J. Parallel Distributed Computing*, 38(2), 248–255, 1996.
- R. W. Carr and J. L. Hennessy. 1981. "WSCLOCK—A simple and effective algorithm for virtual memory management." In Proc. Eighth ACM Symp. Operating

- Systems Principles (SOSP-8), pp. 87–95, Pacific Grove, CA, December 1981.
- S. Carr. 1993. “Memory-Hierarchy Management.” PhD thesis, Rice University, 1993.
- S. Carr, K. S. McKinley, and C. Tseng. 1994. “Compiler optimizations for improving data locality.” In Proc. Sixth Int. Conf. Architectural Support for Programming Languages and Operating Systems (ASPLOS’94), pp. 252–262, San Jose, CA, 1994.
- J. B. Carter, J. K. Bennett, and W. Zwaenepoel. 1991. “Implementation and performance of Munin.” In Proc. 13th ACM Symp. Operating Systems Principles (SOSP), pp. 152–164, October 1991.
- J. Carter, W. Hsieh, L. Stoller, M. Swanson, L. Zhang, E. Brunvand, A. Davis, C. Kuo, R. Kuramkote, M. Parker, L. Schaelicke, and T. Tateyama. 1999. “Impulse: Building a smarter memory controller.” In Proc. Fifth Int. Symp. High Performance Computer Architecture (HPCA’99), pp. 70–79, Orlando, FL, January 1999.
- B. Case. 1994a. “AMD unveils first superscalar 29K core.” *Microprocessor Rep.*, 8(14), 1994.
- B. Case. 1994b. “x86 has plenty of performance headroom.” *Microprocessor Rep.*, 8(11), 1994.
- F. Catthoor, S. Wuytack, E. De Greef, F. Franssen, L. Nachtergaele, and H. De Man. 1998. “System-level transformations for low power data transfer and storage.” In A. Chandrakasan and R. Brodersen, Eds., *Low Power CMOS Design*. IEEE Press, New York, pp. 609–618, 1998.
- K. K. Chan, C. C. Hay, J. R. Keller, G. P. Kurpanek, F. X. Schumacher, and J. Zheng. 1996. “Design of the HP PA7200 CPU.” *Hewlett-Packard J.*, 47(1), 25–33, February 1996.
- A. P. Chandrakasan and R. W. Brodersen. 1995. *Low Power Digital CMOS Design*. Kluwer Academic, Dordrecht/Norwell, MA, 1995.
- A. Chang and M. F. Mergen. 1988. “801 storage: Architecture and programming.” *ACM Trans. Computer Syst.*, 6(1), February 1988.
- P. P. Chang and W. W. Hwu. 1988. “Trace selection for compiling large C application programs to microcode.” In Proc. 21st Ann. Workshop on Microprogramming and Microarchitecture, San Diego, California, United States, November 28 to December 02, 1988, International. Symposium on Microarchitecture, pp. 21–29, IEEE Computer Society Press, Los Alamitos, CA, 1988.
- C. Chao, M. Mackey, and B. Sears. 1990. “Mach on a virtually addressed cache architecture.” In USENIX Mach Workshop, 1990.
- T. Chappell et al. 1991. “A 2-ns cycle, 3.8-ns access 512-kb CMOS ECL SRAM with a fully pipelined architecture.” *IEEE J. Solid-State Circuits*, 26, 1577–1585, Nov. 1991.
- H. R. Charney and D. L. Plato. 1968. “Efficient partitioning of components.” In Proc. 5th Ann. Workshop on Design Automation (DAC ’68), Washington, D. C., United States, July 15–18, 1968, ACM Press, New York, 16.1–16.21, 1968.
- M. J. Charney and A. P. Reeves. 1995. Generalized Correlation Based Hardware Prefetching, Technical Report EE-CEG-95-1, Cornell University, February 1995.
- M. Charney, P. Coteus, P. Emma, J. Rivers, and J. Rogers. 1999. Private communication.
- J. S. Chase, H. M. Levy, M. Baker-Harvey, and E. D. Lazowska. 1992a. How to Use a 64-bit Virtual Address Space, Technical Report 92-03-02, University of Washington, 1992.
- J. S. Chase, H. M. Levy, E. D. Lazowska, and M. Baker-Harvey. 1992b. Lightweight Shared Objects in a 64-bit Operating System, Technical Report 92-03-09, University of Washington, 1992.
- W. Y. Chen, S. A. Mahlke, P. P. Chang, and W. Mei W. Hwu. 1991. “Data access microarchitectures for superscalar processors with compiler-assisted data prefetching.” In Proc. 24th Int. Symp. Microarchitecture (MICRO), 1991.
- T. F. Chen and J. L. Baer. 1992. “Reducing memory latency via non-blocking and prefetching cache.” In the 5th Int. Conf. Architectural Support for Programming Languages and Operating Systems (ASPLOS), pp. 51–61, October 1992.
- J. B. Chen, A. Borg, and N. P. Jouppi. 1992. “A simulation based study of TLB performance.” In Proc. 19th Ann. Int. Symp. Computer Architecture (ISCA-19), 1992.
- W. Y.-W. Chen, Jr. 1993. “Data Preload for Superscalar and VLIW Processors.” PhD thesis, University of Illinois at Urbana-Champaign, Department of Electrical Engineering, August 1993.
- P. M. Chen, E. K. Lee, G. A. Gibson, R. H. Katz, and D. A. Patterson. 1994. “RAID: High-performance, reliable secondary storage.” *ACM Computing Surveys*, 26(2), 145–185, 1994.

- Z. Chen, M. Johnson, L. Wei, and K. Roy. 1998. "Estimation of standby leakage power in CMOS circuits considering accurate modeling of transistor stacks." In Proc. Int. Symp. Low Power Electronics and Design (ISLPED), 1998.
- B. M. Chen, T. H. Lee, K. Peng, and V. Venkataramanan. 2006. *Hard Disk Drive Servo Systems*. Springer, London, 2006.
- R. Cheng. 1987. "Virtual address cache in UNIX." In Proc. Summer 1987 USENIX Technical Conference, 1987.
- D. R. Cheriton, G. A. Slavenburg, and P. D. Boyle. 1986. "Software-controlled caches in the VMP multiprocessor." In Proc. 13th Ann. Int. Symp. Computer Architecture (ISCA-13), 1986.
- D. R. Cheriton, A. Gupta, P. D. Boyle, and H. A. Goosen. 1988. "The VMP multiprocessor: Initial experience, refinements and performance evaluation." In Proc. 15th Ann. Int. Symp. Computer Architecture (ISCA-15), 1988.
- D. R. Cheriton, H. A. Goosen, and P. D. Boyle. 1989. "Multi-level shared caching techniques for scalability in VMP-MC." In Proc. 16th Ann. Int. Symp. Computer Architecture (ISCA-16), 1989.
- B. S. Cherkauer and E. G. Friedman. 1995. "A unified design methodology for CMOS tapered buffers." *IEEE J. Solid-State Circuits*, 3, 99–111, Mar. 1995.
- T. M. Chilimbi, M. D. Hill, and J. R. Larus. 1999. "Cache-conscious structure layout." In Proc. ACM SIGPLAN '99 Conference on Programming Language Design and Implementation (PLDI), Atlanta, GA, ACM, May 1999.
- D. Chiou, P. Jain, L. Rudolph, and S. Devadas. 2000. "Application-specific memory management in embedded systems using software-controlled caches." In Proc. 37th Design Automation Conference (DAC), June 2000.
- Z. Chishti, M. Powell, and T. N. Vijaykumar. 2003. "Distance associativity for high-performance energy-efficient non-uniform cache architectures." In Proc. 36th Ann. Int. Symp. Microarchitecture (MICRO), pp. 55–66, San Diego, CA, December 2003.
- T. Chiueh and R. H. Katz. 1992. "Eliminating the address translation bottleneck for physical address caches." In Proc. Fifth Int. Conf. Architectural Support for Programming Languages and Operating Systems (ASPLOS-5), 1992.
- J.-D. Choi, M. Gupta, M. Serrano, V. C. Sreedhar, and S. Midkiff. 1999. "Escape analysis for java." In Proc. 14th ACM SIGPLAN Conf. Object-oriented Programming, Systems, Languages, and Applications (OOPSLA), pp. 1–19, ACM Press, New York, 1999.
- H.-T. Chou and D. J. DeWitt. 1985. "An evaluation of buffer management strategies for relational database systems." In Proc. 11th Int. Conf. Very Large Data Bases, Stockholm, Sweden, August 21–23, pp.127–141 1985.
- C. K. Chow. 1974. "On optimization of storage hierarchies." *IBM J. Res. Dev.*, 194–203, May 1974.
- C. K. Chow. 1976. "Determination of cache's capacity and its matching storage hierarchy." *IEEE Trans. Computers*, 25(2), 157–164, Feb. 1976.
- D. W. Clark and J. S. Emer. 1985. "Performance of the VAX-11/780 translation buffer: Simulation and measurement." *ACM Trans. Computer Systems*, 3(1), 1985.
- E. G. Coffman and P. J. Denning. 1973. *Operating System Theory*. Prentice Hall, Englewood Cliffs, NJ, 1973.
- D. Colarelli, D. Grunwald, and M. Neufeld. 2002. "The case for massive arrays of idle disks." In Proc. 2002 FAST, Monterey, CA, 2002.
- C. Collins, E. Fiterman, T. Zhang, and B. Jacob. 2000. SimBed: Accurate Microarchitecture-level Simulation of Embedded Real-Time Operating Systems, Tech. Rep. UMD-SCA-2000-1, University of Maryland Systems & Computer Architecture Group, April 2000.
- C. M. Collins. 2000. "An evaluation of embedded system behavior using full-system software emulation." Master's thesis, University of Maryland at College Park, May 2000.
- J. Collins, S. Sair, B. Calder, and D. Tullsen. 2002. "Pointer cache assisted prefetching." In Proc. 35th Ann. IEEE/ACM Int. Symp. Microarchitecture (MICRO), November 2002.
- R. Colwell, R. Nix, J. O'Donnell, D. Papworth, and P. Rodman. 1987. "A VLIW architecture for a trace scheduling compiler." In Proc. Second Int. Conf. Architectural Support for Programming Languages and Operating Systems (ASPLOS-2), pp. 180–192, 1987.
- L. W. Comeau. 1967. "A study of the effect of user program optimization in a paging system." In Proc. First ACM

- Symp. Operating System Principles (SOSP '67), J. Gosden and B. Randell, Eds., pp. 4.1–4.7, ACM Press, New York, 1967.
- Compaq. New Challenges Drive Compaq Advanced Memory Protection Strategy, Compaq Computer Corporation, Whitepaper.
- J. P. Considine and J. J. Myers. 1969. "Establishment and maintenance of a storage hierarchy for an on-line data base under TSS/360." In Proc. Fall Joint Computer Conference, pp. 433–440, November 1969.
- J. P. Considine and J. J. Myers. 1977. "MARC: MVS archival storage and recovery program." *IBM Systems J.*, 16(4), 378–397, 1977.
- T. M. Conte, K. N. Menezes, P. M. Mills, and B. A. Patel. 1995. "Optimization of instruction fetch mechanisms for high issue rates." In Proc. 22nd Ann. Int. Symp. Computer Architecture (ISCA), pp. 333–344. Santa Margherita Ligure, Italy, June 1995.
- R. Cooksey, S. Jourdan, and D. Grunwald. 2002. "A stateless, content-directed data prefetching mechanism." In Proc. Int. Conf. Architectural Support for Programming Languages and Operating System (ASPLOS), 2002.
- K. D. Cooper and T. J. Harvey. 1998. "Compiler-controlled memory." In Architectural Support for Programming Languages and Operating Systems (ASPLOS), pp. 2–11, San Jose, CA, Oct. 1998.
- F. J. Corbato. 1968. A Paging Experiment with the Multics System, MIT Project -MAC Report MAC-M-384, May 1968.
- G. V. Cormack. 1985. "Data compression on a database system." *Commun. ACM*, 28(12), 1336–1342, Dec. 1985.
- D. W. Cornell and P. S. Yu. 1989. "Integration of buffer management and query optimization in relational database environment." In Proc. Fifteenth Int. Conf. Very Large Data Bases, August 22–25, Amsterdam, The Netherlands, pp. 247–255, 1989.
- S. L. Coumeri and D. E. Thomas. 1998. "Memory modeling for system synthesis." In Proc. 1998 Int. Symp. Low Power Electronics and Design (ISLPED '98), Monterey, California, United States, August 10–12, 1998, ACM Press, New York, pp. 179–184, 1998.
- R. Crisp. 1997. "Direct Rambus technology: The new main memory standard." *IEEE Micro*, 17(6), 18–28, Nov. 1997.
- V. Cuppu and B. Jacob. 1999a. The Performance of Next-Generation DRAM Architectures, Tech. Rep. UMD-SCA-TR-1999-1, University of Maryland Systems and Computer Architecture Group, March 1999.
- V. Cuppu and B. Jacob. 1999b. Organizational Design Trade-offs at the DRAM, Memory Bus, and Memory Controller Level: Initial Results, Tech. Rep. UMD-SCA-1999-2, University of Maryland Systems & Computer Architecture Group, November 1999.
- V. Cuppu, B. Jacob, B. Davis, and T. Mudge. 1999. "A performance comparison of contemporary DRAM architectures." In Proc. 26th Ann. Int. Symp. Computer Architecture (ISCA'99), pp. 222–233. Atlanta, GA, May 1999.
- V. Cuppu and B. Jacob. 2001. "Concurrency, latency, or system overhead: Which has the largest impact on uniprocessor dram-system performance?" In Proc. 28th Ann. Int. Symp. Computer Architecture (ISCA'01), pp. 62–71, Göteborg, Sweden, June 2001.
- V. Cuppu, B. Jacob, B. Davis, and T. Mudge. 2001. "High performance DRAMs in workstation environments." *IEEE Trans. Computers*, 50(11), 1133–1153, Nov. 2001. (Special issue on High-Performance Memory Systems)
- H. Custer. 1993. Inside Windows/NT, Technical report, Microsoft Press.
- Z. Cvetanovic and D. Bhandarkar. 1994. "Characterization of Alpha AXP performance using TP and SPEC workloads." Int. Symp. Computer Architecture (ISCA-21), pp. 60–70, April 1994.
- Z. Cvetanovic and R. E. Kessler. 2000. "Performance analysis of the Alpha 21264-based Compaq ES40 system." In Proc. 27th Ann. Int. Symp. Computer Architecture (ISCA'00), pp. 192–202, Vancouver, BC, June 2000.
- W. Dally and J. Poulton. 1998. *Digital Systems Engineering*. Cambridge University Press, Cambridge, UK, 1998.
- R. Das, M. Uysal, J. Saltz, and Y.-S. Hwang. 1994. "Communication optimizations for irregular scientific computations on distributed memory architectures." *J. Parallel Distributed Computing*, 22(3), 462–479, Sept. 1994.
- M. Das. 2000. "Unification-based pointer analysis with directional assignments." In Proc. SIGPLAN '00 Conf. Program Language Design and Implementation (PLDI), pp. 35–46, Vancouver, BC, June 2000.
- B. Davis, T. Mudge, and B. Jacob. 2000a. The New DRAM Interfaces: SDRAM, RDRAM and Variants. In M. Valero,

- K. Joe, M. Kitsuregawa, and H. Tanaka, Editors, *High Performance Computing, Lecture Notes in Computer Science*, Vol. 1940, pp. 26–31, Springer Publishing, Tokyo, Japan, 2000.
- B. Davis, T. Mudge, V. Cuppu, and B. Jacob. 2000b. “DDR2 and low-latency variants.” In Proc. Workshop on Solving the Memory Wall Problem, Held in conjunction with ISCA-27, pp. 15–29, Vancouver, BC, June 2000.
- P. A. D. de Maine and B. A. Marron. 1966. “The SOLID System I: A method for organizing and searching files.” In G. Schechter, Editor, *Information Retrieval—A Critical View* (Based on the Third Annual National Colloquium on Information Retrieval, Philadelphia PA, May 1966), Thompson Book Co., Washington, DC, pp. 243–282, 1967.
- H. Deitel. 1990. *Inside OS/2*. Addison-Wesley, Reading, MA.
- V. Delaluz, M. Kandemir, N. Vijaykrishnan, A. Sivasubramaniam, and M. Irwin. 2001. “Hardware and software techniques for controlling DRAM power modes.” In Seventh Int. Symp. High-Performance Computer Architecture (HPCA’01), January 2001.
- T. Dell. 1997. A White Paper on the Benefits of Chipkill-Correct ECC for PC Server Main Memory. IBM Microelectronics Division, November 1997. White Paper.
- P. J. Denning. 1967. “The working set model for program behavior.” In Proc. First ACM Symp. Operating System Principles (SOSP 1), pp. 15.1–15.12, 1967.
- P. J. Denning. 1968. “The working set model for program behavior.” *Commun. ACM*, 11(5), 323–333, 1968.
- P. J. Denning. 1970. “Virtual memory.” *Computing Surveys*, 2(3), 153–189, 1970.
- P. J. Denning. 1972. “On modeling program behavior.” In Proc. AFIPS Spring Joint Computer Conference, pp. 937–944, 1972.
- P. J. Denning. 1980. “Working sets past and present.” *IEEE Trans. Software Eng.*, 6(1), 64–84, 1980.
- J. B. Dennis. 1965. “Segmentation and the design of multiprogrammed computer systems.” *J. ACM*, 12(4), 589–602, Oct. 1965.
- Design & Test Roundtable. 1997. “Hardware-software codesign.” *IEEE Design Test Computers*, 14(1), 75–83, January–March 1997.
- R. P. Dick, G. Lakshminarayana, A. Raghunathan, and N. K. Jha. 2000. “Power analysis of embedded operating systems.” In 37th Design Automation Conference (DAC), Los Angeles CA, pp. 312–315, June 2000.
- Digital. 1994. DECchip 21064 and DECchip 21064A Alpha AXP Microprocessors Hardware Reference Manual. Digital Equipment Corporation, Maynard, MA.
- Digital. 1996. Digital Semiconductor 21164 (366 MHz Through 433 MHz) Alpha Microprocessor Hardware Reference Manual. Digital Equipment Corporation, Maynard, MA.
- Digital. 1997. DIGITAL FX!32. Digital Equipment Corp., <http://www.digital.com/info/semiconductor/amt/fx32/fx.html>.
- V. J. DiGri and J. King. 1959. “The Share 709 System: Input-output translation.” *J. ACM (JACM)*, 6(2), 141–144, April 1959.
- C. Ding and K. Kennedy. 1999. “Improving cache performance in dynamic applications through data and computation reorganization at run time.” In Proc. ACM SIGPLAN 1999 Conf. on Programming Language Design and Implementation (PLDI 1999), pp. 229–241, Atlanta, GA, May 1999.
- B. Dipert. 2000. “The slammin, jammin, DRAM scramble.” *EDN*, 2000(2), 68–82, Jan. 2000.
- A. Dominguez, S. Udayakumaran, and R. Barua. 2005. “Heap data allocation to scratch-pad memory in embedded systems.” *J. Embedded Computing (JEC)*, 1(4), 2005. IOS Press, Amsterdam, Netherlands.
- F. Douglass. 1993. “The compression cache: Using on-line compression to extend physical memory.” In Proc. Usenix Winter 1993 Technical Conference, pp. 519–529, San Diego, CA, January 1993.
- B. Doyle et al. 2002. “Transistor elements for 30 nm physical gate lengths and beyond.” *Intel Technol. J.* 6, 42–54, May 2002.
- A. L. Drapeau and R. H. Katz. 1993. “Striped tape arrays.” In Proc. 1993 IEEE Symp. on Mass Storage Systems, pp. 1993. 257–265.
- P. Druschel and L. L. Peterson. 1993. “Fbufs: A high-bandwidth cross-domain transfer facility.” In Proc. Fourteenth ACM Symp. on Operating Systems Principles (SOSP-14), pp. 189–202, December 1993.
- R. Duncan, C. Petzold, A. Schulman, M. S. Baker, R. P. Nelson, S. R. Davis, and R. Moote. 1994. *Extending*

- DOS—A Programmer's Guide to Protected-Mode DOS, 2nd Edition.* Addison-Wesley, Reading, MA, 1994.
- J. DuPreez. 2002. Personal communication.
- C. P. Earnest, K. G. Balke, and J. Anderson. 1972. "Analysis of graphs by ordering of nodes." *J. ACM*, 19(1), 23–42, Jan. 1972.
- K. Ebcioglu. 1987. "A compilation technique for software pipelining of loops with conditional jumps." In Proc. 20th Ann. Workshop on Microprogramming (MICRO-20), pp. 69–79, Colorado Springs, CO, December 1987.
- K. Ebcioglu. 1988. "Some design ideas for a VLIW architecture for sequential natured software." In *Parallel Processing* (Proc. IFIP WG 10.3, Working Conference on Parallel Processing), M. Cosnard, M. Barton, and M. Vanneschi, Eds., pp. 3–21, 1988.
- K. Ebcioglu and E. R. Altman. 1997. "DAISY: Dynamic compilation for 100% architectural compatibility." In Proc. 24th Ann. Int. Symp. on Computer Architecture (ISCA-24), pp. 26–37, Denver, CO, 1997.
- C. H. Edwards, Jr. and D. E. Penney. 1982. *Calculus and Analytic Geometry*. Prentice Hall, Englewood Cliffs, NJ, 1982.
- J. R. Ellis. 1985. *Bulldog: A Compiler for VLIW Architectures*. The MIT Press, Cambridge, MA. 1985. (Ellis's Ph.D. Thesis, Yale, 1984).
- C. Ellis. 1999. "The case for higher-level power management." In Workshop on Hot Topics in Operating Systems, 1999.
- Y. Endo, Z. Wang, J. B. Chen, and M. Seltzer. 1996. "Using latency to evaluate interactive system performance." In Proc. 1996 Symp. on Operating System Design and Implementation (OSDI-2), October 1996.
- D. Engler, R. Dean, A. Forin, and R. Rashid. 1994. "The operating system as a secure programmable machine." In Proc. 1994 European SIGOPS Workshop, 1994.
- ESDRAM. 1998. Enhanced SDRAM 1M x 16. Enhanced Memory Systems, Inc., http://www.edram.com/products/datasheets/16M_esdram0298a.pdf.
- Etch. 1998. Memory System Research at the University of Washington. The University of Washington, <http://etch.cs.washington.edu/>.
- A. Eto et al. 1998. "Impact of Neutron Flux on Soft Error in MOS Memories" In. Proc. Int'l. Electron Devices Meeting (IEDM), pp. 367–370. Dec. 1998.
- A. Eustace and A. Srivastava. 1994. ATOM: A Flexible Interface for Building High Performance Program Analysis Tools, Technical Report WRL-TN-44, DEC Western Research Laboratory.
- K. Farkas, P. Chow, N. Jouppi, and Z. Vranesic. 1997. "Memory-system design considerations for dynamically-scheduled processors." In Proc. 24th Ann. Int. Symp. on Computer Architecture (ISCA), 1997.
- A. H. Farrahi, G. E. Téllez, and M. Sarrafzadeh. 1995. "Memory segmentation to exploit sleep mode operation." In Proc. 32nd ACM/IEEE Conf. on Design Automation (DAC '95), pp. 36–41, San Francisco, California, United States, June 12–16, 1995, ACM Press, New York, 1995.
- R. R. Fenichel, and J. C. Yochelson. 1969. "A LISP garbage-collector for virtual-memory computer systems." *Commun. ACM*, 12(11), 611–612, Nov. 1969.
- D. Ferrari. 1973. "A tool for automatic program restructuring." In Proc. Ann. Conf. (ACM '73), Atlanta, Georgia, United States, August 27–29, 1973), pp. 228–231, ACM Press, New York, 1973.
- D. Ferrari. 1974. "Improving locality by critical working sets." *Commun. ACM*, 17(11), 614–620, Nov. 1974.
- D. Ferrari. 1976. "The improvement of program behavior." *IEEE Computer*, 9(11), Nov. 1976.
- J. A. Fisher. 1980. "2n-way jump microinstruction hardware and an effective instruction binding method." In Proc. 13th Ann. Workshop on Microprogramming (MICRO-13), pp. 64–75, November 1980.
- J. Fisher. 1981. "Trace scheduling: A technique for global micro-code compaction." *IEEE Trans. Computers*, 30(7), 478–490, July 1981.
- J. A. Fisher. 1983. "Very long instruction word architectures and the ELI-512." In Proc. 10th Ann. Int. Symp. on Computer Architecture (ISCA-10), pp. 140–150, June 1983.
- J. A. Fisher, J. R. Ellis, J. C. Ruttenberg, and A. Nicolau. 1984. "Parallel processing: A smart compiler and a dumb machine." In Proc. ACM SIGPLAN '84 Symp. on Compiler Construction, SIGPLAN Notices, 19(6), 37–47, June 1984.
- K. Flautner, S. Reinhardt, and T. Mudge. 2001. "Automatic performance-setting for dynamic voltage scaling." In 7th Conf. on Mobile Computing and Networking (MOBICOM'01), Rome, Italy, July 2001.

- J. Flinn and M. Satyanarayanan. 1999. "Powerscope: A tool for profiling the energy usage of mobile applications." In *Workshop on Mobile Computing Systems and Applications*, pp. 2–10, February 1999.
- J. Fotheringham. 1961. "Dynamic storage allocation in the Atlas computer, including an automatic use of a backing store." *Commun. ACM*, 4(10), 435–436, Oct. 1961.
- M. Franklin and M. Smotherman. 1994. "A fill-unit approach to multiple instruction issue." In *Proc. 27th Ann. Int. Symp. on Microarchitecture (MICRO-27)*, pp. 162–171, San Jose, CA, November 1994.
- R. Fromm, S. Perissakis, N. Cardwell, C. Kozyrakis, B. McGaughy, D. Patterson, T. Anderson, and K. Yelick. 1997. "The energy efficiency of IRAM architectures." In *Proc. 24th Ann. Int. Symp. on Computer Architecture (ISCA'97)*, pp. 327–337, Denver, CO, June 1997.
- J. W. Fu and J. H. Patel. 1991. "Data prefetching in multiprocessor vector cache memories." In *Proc. 18th Ann. Int. Symp. on Computer Architecture (ISCA 1991)*, pp. 54–63, Toronto, Ontario, May 1991.
- D. M. Gallagher, W. Y. Chen, S. A. Mahlke, J. C. Gyllenhaal, and W. mei W. Hwu. 1994. "Dynamic memory disambiguation using the memory conflict buffer." In *Proc. Sixth Int. Conf. on Architectural Support for Programming Languages and Operating Systems (ASPLOS-6)*, San Jose, CA, 1994.
- B. Ganesh, A. Jaleel, D. Wang, and B. Jacob. 2007. "Fully-Buffered DIMM memory architectures: Understanding mechanisms, overheads and scaling." In *Proc. 13th Int. Symp. on High Performance Computer Architecture (HPCA 2007)*, Phoenix, AZ, February 2007.
- G. Ganger, B. Worthington, and Y. Patt. 2006. *The DiskSim Simulation Environment Version 2.0 Reference Manual*, <http://www.pdl.cmu.edu/DiskSim/>. 2006.
- J. G. Ganssle. 1994. "An OS in a can." *Embedded Systems Programming*, January 1994.
- J. G. Ganssle. 1997. "The challenges of real-time programming." *Embedded Systems Programming*, 11(7), 20–26, July 1997.
- J. Ganssle. 2000a. "Conspiracy theory." *The Embedded Muse Newsl.*, no. 46, March 3, 2000.
- J. Ganssle. 2000b. "Conspiracy theory, take 2." *The Embedded Muse Newsl.*, No. 47, March 22, 2000.
- H. Garcia-Molina, A. Park, and L. R. Rogers. 1987. "Performance through memory." In *Proc. 1987 ACM Sigmetrics Conference. on Measurement and Modeling of Computer Systems*, pp. 122–131, 1987.
- W. E. Garrett, R. Bianchini, L. Kontothanassis, R. A. McCallum, J. Thomas, R. Wisniewski, and M. L. Scott. 1992. *Dynamic Sharing and Backward Compatibility on 64-bit Machines*, Technical Report TR 418, University of Rochester.
- W. E. Garrett, M. L. Scott, R. Bianchini, L. I. Kontothanassis, R. A. McCallum, J. A. Thomas, R. Wisniewski, and S. Luk. 1993. "Linking shared segments." In *USENIX Technical Conference Proceedings*, pp. 13–27, January 1993.
- J.-L. Gassée. 1996. "CoffeeBean." *Be Newsletter*, Issue 52, December 4, 1996.
- R. Geist and S. Daniel. 1987. "A continuum of disk scheduling algorithms." *ACM Trans. Comput. Syst.*, 5(1), 77–92, 1987.
- P. Gelsinger. 2001. "Microprocessors for the new millennium: Challenges, opportunities, and new frontiers." *ISSCC*, 22–5, 2001.
- L. Geppert. 2004. "A Static RAM says goodbye to data errors." *IEEE Spectrum*, February 2004.
- K. Gharachorloo, D. Lenosk, J. Laudon, P. Gibbons, A. Gupta, and J. Hennessy. 1990. "Memory consistency and event ordering in scalable shared-memory multiprocessors." In *Proc. 17th Ann. Int. Symp. on Computer Architecture (ISCA)*, pp. 15–26, May 1990.
- N. Gloy, T. Blackwell, M. D. Smith, and B. Calder. 1997. "Procedure placement using temporal ordering information." In *Proc. 30th Ann. IEEE/ACM Int. Symp. on Microarchitecture (MICRO)*, pp. 303–313, December 1997.
- R. Gonzalez and M. Horowitz. 1996. "Energy dissipation in general purpose microprocessors." *IEEE J. Solid-State Circuits*, 31(9), 1277–1284, Sept. 1996.
- J. R. Goodman. 1987. "Coherency for multiprocessor virtual address caches." In *Proc. Second Int. Conf. on Architectural Support for Programming Languages and Operating Systems (ASPLOS-2)*, pp. 72–81, 1987.
- B. Goodman. 2002. Personal communication.
- K. Govil, E. Chan, and H. Wasserman. 1995. "Comparing algorithms for dynamic speed-setting of a

- low-power CPU." In Proc. First ACM Int. Conf. on Mobile Computing and Networking, Berkeley, CA, November 1995.
- M. K. Gowan, L. L. Biro, and D. B. Jackson. 1998. "Power considerations in the design of the Alpha 21264 microprocessor." In 35th Design Automation Conference (DAC). 1998.
- I. D. Greenwald and M. Kane. 1959. "The Share 709 System: Programming and modification." *J. ACM (JACM)*, 6(2), 128–133, April 1959.
- J. Griffioen and R. Appleton. 1994. "Reducing file system latency using a predictive approach." In Proc. 1994 Summer USENIX Conf., pp. 197–207, Boston, MA, June 1994.
- P. Gronowski et al. 1996. "A 433-MHz 64-b quad-issue RISC microprocessor." *JSSC*, 31(11), 1687–1696, Nov. 1996.
- A. Grove. 2002. "Changing Vectors of Moore's Law." Presented at International. Electron Devices Meeting (IEDM), December 2002.
- D. Grunwald, B. Zorn, and R. Henderson. 1993. "Improving the cache locality of memory allocation." In R. Cartwright, Ed., Proc. ACM SIGPLAN 1993 Conf. on Programming Language Design and Implementation (PLDI '93), pp. 177–186, Albuquerque, New Mexico, United States, June 21–25, 1993, ACM Press, New York, 1993.
- D. Grunwald, P. Levis, C. B. M. III, M. Neufeld, and K. I. Farkas. 2000. "Policies for dynamic clock scheduling." In Proc. Fourth USENIX Symp. on Operating Systems Design and Implementation (OSDI 2000), pp. 73–86, San Diego, CA, October 2000.
- S. Gurumurthi, A. Sivasubramaniam, M. Kandemir, and H. Franke. 2003. "DRPM: Dynamic speed-control for power management in server class disks." In Proc. 30th Int. Symp. on Computer Architecture (ISCA 2003), pp. 169–179, June 2003.
- L. Gwennap. 1994a. "MIPS R10000 uses decoupled architecture." *Microprocessor Rep.*, 8(14), 1994.
- L. Gwennap. 1994b. "PA-8000 combines complexity and speed." *Microprocessor Rep.*, 8(15), 1994.
- L. Gwennap. 1995a. "Intel's P6 uses decoupled superscalar design." *Microprocessor Rep.*, 9(2), 1995.
- L. Gwennap. 1995b. "PA-8000 stays on track (sidebar in Integrated PA-7300LC powers HP midrange)." *Microprocessor Rep.*, 9(15), 1995.
- L. Gwennap. 1995c. "Intel's P6 uses decoupled superscalar design." *Microprocessor Rep.*, 9(2), Feb. 1995.
- L. Gwennap. 1996. "Digital 21264 sets new standard." *Microprocessor Rep.*, 10(14), October 1996.
- L. Gwennap. 1998a. "Alpha 21364 to ease memory bottleneck." *Microprocessor Rep.*, 12(14), 12–15, Oct. 1998.
- L. Gwennap. 1998b. "New processor paradigm: V-IRAM." *Microprocessor Rep.*, 12(3), 17–19, March 1998.
- J. Haas and P. Vogt. 2005. "Fully-buffered DIMM technology moves enterprise platforms to the next level." *Technology@Intel Magazine*, March 2005.
- E. Hagersten, A. Landin, and S. Haridi. 1992. "DDM—A cacheonly memory architecture." *IEEE Computer*, 25(9), 44–54, Sept. 1992.
- S. Hall, G. Hall, and J. McCall. 2000. *High-Speed Digital System Design—A handbook of Interconnect Theory and Design Practices*, Wiley-Interscience, New York, 2000.
- N. Hallenberg, M. Elsman, and M. Toft. 2002. "Combining region inference and garbage collection." In Proc. ACM SIGPLAN 2002 Conf. on Programming Language Design and Implementation (PLDI) pp. 141–152, ACM Press, New York, 2002.
- G. Hallnor and S. K. Reinhardt. 2000. "A fully associative software-managed cache design." In Proc. 27th Int. Symp. on Computer Architecture (ISCA), Vancouver, BC, Canada, June 2000.
- J. P. Halter and F. Najm. 1997. "A gate-level leakage power reduction method for ultra-low-power CMOS circuits." In Proc. IEEE Custom Integrated Circuits Conf., 1997.
- G. Hamilton and P. Kougiouris. 1993. "The Spring nucleus: A microkernel for objects." In USENIX Technical Conference Proceedings, 1993.
- F. Hamzaoglu and M. R. Stan. 2002. "Circuit-level techniques to control gate-leakage for sub-100nm CMOS." *ISLPED*, August 2002.
- R. Hank, S. Mahlke, R. Bringmann, J. Gyllenhaal, and W. Hwu. 1993. "Superblock formation using static program analysis." In 26th Int. Symp. on Microarchitecture (MICRO), pp. 247–256, IEEE Press, New York, December 1993.
- W. J. Hansen. 1969. "Compact list representation: Definition, garbage collection, and system

- implementation." *Commun. ACM*, 12(9), 499–507, Sep. 1969.
- J. M. Harker, D. W. Brede, R. E. Pattison, G. R. Santana, and L. G. Taft. 1981. "A quarter century of disk file innovation." *IBM J. Res. Dev.*, 25(5), 677–689, 1981.
- S.J. Hartley. 1988. "Compile-time program restructuring in multiprogrammed virtual memory systems." *IEEE Trans. Software Eng.*, 14 (11), 1640–1644, Nov. 1988.
- D.J. Hatfield and J. Gerald. 1971. "Program restructuring for virtual memory." *IBM Systems J.* 10(3), 168–192, 1971.
- S. Haykin. 2002. *Adaptive Filter Theory, 4th Ed.*, Prentice Hall, Upper Saddle River, NJ.
- R. Heald and J. Hoist. 1993. "A 6-ns cycle 256-kb cache memory and memory management unit." *IEEE J. Solid-State Circuits*, 28, 1078–1083, Nov. 1993.
- J. Heinrich, editor. 1995. MIPS R10000 Microprocessor User's Manual, version 1.0. MIPS Technologies, Inc., Mountain View, CA.
- J. Hennessy and M. Heinrich. 1996. "Hardware/software codesign of processors: Concepts and examples." In G. De Micheli and M. Sami, Eds., *Hardware/Software Co-Design*, Kluwer Academic, San Mateo, CA, pp. 29–44, 1996.
- J. L. Hennessy and D. A. Patterson. 1990. *Computer Architecture: A Quantitative Approach*. Morgan Kaufmann, San Mateo, CA, 1990.
- J. L. Hennessy and D. A. Patterson. 1996. *Computer Architecture: A Quantitative Approach, 2nd Ed.*, Morgan Kaufmann, San Mateo, CA, 1996.
- J. L. Hennessy and D. A. Patterson. 2003. *Computer Architecture: A Quantitative Approach, 3rd Ed.*, Morgan Kaufmann, San Mateo, CA, 2003.
- D. S. Henry. 1994. Adding Fast Interrupts to Superscalar Processors, Tech. Rep. Memo-366, MIT Computation Structures Group, December 1994.
- D. Henry, B. Kuszmaul, G. Loh, and R. Sami. 2000. "Circuits for wide-window superscalar processors." In Proc. 27th Ann. Int. Symp. on Computer Architecture (ISCA'00), pp. 236–247, Vancouver, BC, June 2000.
- Hewlett-Packard. 1990. PA-RISC 1.1 Architecture and Instruction Set Reference Manual. Hewlett-Packard Company.
- M. D. Hill, S. J. Eggers, J. R. Larus, G. S. Taylor, G. Adams, B. K. Bose, G. A. Gibson, P. M. Hansen, J. Keller, S. I. Kong, C. G. Lee, D. Lee, J. M. Pendleton, S. A. Ritchie, D. A. Wood, B. G. Zorn, P. N. Hilfinger, D. Hodges, R. H. Katz, J. K. Ousterhout, and D. A. Patterson. 1986. "Design decisions in SPUR." *IEEE Computer*, 19(11), Nov. 1986.
- G. Hinton, D. Sager, M. Upton, D. Boggs, D. Carmeanand, A. Kyker, and P. Roussel. 2001. "The microarchitecture of the Pentium 4 Processor." *Intel Technol. J.*, First Quarter, 2001.
- T. Hirose et al. 1990. "A 20-ns 4-Mb CMOS SRAM with hierarchical word decoding architecture." *IEEE J. Solid-State Circuits*, SC-25(5), 1068–1074, Oct. 1990.
- J. D. Hiser and J. W. Davidson. 2004. "Embarc: an efficient memory bank assignment algorithm for retargetable compilers." In Proc. 2004 ACM SIGPLAN/SIGBED Conf. on Languages, Compilers, and Tools for Embedded Systems (LCTES), pp. 182–191, ACM Press, New York, 2004.
- Hitachi/Renesas. 1999. SH7050 32-bit CPU. Hitachi/Renesas, Revised Sep. 1999. <http://documentation.renesas.com/eng/products/mpumcu/e602121sh7050.pdf>.
- Hitachi/Renesas. 2004. M32R-32192 32-bit Embedded CPU. Revised July 2004. <http://documentation.renesas.com/eng/products/mpumcu/rej03b001932192ds.pdf>.
- A. S. Hoagland. 2003. "History of magnetic disk storage based on perpendicular magnetic recording." *IEEE Trans. Magnetics*, 39(4), 1871–1875, 2003.
- H. Hohnson and M. Graham. 1993. *High-Speed Digital Design—A Handbook of Black Magic*, Prentice Hall PTR, Upper Saddle River, NJ, 1993.
- N. Honda, K. Ouchi, and S. Iwasaki. 2002. "Design consideration of ultrahigh-density perpendicular magnetic recording media." *IEEE Trans. Magnetics*, 38(4), 1615–1621, 2002.
- S. I. Hong, S. A. McKee, M. H. Salinas, R. H. Klenke, J. H. Aylor, and W. A. Wulf. 1999. "Access order and effective bandwidth for streams on a Direct Rambus memory." In Proc. Fifth Int. Symp. on High Performance Computer Architecture (HPCA'99), pp. 80–89, Orlando, FL, January 1999.
- M. Horowitz, T. Indermaur, and R. Gonzalez. 1994. "Low-power digital design." In IEEE Symp. on Low Power Electronics, pp. 8–11, October 1994.
- M. Horowitz, M. Martonosi, T. C. Mowry, and M. D. Smith. 1995. Informing Loads: Enabling Software to Observe

- and React to Memory Behavior, Technical Report CSL-TR-95-673, Stanford University, Stanford, CA.
- T. R. Hotchkiss, N. D. Marschke, and R. M. McColsky. 1996. "A new memory system design for commercial and technical computing products." *The Hewlett-Packard J.*, 47 (1), Feb. 1996.
- H. Hsiao and D. DeWitt. 1993. "A performance study of three high availability data storage strategies." *J. Distributed Parallel Databases*, 1(1), 53–80, 1993.
- W. W. Hsu and A. J. Smith. 2004. "The real effect of i/o optimizations and disk improvements." *IBM J. Res. Dev.*, 48(2), 255–289, 2004.
- W. W. Hsu, H. C. Young, and A. J. Smith. 2005. "The automatic improvement of locality in storage systems." *ACM Trans. Computers*, 23(4), 424–473, 2005.
- Z. Hu, S. Kaxiras, and M. Martonosi. 2002. "Timekeeping in the memorysystem: Predicting and optimizing memory behavior." In 29th Int. Symp. on Computer Architecture (ISCA), May 2002.
- Z. Hu, M. Martonosi, and S. Kaxiras. 2003. "Tag correlating prefetchers." In 9th Int. Symp. on High-Performance Computer Architecture (HPCA), February 2003.
- A. S. Huang, G. Slavenberg, and J. P. Shen. 1994. "Speculative disambiguation: A compilation technique for dynamic memory disambiguation." In Proc. 21st Ann. Int. Symp. on Computer Architecture (ISCA-21), Chicago, IL, 1994.
- F. Y. Huang, M. T. White, and T. Semba. 2002. "Single vs dual stage actuator—why and when." In Proc. ASME/STLE Int. Joint Tribology Conference, pp. 27–30, Cancun, Mexico, 2002.
- J. Huck and J. Hays. 1993. "Architectural support for translation table management in large address space machines." In Proc. 20th Ann. Int. Symp. on Computer Architecture (ISCA'93), pp. 39–50, May 1993.
- J. Huck. 1996. Personal communication.
- C. J. Hughes. 2000. "Prefetching linked data structures in systems with merged DRAM-logic." Master's thesis, University of Illinois at Urbana-Champaign, May 2000. Technical Report UIUCDCS-R-2001-2221.
- G. F. Hughes. 2002. "Patterned media recording systems—The potential and the problems." In Magnetics Conference, 2002. INTERMAG Europe 2002. Digest of Technical Papers, page GA6, Amsterdam, The Netherlands.
- J. Huh and T. Chang. 2003. "Hierarchical disk cache management in RAID 5 controller." *J. Computing Sciences in Colleges Archive*, 19(2), 47–59, Dec. 2003.
- A. Hume. 1988. "The File Motel—An incremental backup system for Unix." In Proc. Summer 1988 USENIX Conference, pp. 61–72, June 1988.
- C. Huneycutt and K. Mackenzie. 2002. "Software caching using dynamic binary rewriting for embedded devices." In Proc. Int. Conf. on Parallel Processing, pp. 621–630, 2002.
- I. Hur and C. Lin. 2004. "Adaptive history-based memory schedulers." In Proc. 37th Int. Symp. on Microarchitecture (MICRO), December 2004.
- J. Huynh. 2003. The AMD Athlon MP Processor with 512KB L2 Cache: Technology and Performance Leadership for x86 Microprocessors. AMD White Paper, May 2003.
- W. W. Hwu and P. P. Chang. 1989. "Achieving high instruction cache performance with an optimizing compiler." In Proc. 16th Ann. Int. Symp. on Computer Architecture (ISCA), pp. 242–251, Jerusalem, Israel, April 1989.
- W.-M. Hwu and Y. N. Patt. 1986. "HPSm, a high performance restricted data flow architecture having minimal functionality." In Proc. 13th Ann. Int. Symp. on Computer Architecture (ISCA-13), 1986.
- W.-M. W. Hwu and Y. N. Patt. 1987. "Checkpoint repair for out-of-order execution machines." In Proc. 14th Ann. Int. Symp. on Computer Architecture (ISCA-14), 1987.
- P. Ibanez, V. Vinals, J. Briz, and M. Garzaran. 1998. "Characterization and improvement of load/store cache-based prefetching." In Int. Conf. on Supercomputing, pp. 369–376, July 1998.
- IBM and Motorola. 1993. PowerPC 601 RISC Microprocessor User's Manual. IBM Microelectronics and Motorola.
- IBM and Motorola. 1994. PowerPC 604 RISC Microprocessor User's Manual. IBM Microelectronics and Motorola.
- IBM. 1981. Information Management System: Programming Reference Manual, 9th Ed., IBM, 1981.
- IBM. 1998a. EDO DRAM 4M x 16 Part No. IBM0165165PT3C. <http://www.chips.ibm.com/products/memory/88H2011/88H2011.pdf>.
- IBM. 1998b. SDRAM 1M x 16 x 4 Bank Part No. IBM0364164. <http://www.chips.ibm.com/products/memory/19L3265/19L3265.pdf>.

- IBM. 2002a. The PowerPC 405 Embedded Processor Family. IBM Inc. Microelectronics, 2002. <http://www306.ibm.com/chips/products/powerpc/processors/>.
- IBM. 2002b. The PowerPC 440 Embedded Processor Family. IBM Inc. Microelectronics, 2002. <http://www306.ibm.com/chips/products/powerpc/processors/>.
- IBM. 2002c. IBM Power4 System Architecture White Paper, 2002. <http://www1.ibm.com/servers/eserver/pseries/hardware/whitepapers/power4.html>.
- Infineon. 2001. XC-166 16-bit Embedded Family. Revised Jan. 2001. <http://www.infineon.com/cm upload/documents/036/812/c166sv2um.pdf>.
- J. Inouye, R. Konuru, J. Walpole, and B. Sears. 1992. The Effects of Virtually Addressed Caches on Virtual Memory Design and Performance, Technical Report CS/E 92-010, Oregon Graduate Institute.
- K. Inoue, K. Kai, and K. Murakami. 1999. "Dynamically variable line-size cache exploiting high on-chip memory bandwidth of merged DRAM/logic LSIs." In Proc. Fifth Int. Symp. on High Performance Computer Architecture (HPCA'99), pp. 218–222, Orlando, FL, January 1999.
- Intel. 1993. Pentium Processor User's Manual. Intel Corporation, Mt. Prospect, IL.
- Intel. 1995. Pentium Pro Family Developer's Manual, Volume 3: Operating System Writer's Guide. Intel Corporation, Mt. Prospect, IL.
- Intel. Intel 875P Chipset: Intel 82875P Memory Controller Hub (MCH) Datasheet. <http://www.intel.com>.
- K. Ishibashi. 1990. "An alpha-immune 2-V supply voltage SRAM using a polysilicon PMOS load cell." *IEEE J. Solid-State Circuits*, SC-25(1), 55–60, Feb. 1990.
- S. Iwasaki. 1980. "Perpendicular magnetic recording." *IEEE Trans. Magnetics*, 16(1), 71–76, 1980.
- S. Iwasaki. 1984. "Perpendicular magnetic recording—Evolution and future." *IEEE Trans. Magnetics*, 20(5), 657–662, 1984.
- S. Iwasaki. 2002. "Perpendicular magnetic recording focused on the origin and its significance." *IEEE Trans. Magnetics*, 38(4), 1609–1641, 2002.
- A. Iyengar. 1996. "Design and performance of a general purpose software cache." *J. Parallel Distributed Computing*, 38(2), 248–255, 1996.
- B. Jacob. 1994. Optimization of Storage Hierarchies," Tech. Rep. CSE-TR-228-95, University of Michigan, May 1994.
- B. Jacob. 1997. "Software-Oriented Memory-Management Design." PhD Thesis, The University of Michigan, July 1997.
- B. Jacob. 1998. "Software-managed caches: Architectural support for real-time embedded systems." In Proc. Int. Workshop on Compiler and Architecture Support for Embedded Systems (CASES'98), Washington, DC, December 1998.
- B. Jacob. 2002a. "Virtual memory." In R. Flynn, Editor, *Computer Sciences*. Macmillan Reference USA: Farmington Hills, MI, 2002.
- B. Jacob. 2002b. "Virtual memory systems and TLB structures." In V. Oklobdzija, Editor, *The Computer Engineering Handbook*, CRC Press, Boca Raton, FL, pp. 5:55–5:65, 2002.
- B. Jacob. 2003. "A case for studying DRAM issues at the system level." *IEEE Micro*, 23(4), 44–56, July/Aug. 2003.
- B. Jacob and S. Bhattacharyya. 2000. Real-Time Memory Management: Compile-Time Techniques and Run-Time Mechanisms that Enable the Use of Caches in Real-Time Systems, Technical Report UMIACS-TR-2000-60, University of Maryland Institute for Advanced Computer Studies (UMIACS) September 2000.
- B. Jacob and S. Bhattacharyya, Editors. 2002. "Embedded systems: The memory resource." Special (and inaugural) issue of *ACM Trans. Embedded Computing Systems*, 1(1), November 2002 (continued as vol. 2, no. 1 in February 2003).
- B. Jacob, P. Chen, S. Silverman, and T. Mudge. 1996. "An analytical model for designing storage hierarchies." *IEEE Trans. Computers*, 45(10), 1180–1194, Oct. 1996.
- B. Jacob, P. Chen, S. Silverman, and T. Mudge. 1997. "A comment on 'An analytical model for designing memory hierarchies.'" *IEEE Trans. Computers*, 46(10), 1151, Oct. 1997.
- B. Jacob and T. Mudge. 1996. Specification of the PUMA Memory Management Design, Technical Report CSE-TR-314-96, University of Michigan.
- B. Jacob and T. Mudge. 1997. "Software-managed address translation." In Proc. Third IEEE Int. Symp. High Performance Computer Architecture (HPCA 1997), pp. 156–167, San Antonio, TX, February 1997.
- B. Jacob and T. Mudge. 1998a. "A look at several memory-management units, TLB-refill mechanisms, and page table organizations." In Proc. Eighth Int. Conf. on

- Architectural Support for Programming Languages and Operating Systems (ASPLOS'98), pp. 295–306, San Jose, CA, 1998.
- B. Jacob and T. Mudge. 1998b. “Virtual memory in contemporary microprocessors.” *IEEE Micro*, 18(4), 60–75, 1998.
- B. Jacob and T. Mudge. 1998c. “Virtual memory: Issues of implementation.” *IEEE Computer*, 31(6), 33–43, 1998.
- B. Jacob and T. Mudge. 2001. “Uniprocessor virtual memory without TLBs.” *IEEE Transactions on Computers*, 50(5), 482–499, May 2001.
- V. Jacobson, R. Braden, and D. Borman. 1992. TCP Extensions for High Performance—Network Working Group Request for Comments 1323. May 1992.
- D. Jacobson and J. Wilkes. 1991. Disk Scheduling Algorithms Based on Rotational Position, Technical Report HPCLCSP-91-7, HP Labs, Palo Alto, CA.
- R. C. Jaeger. 1975. “Comments on ‘An optimized output stage for MOS integrated circuits.’” *IEEE J. Solid-State Circuits*, SC-10, 185–186, June 1975.
- A. Jaleel and B. Jacob. 2001a. “In-line interrupt handling for software-managed TLBs.” In Proc. 19th IEEE Int. Conf. on Computer Design (ICCD 2001), pp. 62–67, Austin, TX, September 2001.
- A. Jaleel and B. Jacob. 2001b. “Improving the precise interrupt mechanism of software-managed TLB miss handlers.” In *High Performance Computing, Lecture Notes in Computer Science*, 2228, 282–293, 2001; B. Monien, V. Prasanna, and S. Vajapeyam, Editors, Springer Publishing, Berlin, Germany, 2001.
- A. Jaleel and B. Jacob. 2005. “Using virtual load/store queues (VLSQs) to reduce the negative effects of reordered memory instructions.” In Proc. 11th IEEE Int. Symp. on High Performance Computer Architecture (HPCA 2005), pp. 191–200, San Francisco, CA, February 2005.
- Aamer Jaleel, Matthew Mattina, and Bruce Jacob. 2001. “Last-level cache (LLC) performance of data-mining workloads on a CMP—A case study of parallel bioinformatics workloads.” In Proc. 12th International Symposium on High Performance Computer Architecture (HPCA 2006). PP. 88–98. Austin TX, February 2006.
- Aamer Jaleel and Bruce Jacob. 2006. “In-line interrupt handling and lock-up free translation lookaside buffers (TLBs).” *IEEE Transactions on Computers*, vol. 55, no. 5, pp. 559–574. May 2006.
- J. Janzen. 2001. “Calculating memory system power for DDR SDRAM.” *Micron Designline*, 10(2), 1–12, 2Q, 2001.
- J. Janzen. 2004. “Calculating memory system power for DDR2.” *Micron Designline*, 13(1), 1Q, 2004.
- L. K. John. 2004. “More on finding a single number to indicate overall performance of a benchmark suite.” *SIGARCH Computer Architecture News*, 32(1), pp. 3–8, Mar. 2004.
- M. Johnson. 1991. *Superscalar Microprocessor Design*. Prentice Hall, New York, 1991.
- T. L. Johnson and W.-M. W. Hwu. 1997. “Run-time adaptive cache hierarchy management via reference analysis.” In Proc. 24th Ann. Int. Symp. on Computer Architecture (ISCA-24), pp. 315–326, Denver, CO, 1997.
- D. Joseph and D. Grunwald. 1997. “Prefetching using Markov predictors.” In Proc. 24th Int. Symp. on Computer Architecture (ISCA 1997), pp. 252–263, Denver, CO, June 1997.
- N. P. Jouppi. 1990. “Improving direct-mapped cache performance by the addition of a small fully-associative cache and prefetch buffers.” In Proc. 17th Ann. Int. Symp. on Computer Architecture (ISCA-17), pp. 364–373, Seattle, WA, May 1990.
- N.P. Jouppi. 1993. “Cache write policies and performance.” In Proc. Int. Symp. Computer Architecture (ISCA), 191–201, 1993.
- T. Juan, T. Lang, and J.J. Navarro. 1997. “Reducing TLB power requirements.” In Proc. 1997 IEEE Int. Symp. Low Power Electronics and Design (ISLPED'97), pp. 196–201, Monterey, CA, August 1997.
- E. Jul, H. Levy, N. Hutchinson, and A. Black. 1988. “Fine-grained mobility in the Emerald system.” *ACM Trans. Computer Systems*, 6(1), 109–133, 1988.
- D. R. Kaeli and P. G. Emma. 1991. “Branch history table prediction of moving target branches due to subroutine returns.” In Proc. 18th Ann. Int. Symp. on Computer Architecture (ISCA), 34–42, 1991.
- D. Kalinsky. 1999. “A survey of task schedulers.” In Embedded Systems Conf. 1999, San Jose, CA, September 1999.
- H. Kalter, J. Barth, J. Dilorenzo, C. Drake, J. Fifield, W. Hovis, G. Kelley, S. Lewis, J. Nickel, C. Stapper, and J. Yankosky,

- 1990a. "A 50 ns 16 Mb DRAM with a 10 ns data rate." In 37th IEEE Int. Solid-State Circuits Conf. (ISSCC), pp. 232–233, San Francisco, CA, February 1990.
- H. L. Kalter, C.H. Stapper, J.E. Barth, Jr., J. DiLorenzo, C.E. Drake, J.A. Fifield, G.A. Kelley, Jr., S.C. Lewis, W.B. van der Hoeven, and J.A. Yankosky. 1990b. "A 50-ns 16-Mb DRAM with a 10-ns data rate and on-chip ECC." *IEEE J. Solid-State Circuits*, 25(5), 1118–1128, Oct. 1990.
- M. Kandemir, J. Ramanujam, M. J. Irwin, N. Vijaykrishnan, I. Kadayif, and A. Parikh. 2001. "Dynamic management of scratch-pad memory space." In Proc. 38th Conf. on Design Automation (DAC 2001), pp. 690–695, 2001.
- G. Kane. 1996. *PA-RISC 2.0 Architecture*. Prentice Hall PTR, Upper Saddle River, NJ, 1996.
- G. Kane and J. Heinrich. 1992. *MIPS RISC Architecture*. Prentice Hall, Englewood Cliffs, NJ, 1992.
- C. Karabotsos. 2002. Personal communication.
- M. Karlsson, F. Dahlgren, and P. Stenstrom. 2000. "A prefetching technique for irregular accesses to linked data structures." In Proc. 6th Int. Conf. on High Performance Computer Architecture (HPCA), pp. 206–217, Toulouse, France, January 2000.
- K. Karplus and A. Nicolau. 1985. "Efficient hardware for multiway jumps and pre-fetches." In Proc. 18th Ann. Workshop on Microprogramming (MICRO-18), pp. 11–18, Pacific Grove, CA, December 1985.
- V. Kathail, M. S. Schlansker, and B. R. Rau. 2000. HPL-PD Architecture Specification: Version 1.1, HP Laboratories Technical Report HPL-93-80(R.1), Palo Alto, CA, February 2000.
- S. Kaxiras, Z. Hu, and M. Martonosi. 2001. "Cache decay: Exploiting generational behavior to reduce cache leakage power." In Proc. 28th Int. Symp. on Computer Architecture (ISCA-28), pp. 240–251, Göteborg, Sweden, June 2001.
- K. Keeton et al. 1998. "Performance characterization of a quad Pentium Pro SMP using OLTP workloads." In Proc. Int. Symp. Computer Architecture (ISCA), 25, June 1998, pp. 15–26.
- P. Keleher, A. L. Cox, and W. Zwaenepoel. 1992. "Lazy release consistency for software distributed shared memory." In Proc. 19th Ann. Int. Symp. on Computer Architecture (ISCA), pp. 13–21, May 1992.
- P. Keleher, S. Dwarkadas, A. Cox, and W. Zwaenepoel. 1994. "TreadMarks: Distributed shared memory on standard workstations and operating systems." In Proc. 1994 Winter Usenix Conf., pp. 115–131, January 1994.
- M. Kellogg. 2002. Personal communication.
- C. N. Keltcher. 2002. "The AMD Hammer Processor Core." Presentation given at HotChips 14. August 2002.
- R. E. Kessler and M. D. Hill. 1992. "Page placement algorithms for large real-indexed caches." *ACM Trans. Comput. Syst.*, 10(4), 338–359, Nov. 1992.
- Y. A. Khalidi, M. Talluri, M. N. Nelson, and D. Williams. 1993. "Virtual memory support for multiple page sizes." In Proc. Fourth Workshop on Workstation Operating Systems, 1993.
- Y. A. Khalidi and M. Talluri. 1995. Improving the Address Translation Performance of Widely Shared Pages, Technical Report SMLI TR-95-38, Sun Microsystems.
- T. Kilburn, D. B. G. Edwards, M. J. Lanigan, and F. H. Sumner. 1962. "One-level storage system." *IRE Trans. Electronic Computers*, EC-11(2), 223–235, April 1962.
- M. V. Kim. 1986. "Synchronized disk interleaving." *IEEE Trans. Computers*, C-35 (11), 978–988, November 1986.
- C. Kim, D. Burger, and S.W. Keckler. 2002. "An adaptive, non-uniform cache structure for wire-delay dominated on-chip caches." In Proc. Int. Conf. Architectural Support for Programming Languages and Operating Systems (ASPLOS-10), pp. 211–222, San Jose, CA, December 2002.
- N. S. Kim et al. 2004a. "Circuit and microarchitectural techniques for reducing cache leakage power." *IEEE J. Solid-State Circuits*, 12(2), 167–184, Feb. 2004.
- Y. I. Kim, K. H. Yang, and W. S. Lee. 2004b. "Thermal degradation of DRAM retention time: Characterization and improving techniques." In Proc. 42nd Ann. Int. Reliability Physics Symposium, pp. 667–668, 2004.
- N. S. Kim et al. 2004c. "Circuit and microarchitectural techniques for reducing cache leakage power." *IEEE J. Solid-State Circuits*, 12(2), 167–184, Feb. 2004.
- J. Kin, M. Gupta and W. Mangione-Smith. 1997. "The filter cache: An energy efficient memory structure." In Proc. 30th Ann. Int. Symp. on Microarchitecture (MICRO'97), pp. 184–193, Research Triangle Park, NC, December 1997.
- J. Kin, M. Gupta, and W. H. Mangione-Smith. 2000. "Filtering memory references to increase energy efficiency." *IEEE Trans. Computers*, 49(1), 1–15, Jan. 2000.

- D. B. Kirk. 1989. "SMART (strategic memory allocation for real-time) cache design." In Proc. IEEE Symp. on Real-Time Systems (RTSS), pp. 229–237, December 1989.
- A. C. Klaiber and H. M. Levy. 1991. "An architecture for software-controlled data prefetching." In Proc. 18th Int. Symp. on Computer Architecture (ISCA), pp. 43–53, Toronto, Canada, May 1991.
- L. Kleinrock. 1975. *Queueing Systems Volume 1: Theory*. John Wiley & Sons, Hoboken, NJ, 1975.
- J. Knight. 1976. "CASHEW—A proposed permanent data storage system." Computer Center Report, Lawrence Berkeley Laboratory, May 1976.
- D. E. Knuth. 1963. "Computer-drawn flowcharts." *Commun. ACM*, 6(9), 555–563, Sep. 1963.
- D. E. Knuth. 1973. *The Art of Computer Programming—Volume 3 (Sorting and Searching)*. Addison-Wesley, Reading, MA, 1973.
- U. Ko, P. T. Balsara, and A. K. Nanda. 1998. "Energy optimization of multilevel cache architectures for RISC and CISC processors." *IEEE Trans. Very Large Scale Integr. Syst.*, 6(2), 299–308, June 1998.
- P. Kohout, B. Ganesh, and B. Jacob. 2003. "Hardware support for real-time operating systems." In Proc. First IEEE/ACM/IFIP Int. Conf. on Hardware/Software Codesign and System Synthesis (CODES+ISSS 2003), pp. 45–51, Newport Beach, CA, October 2003.
- K. Korner. 1990. "Intelligent caching for remote file service." In Proc. Tenth Int. Conf. on Distributed Computer Systems, pp. 220–226, IEEE Press, New York, 1990.
- D. F. Kotz and C. S. Ellis. 1990. "Prefetching in file systems for MIMD multiprocessors." *IEEE Trans. Parallel Distributing Syst.* 1(2), 218–230. Apr. 1990.
- D. Koufaty and J. Torrellas. 1998. "Comparing data forwarding and prefetching for communication-induced misses in shared-memory MPs." In Int. Conf. on Supercomputing, pp. 53–60, July 1998.
- C. Kozyrakis, S. Perissakis, D. Patterson, T. Anderson, K. Asanovic, N. Cardwell, R. Fromm, J. Golbus, B. Gribstad, K. Keeton, R. Thomas, N. Treuhaf, and K. Yelick. 1997. "Scalable processors in the billion-transistor era: IRAM." *IEEE Computer*, 30(9), 75–78, Sept. 1997.
- T. M. Kroeger and D. D. E. Long. 1996. "Predicting file system actions from prior events." In Proc. USENIX 1996 Technical Conference, pp. 319–328, San Diego, CA, January 1996.
- D. Kroft. 1981. "Lockup-free instruction fetch/prefetch cache organization." In Proc. 8th Int. Symp. on Computer Architecture (ISCA), pp. 81–87, May 1981.
- A. Kumar. 1996. "The HP PA-8000 RISC CPU: A high performance out-of-order processor." In Hot Chips 8: A Symp. on High-Performance Chips, Stanford, CA. <http://infopad.eecs.berkeley.edu/HotChips8/>.
- J. J. Labrosse. 1999. *MicroC/OS-II: The Real-Time Kernel*. R&D Books (Miller Freeman, Inc.), Lawrence, KS, 1999.
- A. Lai, C. Fide, and B. Falsafi. 2001. "Dead-block prediction and dead-block correlating prefetchers." In The 28th Int. Symp. on Computer Architecture (ISCA), pp. 144–154, June 2001.
- L. Lamport. 1979. "How to make a multiprocessor computer that correctly executes multiprocess programs." *IEEE Trans. Computers*, C-28(9), 690–691, 1979.
- D. Landskov, S. Davidson, B. Shriver, and P. W. Mallett. 1980. "Local microcode compaction techniques." *ACM Computing Surveys*, 12(3), 261–294. Sept. 1980.
- P. Lapsley, J. Bier, A. Shoham, and E. A. Lee. 1994. *DSP Processor Fundamentals: Architectures and Features*. Berkeley Design Technology, Inc., Berkeley, CA, 1994.
- P. Lapsley, J. Bier, A. Shoham, and E. A. Lee. 1997. *DSP Processor Fundamentals*. IEEE Press, Piscataway, NJ, 1997.
- E. Larson and T. Austin. 2000. "Compiler controlled value prediction using branch predictor based confidence." In Proc. 33th Ann. Int. Symp. on Microarchitecture (MICRO-33), IEEE Computer Soc., Los Alamitos, CA, December 2000.
- E. Larson, S. Chatterjee, and T. Austin. 2001. "The MASE Microarchitecture Simulation Environment" 2001 IEEE Int. Symp. Performance Analysis of Systems and Software (ISPASS-2001), June 2001.
- T. Laskodi, B. Eifrig, and J. Gait. 1988. "A UNIX file system for a write-once optical disk." In Proc. Summer 1988 USENIX Conf., pp. 51–60, June 1988.
- LCTES Panel. 2003. "Compilation challenges for network processors." Industrial Panel, ACM Conf. Languages, Compilers and Tools for Embedded Systems (LCTES), June 2003.
- F. F. Lee. 1960. "Study of 'look aside' memory." *IEEE Trans. Computers*, 18(11), 1062–1064, Nov. 1960.

- J. Lee and A. J. Smith. 1984. "Branch prediction strategies and branch target buffer design." *IEEE Computer*, 17(1), 6–22, Jan. 1984.
- E. A. Lee and D. G. Messerschmitt. 1987. "Synchronous dataflow." *Proc. IEEE*, 75(9), 1235–1245, 1987.
- C. C. Lee, I. C. Chen, and T. Mudge. 1997a. "The bi-mode branch predictor." In Proc. 30th Ann. Int. Symp. on Microarchitecture (MICRO-30), pp. 4–13, Research Triangle Park, NC, December 1997.
- C. Lee, M. Potkonjak, and W. Mangione-Smith. 1997b. "MediaBench: A tool for evaluating and synthesizing multimedia and communications systems." In Proc. 30th Ann. Int. Symp. on Microarchitecture (MICRO'97), pp. 330–335, Research Triangle Park, NC, December 1997.
- H.-H. Lee and G. Tyson. 2000. "Region-based caching: An energy-delay efficient memory architecture for embedded processors." In Proc. Int. Conf. on Compilers, Architectures, and Synthesis for Embedded Systems (CASES 2000), pp. 120–127, San Jose, CA, November 2000.
- T. Lee. 2002. Personal communication.
- S. J. Leffler, M. K. McKusick, M. J. Karels, and J. S. Quarterman. 1989. *The Design and Implementation of the 4.3BSD UNIX Operating System*. Addison-Wesley, Reading, MA, 1989.
- C. Lefurgy, P. Bird, I.-C. Chen, and T. Mudge. 1997. "Improving code density using compression techniques." In Proc. 30th Ann. Int. Symp. on Microarchitecture (MICRO 1997), pp. 194–203, Research Triangle Park, NC, December 1997.
- K. Li and P. Hudak. 1986. "Memory coherence in shared virtual memory systems." In Proc. Fifth Ann. ACM Symp. on Principles of Distributed Computing, Calgary, Alberta, Canada, August 11–13, 1986.
- K. Li and P. Hudak. 1989. "Memory coherence in shared virtual memory systems." *ACM Trans. Comput. Syst.*, 7(4), 321–359, Nov. 1989.
- Y. Li, M. Potkonjak, and W. Wolf. 1997. "Real-time operating systems for embedded computing." In Int. Conf. on Computer Design (ICCD), Austin, TX, October 1997.
- J. Liedtke. 1993. "Improving IPC by kernel design." In Proc. Fourteenth ACM Symp. on Operating Systems Principles (SOSP-14), pp. 175–187, 1993.
- J. Liedtke. 1995a. "Address space sparsity and fine granularity." *ACM Operating Systems Rev.*, 29(1), 87–90, 1995.
- J. Liedtke. 1995b. "On micro-kernel construction." In Proc. Fifteenth ACM Symp. on Operating Systems Principles (SOSP-15), 1995.
- J. Liedtke and K. Elphinstone. 1996. "Guarded page tables on MIPS R4600." *ACM Operating Systems Rev.*, 30(1), 4–15, 1996.
- C. Liema, F. Nacabal, C. Valderrama, P. Paulin, and A. Jerraya. 1997. "System-on-a-chip cosimulation and compilation." *IEEE Design Test Computers*, 14(2), 16–25, April–June 1997.
- W. Lin, S. Reinhardt, and D. Burger. 2001. "Reducing DRAM latencies with an integrated memory hierarchy design." In Proc. 7th Int. Symp. on High-Performance Computer Architecture (HPCA), January 2001.
- F. J. List. 1986. The Static Noise Margin of SRAM Cells, ESSCIRC Dig. Tech. Papers, Sept. 1986, pp. 16–18, 1986.
- J. W. S. Liu. 2000. *Real-Time Systems*. Prentice Hall, Upper Saddle River, NJ, 2000.
- J. Lohstroh, E. Seevinck, and J. de Groot. 1983. "Worst-case static noise margin criteria for logic circuits and their mathematical equivalence." *IEEE J. Solid-State Circuits*, SC-18(6), 803–807, Dec. 1983.
- T. C. Lowe. 1968. "The influence of data base characteristics and usage on direct access file organization." *J. ACM*, 15(4), 535–548, Oct. 1968.
- T. C. Lowe. 1969. "Analysis of Boolean program models for time-shared, paged environments." *Commun. ACM*, 12(4), 199–205, April 1969.
- T. C. Lowe. 1970. "Automatic segmentation of cyclic program structures based on connectivity and processor timing." *Commun. ACM*, 13(1), 3–6, Jan. 1970.
- E. S. Lowry and C. W. Medlock. 1969. "Object code optimization." *Commun. ACM*, 12(1), 13–22, Jan. 1969.
- C.-K. Luk and T. C. Mowry. 1996. "Compiler-based prefetching for recursive data structures." In Proc. Seventh Int. Conf. on Architectural Support for Programming Languages and Operating Systems (ASPLOS), pp. 222–233, Cambridge, MA, October 1996.
- C.-K. Luk and T. C. Mowry. 1998. "Cooperative instruction prefetching in modern processors." In Proc. 31st Ann.

- ACM/IEEE Int. Symp. on Microarchitecture (MICRO), pp. 182–194, November 30–December 2, 1998.
- A. Luotonen and K. Altis. 1994. “World-wide Web proxies.” *Computer Networks ISDN Systems*, 27(2), 147–154, November 1994.
- J. E. MacDonald and K. L. Sigworth. 1975. “Storage hierarchy optimization procedure.” *IBM J. Res. Dev.*, 133–140, March 1975.
- J. Macri. 2002. Personal communication.
- K. Mai et al. 1998. “Low-power SRAM design using half-swing pulse-mode techniques.” *IEEE J. Solid-State Circuits*, 33(11), 1659–1670, November 1998.
- A. Malik, B. Moyer, and D. Cermak. 2000. “A low power unified cache architecture providing power and performance flexibility.” In Proc. Int. Symp. on Low Power Electronics and Design (ISLPED), pp. 241–243, Rapallo, Italy, June 2000.
- M. Mamidipaka and N. Dutt. 2004. eCACTI: An Enhanced Power Estimation Model for On-Chip Caches, Center for Embedded Computer Systems, Technical Report TR 04-28, Oct. 2004.
- A. A. Mamun, G. Guo, and B. Chao. 2006. *Hard Disk Drive*. CRC Press, Boca Raton, FL, 2006.
- B. A. Marron and P. A. de Maine. 1967. “Automatic data compression.” *Commun. ACM*, 10(11), 711–715, Nov. 1967.
- R. E. Matick and S. E. Schuster. 2005. “Logic-based eDRAM: Origins and rationale for use.” *IBM J. Res. Dev.*, 49(1), 145–165, 2005.
- Matlab 6.1. 2001. The Math Works, Inc., 2001. <http://www.mathworks.com/products/matlab/>.
- R. L. Mattson, J. Gecsei, D. R. Slutz, and I. L. Traiger. 1970. “Evaluation techniques for storage hierarchies.” *IBM Syst. J.*, 9(2), 78–117, 1970.
- R. Mattson and S. Ng. 1992. “Maintaining good performance in disk arrays during failure via uniform parity group distribution.” In Proc. 1st Int. Symp. on High Performance Distributed Computing, pp. 260–269, Syracuse, NY, 1992.
- R. L. Mattson and S. Ng. 1993. Method and Means for Managing DASD Array Accesses when Operating in Degraded Mode. US Patent No. 5265098. U.S. Patent and Trademark Office.
- T. May and M. Woods. 1978. “A new physical mechanism for soft errors in dynamic memories.” In Proc. Sixteenth Int. Reliability Physical Symp., April 1978.
- C. May, E. Silha, R. Simpson, and H. Warren, Editors. 1994. *The PowerPC Architecture: A Specification for a New Family of RISC Processors*. Morgan Kaufmann, San Francisco, CA, 1994.
- J. McCalpin. 2000. “An industry perspective on performance characterization: Applications vs benchmarks.” Keynote address at Third Ann. IEEE Workshop on Workload Characterization, Austin TX, September 16, 2000.
- J. McCalpin. STREAM: Sustainable Bandwidth in High Performance Computers. <http://www.cs.virginia.edu/stream/>.
- J. McCarthy. 1960. “Recursive functions of symbolic expressions and their computation by machine, Part I.” *Commun. ACM*, 3(4), 184–195, Apr. 1960.
- S. McFarling. 1989. “Program optimization for instruction caches.” In Proc. Third Int. Conf. on Architectural Support for Programming Languages and Operating Systems (ASPLOS-1989), pp. 183–191, 1989.
- S. McFarling. 1991. Cache Replacement with Dynamic Exclusion, WRL Technical Note TN-22, Digital Western Research Laboratory, November 1991. (Note: later published in ISCA, see McFarling [1992].)
- S. McFarling. 1992. “Cache replacement with dynamic exclusion.” In Proc. 19th Ann. Int. Symp. on Computer Architecture (ISCA ’92), pp. 191–200, Queensland, Australia, May 19–21, 1992, ACM Press, New York, 1992. DOI= <http://doi.acm.org/10.1145/139669.139727>.
- S. McKee. 1994. Dynamic Access Ordering: Bounds on Memory Bandwidth, Technical Report CS-94-38, University of Virginia, October 1994.
- S. A. McKee and W. A. Wulf. 1995. “Access ordering and memory-conscious cache utilization.” In Proc. Int. Symp. on High Performance Computer Architecture (HPCA’95), pp. 253–262, Raleigh, NC, January 1995.
- S. McKee et al. 1996a. “Design and evaluation of dynamic access ordering hardware.” In Proc. Int. Conf. on Supercomputing, May 1996.
- S. McKee, A. Aluwihare, B. Clark, R. Klenke, T. Landon, C. Oliver, M. Salinas, A. Szymkowiak, K. Wright, W. Wulf, and J. Aylor. 1996b. “Design and evaluation of dynamic access ordering hardware.” In Proc. Int. Conf. on Supercomputing, Philadelphia, PA, May 1996.

- W. McKee et al. 1996c. "Cosmic ray neutron induced upsets as a major contributor to the soft error rate of current and future generation DRAMs." In Proc. Int. Reliability Physical Symp., 1996.
- Mcore. 1997. M-CORE Reference Manual. Motorola Literature Distribution, Denver, CO, 1997.
- Mcore. 1998. M-CORE MMC2001 Reference Manual. Motorola Literature Distribution, Denver, CO, 1998.
- C. D. Mee and E. D. Daniel, Editors. 1996. *Magnetic Recording Technology*. McGraw-Hill, New York, 1996.
- J. Mellor-Crummey, D. Whalley, and K. Kennedy. 1999. "Improving memory hierarchy performance for irregular applications." In Proc. 13th Int. Conf. on Supercomputing (ICS '99), pp. 425–433, Rhodes, Greece, June 20–25, 1999, ACM Press, New York, 1999.
- S. W. Melvin, M. C. Shebanow, and Y. N. Patt. 1988. "Hardware support for large atomic units in dynamically scheduled machines." In Proc. 21st Ann. Int. Symp. on Microarchitecture (MICRO-21), pp. 60–63, San Diego, CA, November 1988.
- J. M. Menon, R. L. Mattson, and S. Ng. 1993. Method and Means for Distributed Sparing in DASD Arrays. US Patent No. 5258984. U.S. Patent and Trademark Office.
- M. Mesnier, G. R. Ganger, and E. Riedel. 2003. "Object-based storage." *IEEE Commun. Magazine*, 41(8), 84–90, 2003.
- Micron. 1995. 1 Gbit DDR2 SDRAM Device Datasheet, Micron Inc.
- Micron. 2005. *240-Pin 512MB/1GB/2GB DDR2 SDRAM FBDIMM (DR FB x72) Features*, April 2005.
- Micron. 2006. *1Gb: x4,x8,x16 DDR SDRAM Features*, January 2006.
- M. A. Milne. 1971. "CLUSTR: A program for structuring design problems." In Proc. 8th Workshop on Design Automation (DAC '71), Atlantic City, New Jersey, United States, June 28–30, 1971, 242–249, ACM Press, New York, 1971.
- O. Minato et al. 1987. "A 42 ns 1Mb CMOS SRAM." *ISSCC Dig. Tech. Papers*, Feb., 260–261, 1987.
- J. Mitchell, J. Gibbons, G. Hamilton, P. Kessler, Y. Khalidi, P. Kougiouris, P. Madany, M. Nelson, M. Powell, and S. Radia. 1994. "An overview of the Spring system." In Proc. IEEE Compton, 1994.
- N. Mitchell, L. Carter, and J. Ferrante. 1999. "Localizing non-affine array references." In Proc. Int. Conf. on Parallel Architectures and Compilation Techniques, Newport Beach, LA, October 1999.
- O. Mock and C. J. Swift. 1959. "The Share 709 system: Programmed input-output buffering." *J. ACM (JACM)*, 6(2), 145–151, April 1959.
- J. C. Mogul. 1996. "Hinted caching in the Web." In Proc. Seventh ACM SIGOPS European Workshop, pp. 103–108, Connemara, Ireland, September 1996.
- J. Montanaro et al. 1996. "A 160-MHz, 32-b, 0.5-W CMOS RISC microprocessor." *JSSC*, 31(11), 1703–1714, Nov. 1996.
- Y. Mori, R.-I. Yamada, S. Kamohara, M. Moniwa, K. Ohyu, and T. Yamanaka. 2001. "A new method for predicting distribution of DRAM retention time." In Proc. 39th Ann. Int. Reliability Physics Symposium, pp. 7–11, 2001.
- Y. Mori, K. Ohyu, K. Okonogi, and R.-I. Yamada. 2005. "The origins of variable retention time in DRAM." In Int. Electron Devices Meeting Technical Digest, pp. 1057–1060, 2005.
- C. A. Moritz, M. Frank, and S. Amarasinghe. 2000. "FlexCache: A framework for flexible compiler generated data caching." In The 2nd Workshop on Intelligent Memory Systems, Boston, MA, November 12, 2000.
- J. E. B. Moss. 1992. "Working with persistent objects: To swizzle or not to swizzle." *IEEE Trans. Software Eng.*, 18(8), 657–673, Aug. 1992.
- Motorola/Freescale. 2002a. Coldfire MCF5206E 32-bit CPU. Motorola/Freescale, Revised 2002. <http://www.freescale.com/files/dsp/doc/fact sheet/CFPRODFACT.pdf>.
- Motorola/Freescale. 2002b. MPC500 32-bit MCU Family. Motorola/Freescale, Revised July 2002. <http://www.freescale.com/files/-microcontrollers/doc/fact sheet/MPC500FACT.pdf>.
- Motorola/Freescale. 2003. Dragonball MC68SZ328 32-bit Embedded CPU. Motorola/Freescale, Revised April 2003. <http://www.freescale.com/files/32bit/doc/fact sheet/MC68SZ328FS.pdf>.
- M. Moudgill and S. Vassiliadis. 1996. "Precise interrupts." *IEEE Micro*, 16(1), 58–67, Feb. 1996.
- T. Mowry and A. Gupta. 1991. "Tolerating latency through software-controlled prefetching in shared-memory

- multiprocessors." *J. Parallel Distributed Computing*, 12(2), 87–106, June 1991.
- T. Mowry, M. Lam, and A. Gupta. 1992. "Design and evaluation of a compiler algorithm for prefetching." In Proc. 5th Int. Conf. on Architectural Support for Programming Languages and Operating Systems (ASPLOS-V), pp. 62–73, Boston, MA, October 1992.
- T. C. Mowry. 1994. Tolerating Latency Through Software-Controlled Data Prefetching, PhD Thesis. Technical report, Stanford University, Stanford, CA, March 1994.
- T. Mowry. 1998. "Tolerating latency in multiprocessors through compiler-inserted prefetching." *Trans. Comput. Syst.*, 16(1), 55–92, Feb. 1998.
- F. Mueller. 1995. "Compiler support for software-based cache partitioning." In Proc. ACMSIGPLAN 1995 Workshop on Languages, compilers, & Tools for Real-Time Systems, pp. 125–133, ACM Press, New York, 1995.
- J. M. Mulder, N. T. Quach, and M. J. Flynn. 1991. "An area model for on-chip memories and its application." *IEEE J. Solid-State Circuits*, 26(2), 98–106, 1991.
- J. E. Mulford and R. K. Ridall. 1971. "Data compression techniques for economic processing of large commercial files." In Proc. 1971 Int. ACM SIGIR Conf. on Information Storage and Retrieval (SIGIR '71), pp. 207–215, College Park, Maryland, April 01–02, 1971, ACM Press, New York, 1971.
- R. B. Mulvany and L. H. Thompson. 1981. "Innovations in disk file manufacturing." *IBM J. Res. Dev.*, 25(5), 663–675, 1981.
- C. D. Murta, V. Almeida, and W. Meira, Jr. 1998. "Analyzing performance of partitioned caches for the WWW." Proc. 3rd Int. WWW Caching Workshop, June 1998.
- D. Nagle. 1995. Personal communication.
- D. Nagle, R. Uhlig, T. Stanley, S. Sechrest, T. Mudge, and R. Brown. 1993. "Design tradeoffs for software-managed TLBs." In Proc. 20th Ann. Int. Symp. on Computer Architecture (ISCA-20), 1993.
- D. Nagle, R. Uhlig, T. Mudge, and S. Sechrest. 1994. "Optimal allocation of on-chip memory for multiple-API operating systems." In Proc. 21st Ann. Int. Symp. on Computer Architecture (ISCA-1994), pp. 358–369, 1994.
- R. Nair. xprof/xtrace—An RS/6000 Xwindows-Based Tracing and Profiling Package, Technical report, IBM T. J. Watson Research Lab.
- R. Nair. 1996. "Profiling IBM RS/6000 applications." *Int. J. Computer Simulation*, 6(1), 101–112, 1996.
- R. Nair and M. E. Hopkins. 1997. "Exploiting instruction level parallelism in processors by caching scheduled groups." In Proc. 24th Ann. Int. Symp. on Computer Architecture (ISCA-24), pp. 13–25, Denver, CO, 1997.
- K. Nakamura. 1997. "A 500-MHz 4-Mb CMOS pipeline-burst cache SRAM with point-to-point noise reduction coding I/O." *IEEE J. Solid-State Circuits*, 32(11), 1758–1765, Nov. 1997.
- H. Nambu et al. 1998a. "A 1.8-ns access, 550MHz, 4.5-Mb CMOS SRAM." *IEEE J. Solid-State Circuits*, 33(11), 1650–1658, Nov. 1998.
- H. Nambu et al. 1998b. "A 1.8 ns access, 550 MHz 4.5 Mb CMOS SRAM." In 1998 IEEE Int. Solid State Circuits Conf. Dig. *Tech. Papers*, pp. 360–361, 1998.
- C. Natarajan, B. Christenson, and F. Briggs. 2004. "A study of performance impact of memory controller features in multi-processor server environment." In Proc. 3rd Workshop on Memory Performance Issues (WMPPI-2004), 2004.
- B. Nayfeh et al. 1996a. "Evaluation of design alternatives for a multiprocessor microprocessor." Int. Symp. on Computer Architecture (ISCA-23), pp. 67–77, May 1996.
- B. A. Nayfeh et al. 1996b. "The impact of shared-cache clustering in small-scale shared-memory multiprocessors." Int. Symp. High Performance Computer Architecture (HPCA-2), pp. 74–84, February 1996.
- M. Nelson, B. Welch, and J. Ousterhout. 1988. "Caching in the Sprite Network File System." *ACM Trans. Comput. Syst.*, 6(1), 134–154, Feb. 1988.
- S. Ng. 2006. Personal communication.
- S. Ng. 1986. "Reliability and availability of duplex systems: Some simple models." *IEEE Trans. Reliability, R-*, 35(3), 295–300, 1986.
- S. Ng. 1987. "Reliability availability and performance analysis of duplex disks systems." In Proc. IASTED Int. Symp. on Reliability and Control, pp. 5–9, Paris, France, 1987.

- S. Ng. 1989. "Some design issues of disk arrays." In *CompCon Spring89*, pp. 137–142, San Francisco, CA, 1989.
- R. Ng, C. Faloutsos, and T. Sellis. 1991. "Flexible buffer allocation based on marginal gains." In *Proc. 1991 ACM SIGMOD Int. Conf. on Management of Data (SIGMOD '91)*, pp. 387–396, Denver, Colorado, United States, May 29–31, 1991, J. Clifford and R. King, Eds., ACM Press, New York, 1991.
- S. Ng. 1991. "Improving disk performance via latency reduction." *IEEE Trans. Computers*, 40(1), 22–30, 1991.
- S. Ng. 1994a. "Crosshatch disk array for improved reliability and performance." In *Proc. 21st Int. Symp. on Computer Architecture (ISCA)*, pp. 255–264, Chicago, IL, 1994.
- S. Ng. 1994b. Method and Means for Optimally Accessing Data Residing on Dual Actuator DASDs. US Patent No. 5341351. U.S. Patent and Trademark Office.
- S. Ng. 1994c. "Sparing for redundant disk arrays." *Distributed Parallel Databases*, 2(2), 133–149, 1994.
- S. Ng. 1995. Two-Dimensional Disk Array. US Patent No. 5412661. U.S. Patent and Trademark Office.
- S. Ng. 1998. "Advances in disk technology: Performance issues." *Computers*, pp. 75–81, 1998.
- S. Ng. 1999. System for Handling Missed Revolution in a Disk Drive by Aborting the Execution of Primary Command and Executing Secondary Command if a Missed Revolution Occurs. US Patent No. 5991825. U.S. Patent and Trademark Office.
- S. Ng. 2001a. Method of System for Determining the Data Layout Geometry of a Disk Drive. US Patent No. 6237070. U.S. Patent and Trademark Office.
- S. Ng. 2001b. Method of System for Determining the Data Layout Geometry of a Disk Drive. US Patent No. 6253279. U.S. Patent and Trademark Office.
- S. Ng. and R. Mattson. 1994. "Uniform parity group distribution in disk arrays with multiple failures." *IEEE Trans. Computers*, 43(4), 501–506, 1994.
- S. Ng. 2006. Personal communication.
- A. Nicolau. 1989. "Run-time disambiguation: Coping with statically unpredictable dependencies." *IEEE Trans. Computers*, 38(5), 663–678, 1989.
- J. Nievergelt. 1965. "On the automatic simplification of computer programs." *Commun. ACM*, 8(6), 366–370, June 1965.
- K. Noda et al. 1998. "A 1.9 um² loadless CMOS four-transistor SRAM cell in a 0.18um² logic technology." *IEDM Tech. Dig.*, 847–850, 1998.
- Y. Nunomura et al. 1997. "M32R/D—Integrating DRAM and microprocessor." *IEEE Micro*, 17(6), 40–48, Nov. 1997.
- NVIDIA. Technical Brief: NVIDIA nForce Integrated Graphics Processor (IGP) and Dynamic Adaptive Speculative Pre-Processor (DASP). <http://www.nvidia.com/>.
- E. I. Organick. 1972. *The Multics System: An Examination of Its Structure*. The MIT Press, Cambridge, MA, 1972.
- K. Osada et al. 2001. "Universal-Vdd 0.65-2.0V 32-kB cache using a voltage-adapted timing-generation scheme and a lithographically symmetrical cell." *IEEE J. Solid-State Circuits*, 36(11), 1738–1744, Nov. 2001.
- R. Oswald. 1974. "Design of a disk file head-positioning servo." *IBM J. Res. Dev.*, 18, 506–512, 1974.
- N. K. Ouchi. 1978. System for Recovering Data Stored in Failed Memory Unit. US Patent No. 4092732. U.S. Patent and Trademark Office.
- A. O'Donnell. 2002. Personal communication.
- C. W. Padgett and F. L. Newman. 1974. Memory Clocking System. US Patent Number 3,943,496. U.S. Patent and Trademark office, Submitted on September 9, 1974.
- V. N. Padmanabhan and J. C. Mogul. 1996. "Using predictive prefetching to improve World Wide Web latency." *Computer Commun. Rev.*, 26(3), 22–39, July 1996.
- S. Palacharla and R. Kessler. 1994. "Evaluating Stream Buffers as a Secondary Cache Replacement." In *The 21st Int. Symp. on Computer Architecture (ISCA)*, pp. 24–33, April 1994.
- S. Palacharla, N. P. Jouppi, and J. E. Smith. 1996. Quantifying the complexity of superscalar processors, Technical Report CS-TR-96-1328, university of Wisconsin, Madison November 19, 1996.
- P. R. Panda, N. D. Dutt, and A. Nicolau. 2000. "On-chip vs. off-chip memory: The data partitioning problem in embedded processor-based systems." *ACM Trans. Design Automation Electronic Systems*, 5(3), July 2000.
- H. C. Park et al. 1998. "A 833-Mb/s 2.5-V 4-Mb double-date-rate SRAM," In 1998 IEEE Int. Solid State Circuits Conf. Dig. Tech. Papers, pp. 356–357, 1998.
- Y. Park and B. Goldberg. 1992. "Escape analysis on lists." In *Proc. ACM SIGPLAN1992 Conf. on Programming*

- Language Design and Implementation (PLDI), pp. 116–127, ACM Press, New York, 1992.
- D. Patterson, G. Gibson, and R. H. Katz. 1988. “A case for redundant arrays of inexpensive disks (RAID).” In Proc. ACM SIGMOD Conf. pp. 109–116, Chicago, IL, 1988.
- R. H. Patterson, G. Gibson, G. Ginting, D. Stodolsky, and J. Zelenka. 1995. “Informed prefetching and caching.” In Proc. 15th Symp. on Operating Systems Principles (SOSP), pp. 79–95, Copper Mountain, CO, December, 1995.
- M. Pechura. 1982. “File archival techniques using data compression.” *Commun. ACM*, 25(9), 605–609, Sept. 1982.
- M. Peckerar, R. Fulton, P. Blaise, and D. Brown. 1979. “Radiation effects in MOS devices caused by X-ray and e-beam lithography,” *J. Vacuum Science Technology*, 16(6), 1658–1661, November–December 1979.
- M. C. Peckerar, C. M. Dozier, D. B. Brown, and D. Patterson. 1982. “Radiation effects introduced by X-ray lithography in MOS devices.” *IEEE Trans. Nuclear Science*, 29(6), 1697–1701, Dec. 1982.
- A. Peleg and U. Weiser. 1995. Dynamic Flow Instruction Cache Memory Organized around Trace Segments Independent of Virtual Address Line. US Patent No. 5,381,533, U.S. Patent Office.
- T. Pering and R. Brodersen. 1998. “The simulation and evaluation of dynamic voltage scaling algorithms.” In Proc. Int. Symp. on Low-Power Electronics and Design (ISLPED’98), June 1998.
- T. Pering, T. Burd, and R. Brodersen. 1998. “Dynamic voltage scaling and the design of a low-power microprocessor system.” In Power Driven Microarchitecture Workshop, attached to ISCA98, 1998.
- T. Pering, T. Burd, and R. Brodersen. 2000. “Voltage scheduling in the lpARM microprocessor system.” In Proc. Int. Symp. on Low-Power Electronics and Design (ISLPED’00), pp. 96–101, July 2000.
- K. Pettis and R. C. Hansen. 1990. “Profile guided code positioning.” In Proc. ACM SIGPLAN 1990 Conf. on Programming Language Design and Implementation (PLDI ’90), pp. 16–27; White Plains, New York, ACM Press, New York, 1990.
- P. J. Fleming and J. J. Wallace. 1986. “How not to lie with statistics: The correct way to summarize benchmark results.” *CACM*, 29(3), 218–221, March 1986.
- J. E. Pierce. 1995. “Cache behavior in the presence of speculative execution: the benefits of misprediction.” Doctoral Thesis. The University of Michigan.
- J. Pierce and T. Mudge. 1996. “Wrong-path instruction prefetching.” In Proc. 29th Ann. ACM/IEEE Int. Symp. on Microarchitecture Paris, France, December 02–04, 1996, pp. 165–175, Int. Symp. on Microarchitecture (MICRO), IEEE Computer Society, Washington, DC, 1996.
- E. Pinheiro, W.-D. Weber, and L. A. Barroso. 2007. “Failure trends in a large disk-drive population.” In Proc. Fifth USENIX Conf. on File and Storage Technologies (FAST 2007), San Jose, CA, February 2007.
- A. R. Pleszkun, J. R. Goodman, W.-C. Hsu, R. T. Joersz, G. Bier, P. Woest, and P. B. Schechter. 1987. “WISQ: A restartable architecture using queues.” In Proc. 14th Ann. Int. Symp. on Computer Architecture (ISCA-14), 1987.
- S. Podlipnig and L. Böszörményi. 2003. “A survey of Web cache replacement strategies.” *ACM Computing Surveys*, 35(4), 374–398, 2003.
- F. J. Pollack, K. C. Kahn, and R. M. Wilkinson. 1981. “The iMAX-432 object filing system.” In Proc. Eighth ACM Symp. on Operating Systems Principles (SOSP ’81), pp. 137–147, Pacific Grove, CA, December 14–16, 1981, ACM Press, New York, 1981.
- J. Pomerene, T. Puzak, R. Rechtschaffen, and F. Sparacio. 1989. Prefetching System for a Cache Having a Second Directory for Sequentially Accessed Blocks. US Patent 4,807,110. U.S. Patent office, February 1989, filed April 1984.
- M. A. Postiff and T. Mudge. 1999. Smart Register Files for High-Performance Microprocessors, Technical Report no. CSE-TR-403-99, University of Michigan.
- J. Poulton. 1999. “Signaling in High Performance Memory Systems,” Tutorial presented at ISSCC, San Francisco, CA, February 1999.
- M. Powell et al. 2000. “Gated-Vdd: A circuit technique to reduce leakage in deep-submicron cache memories,” in Proc. IEEE/ACM Int. Symp. on Low Power Electronics and Design (ISLPED), pp. 90–95, 2000.
- F. Prein. 2002. Personal communication.
- D. Pricer. 2002. Personal communication.
- B. Prince. 1997. *Semiconductor Memories, 2nd Ed.* John Wiley & Sons Ltd., New York, 1997.

- B. Prince. 1999. *High Performance Memories*. John Wiley & Sons Ltd., New York, 1999.
- B. Prince. 2000. *High Performance Memories*. John Wiley & Sons, West Sussex, England, 2000.
- S. Przybylski. 1990. *Cache and Memory Hierarchy Design: A Performance-Directed Approach*. Morgan Kaufmann, San Mateo, CA, 1990.
- S. Przybylski. 1996. *New DRAM Technologies: A Comprehensive Analysis of the New Architectures*. MicroDesign Resources, Sebastopol, CA, 1996.
- PTM. 2006. Predictive technology model. <http://www.eas.asu.edu/~ptm>
- W. Pugh. 1990. "Skip Lists: A probabilistic alternative to balanced trees." *Commun. ACM*, 33(6), June 1990.
- X. Qiu and M. Dubois. 1999. "Tolerating late memory traps in ILP processors." In Proc. 26th Ann. Int. Symp. on Computer Architecture (ISCA'99), pp. 76–87, Atlanta, GA, May 1999.
- S. Quinlan. 1991. "A cached WORM file system." *Software—Practice and Experience*, 21(12), 1289–1299, Dec. 1991.
- C. V. Ramamoorthy. 1965. "Analysis of computational systems: Discrete Markov analysis of computer programs." In Proc. 1965 20th Natl. Conf., pp. 386–392, Cleveland, Ohio, August 24–26, 1965, L. Winner, Ed., ACM Press, New York, 1965.
- C. V. Ramamoorthy. 1966. "The analytic design of a dynamic look ahead and program segmenting system for multiprogrammed computers." In Proc. 1966 21st Natl. Conf. ACM Press, New York, pp. 229–239, 1966.
- C. V. Ramamoorthy and K. M. Chandy. 1970. "Optimization of memory hierarchies in multiprogrammed systems." *J. ACM*, 17(3), 426–445, July 1970.
- Rambus. 1994. Rambus Memory: Enabling Technology for PC Graphics. Tech. Rep., Rambus Inc., Mountain View, CA, October 1994.
- Rambus. 1995. 64-Megabit Rambus DRAM Technology Directions. Tech. Rep., Rambus Inc., Mountain View, CA, September 1995.
- Rambus. 1996a. Comparing RDRAM and SGRAM for 3D Applications. Tech. Rep., Rambus Inc., Mountain View, CA, October 1996.
- Rambus. 1996b. Memory Latency Comparison. Tech. Rep., Rambus Inc., Mountain View, CA, September 1996.
- Rambus. 1998a. 16/18Mbit & 64/72Mbit Concurrent RDRAM Data Sheet. Rambus, <http://www.rambus.com/docs/Cnctds.pdf>.
- Rambus. 1998b. Direct RDRAM 64/72-Mbit Data Sheet. Rambus. <http://www.rambus.com/docs/64dDDS.pdf>.
- Rambus. 2000. Direct RDRAM 256/288-Mbit Data Sheet. Rambus. <http://www.rambus.com/developer/downloads/rdrdm.256s.0060-1.1.book.pdf>.
- A. Ramirez, L. A. Barroso, K. Gharachorloo, R. Cohn, J. Larriba-Pey, P. G. Lowney, and M. Valero. 2001. "Code layout optimizations for transaction processing workloads." In Proc. 28th Ann. Int. Symp. on Computer Architecture (ISCA '01), pp. 155–164, Göteborg, Sweden, June 30–July 04, 2001, ACM Press, New York, 2001.
- S. Ranade. 1991. *Mass Storage Technologies*. Meckler Publishing, Westport, CT, 1991.
- B. Randell and C. J. Kuehner. 1967. "Dynamic storage allocation systems." In Proc. First ACM Symp. on Operating System Principles (SOSP '67), pp. 9.1–9.16, J. Gosden and B. Randell, Eds., ACM Press, New York, 1967.
- P. Ranganathan et al. 1998. "Performance of database workloads on shared-memory systems with out-of-order processors." In Proc. Int. Conf. Architectural Support for Programming Languages and Operating Systems (ASPLOS-8), pp. 307–318, October 1998.
- R. M. Rao, J. L. Burns and R.B. Brown. (2003) "Circuit techniques for gate and subthreshold leakage minimization in future CMOS technologies," ESSCIRC '03. Proc. 29th European Solid-State Circuits Conf., 2003.
- R. Rashid, A. Tevanian, M. Young, D. Young, R. Baron, D. Black, W. Bolosky, and J. Chew. 1988. "Machine-independent virtual memory management for paged uniprocessor and multiprocessor architectures." *IEEE Trans. Computers*, 37(8), 896–908, 1988.
- E. S. Raymond. 1997. The On-line Hacker Jargon File, version 4.0.0. The MIT Press. <http://www.ccil.org/jargon/>.
- R. Rechtschaffen. 1983. "Cache miss history table." *IBM Technical Disclosure Bulletin*, 25(11B), 5978–5980, April 1983.
- S. L. Rege. 1976. "Cost, performance and size trade-offs for different levels in a memory hierarchy." *IEEE Computer*, 19, 43–51, April 1976.
- S. Reinhardt, M. Hill, J. Larus, A. Lebeck, J. Lewis, and D. Wood. 1993. "The Wisconsin Wind Tunnel: Virtual prototyping of parallel computers." In Proc. ACM

- SIGMETRICS Conf. on Measurement and Modeling of Computer Systems '93, 1993.
- G. Reinman and N. Jouppi. 2000. CACTI 2.0: An Integrated Cache Timing and Power Model, WRL Research Report 2000/7, Feb. 2000.
- P. J. Restle, J. W. Park, and B. F. Lloyd. 1992. "DRAM variable retention time." *In International. Electron Devices Meeting Technical Digest*, pp. 807–810, 1992.
- D. Rhoden. 2002. Personal communication.
- R. Riedlinger and T. Grutkowski. 2002. "The high-bandwidth 256 kB 2nd level cache on an Itanium microprocessor," In ISSCC, 2002.
- S. A. Ritchie. 1985. "TLB for Free: In-Cache Address Translation for a Multiprocessor Workstation," Technical Report UCB/CSD 85/233, University of California.
- J. A. Rivers and E. S. Davidson. 1996. "Reducing conflicts in direct-mapped Caches with a temporality based design." In Proc. 1996 Int. Conf. on Parallel Processing (ICPP 1996), Volume 1: Architecture, pp. 154–163, Bloomington, IL, August 1996.
- J. A. Rivers, E. S. Tam, G. S. Tyson, E. S. Davidson, and M. Farrens. 1998. "Utilizing reuse information in data cache management." In Proc. 12th Int. Conf. on Supercomputing (ICS '98), pp. 449–456. Melbourne, Australia, 1998.
- S. Rixner, W. Dally, U. Kapasi, P. Mattson, and J. Owens. 2000. "Memory access scheduling." In Proc. 27th Int. Symp. on Computer Architecture (ISCA), June 2000.
- S. Rixner. 2004. "Memory controller optimizations for Web servers." In Proc. 37th Int. Symp. on Microarchitecture (MICRO), December 2004.
- N. Robertson, H. Hu, and C. Tsang. 1997. "High performance write head using NiFe 45/55." *IEEE Trans. Magnetics*, 33(5), 2818–2820, 1997.
- T. Roscoe. 1994. "Linkage in the Nemesis single address space operating system." *ACM Operating Syst. Rev.*, 28(4), 48–55, 1994.
- T. Roscoe. 1995. The Structure of a Multi-Service Operating System, PhD thesis, Queens' College, University of Cambridge.
- M. Rosenblum, E. Bugnion, S. A. Herrod, E. Witchel, and A. Gupta. 1995. "The impact of architectural trends on operating system performance." In Proc. Fifteenth ACM Symp. on Operating Systems Principles (SOSP-15), December 1995.
- M. Rosenblum and J. K. Ousterhout. 1992. "The design and implementation of a log-structured file system." *ACM Transactions on Computer Systems*, 10(1), 26–52, 1992.
- E. Rotenberg, S. Bennett, and J. E. Smith. 1996. "Trace cache: A low latency approach to high bandwidth instruction fetching." In Proc. 29th Ann. ACM/IEEE Int. Symp. on Microarchitecture (MICRO-29), pp. 24–35, Paris, France, December 1996.
- A. Roth, A. Moshovos, and G. Sohi. 1998. "Dependence based prefetching for linked data structures." In The 8th Int. Conf. on Architectural Support for Programming Languages and Operating Systems (ASPLOS), pp. 115–126, October 1998.
- A. Roth and G. S. Sohi. 1999. "Effective jump-pointer prefetching for linked data structures." In Proc. 26th Int. Symp. on Computer Architecture (ISCA), Atlanta, GA, May 1999.
- K. Roy and M. C. Johnson. 1996. "Software design for low power." In NATO Advanced Study Institute on Low Power Design in Deep Submicron Electronics (ISGA), Ciocco, Lucca, Italy, August 1996.
- C. Ruemmler and J. Wilkes. 1994. "An introduction to disk drive modeling." *Computer*, 27(3), 17–28, 1994.
- J. Russell and M. Jacome. 1998. "Software power estimation and optimization for high performance, 32-bit embedded processors." In Int. Conf. on Computer Design (ICCD), Austin, TX, October 1998.
- K. Ryan. 2002. Personal communication.
- G. M. Sacco and M. Schkolnick. 1982. "A mechanism for managing the buffer pool in a relational database system using the hot set model." In Proc. 8th Int. Conf. on Very Large Data Bases, pp. 257–262, Mexico City, Mexico, September 1982.
- S. Sair and M. Charney. 2000. "Memory behavior of the SPEC 2000 Benchmark Suite." *IBM Research Report*, October, 2000.
- Samsung. 1998. FPM DRAM 4M x 16 Part No. KM416V4100C. Samsung Semiconductor. [http://www.usa.samsungsemi.com/products/prodspec/dramcomp/KM416V40\(1\)00C.PDF](http://www.usa.samsungsemi.com/products/prodspec/dramcomp/KM416V40(1)00C.PDF)
- K. Sasaki et al. 1988. "A 15-ns 1-Mbit CMOS SRAM." *IEEE J. Solid-State Circuits*, 23(5), 1067–1072, Oct. 1988.
- K. Sasaki et al. 1989. "A 9-ns 1-Mbit CMOS SRAM." *IEEE J. Solid-State Circuits*, 24(5), 1219–1225, Oct. 1989.

- K. Sasaki et al. 1990. "A 23-ns 4-Mb CMOS SRAM with 0.2-uA standby current." *IEEE J. Solid-State Circuits*, 25(5), 1075–1081, Oct. 1990.
- I. Sase et al. 1997. "Multimedia LSI accelerator with embedded DRAM." *IEEE Micro*, 17(6), 49–54, Nov. 1997.
- H. Sato et al. 1999. "A 500-MHz pipeline burst SRAM with improved SER immunity." *IEEE J. Solid-State Circuits*, SC-34(11), 1571–1579, Nov. 1999.
- A. Saulsbury, F. Pong, and A. Nowatzky. 1996. "Missing the memory wall: The case for processor/memory integration." In Proc. 23rd Ann. Int. Symp. on Computer Architecture (ISCA'96), pp. 90–101, Philadelphia, PA, May 1996.
- Y. Sazeides and J. E. Smith. 1997. "The predictability of data values." In Proc. 30th Ann. Int. Symp. on Microarchitecture (MICRO 1997), pp. 248–258, Research Triangle Park, NC, December 1997.
- C. Scheurich and M. Dubois. 1998. "Concurrent miss resolution in multiprocessor caches." In Proc. 1988 Int. Conf. on Parallel Processing, 1998.
- I. Schoinas, B. Falsafi, A. R. Lebeck, S. K. Reinhardt, J. R. Larus, and D. A. Wood. 1994. "Fine-grain access control for distributed shared memory." In Proc. Sixth Int. Conf. on Architecture Support for Programming Languages and Operating Systems (ASPLOS), pp. 297–306, 1994.
- M. D. Schroeder. 1971. "Performance of the GE-645 associative memory while Multics is in operation." In Proc. ACM SIGNOPS Workshop on System Performance Evaluation, pp. 227–245. Cambridge, MA, April 1971.
- D. M. Schuler and E. G. Ulrich. 1972. "Clustering and linear placement." In Proc. 9th Workshop on Design Automation (DAC '72), pp. 50–56, June 26–28, 1972, ACM Press, New York, 1972.
- R. C. Schumann. 1997. "Design of the 21174 memory controller for DIGITAL personal workstations." *Digital Technical J.*, 9(2), 57–70, 1997.
- S. Schuster et al. 1986. "A 15-ns CMOS 64K RAM." *IEEE J. Solid-State Circuits*, SC-21(5), 704–712, Oct. 1986.
- W. D. Schwaderer and A. W. Wilson, Jr. 1996. *Understanding I/O Subsystems*. Adaptec, Milpitas, CA, 1996.
- T. Schwarz and W. Burkhard. 1995. "Reliability and performance of RAID5." *IEEE Trans. Magnetics*, 31(2), 1161–1166, 1995.
- M. L. Scott, T. J. LeBlanc, and B. D. Marsh. 1988. "Design rationale for Psyche, a general-purpose multiprocessor operating system." In Proc. 1988 Int. Conf. on Parallel Processing, August 1988.
- J. Scott, L. Lee, A. Chin, J. Arends, and B. Moyer. 1999. "Designing the M.CORE M3 CPU architecture." In Int. Conf. on Computer Design, Austin, TX, October 1999.
- M. L. Seidl and B. G. Zorn. 1998. "Segregating heap objects by reference behavior and lifetime." In Proc. Eighth Int. Conf. on Architectural Support For Programming Languages and Operating Systems (ASPLOS-VIII), pp. 12–23, San Jose, CA, October 02–07, 1998, ACM Press, New York, 1998.
- M. Seltzer, P. Chen, and J. Ousterhout. 1990. "Disk scheduling revisited." In Winter USENIX 1990, pp. 313–324, Washington, DC, 1990.
- T. Semba, T. Hirano, J. Hong, and L. Fan. 1999. "Dual-stage servo controller for hdd using mems microactuator." *IEEE Trans. Magnetics*, 35(5), 2271–2273, 1999.
- S. M. Shahriar and J. C. Liu. 1997. "On the design of multiprogrammed caches for hard real-time systems." In Proc. IEEE Int. Performance, Computing and Communications Conference (IPCCC'97), pp. 17–25, February 1997.
- D. L. Shell. 1959. "The Share 709 System: A cooperative effort." *J. ACM (JACM)*, 6(2), 123–127, April 1959.
- T. Sherwood, S. Sair, and B. Calder. 2000. "Predictor-directed stream buffers." In The 33rd Int. Symp. on Microarchitecture (MICRO), pp. 42–53, December 2000.
- N. Shirle and D. Lieu. 1996. "History and trends in the development of motorized spindles for hard disk drives." *IEEE Trans. Magnetics*, 32(3), 1703–1708, 1996.
- W. Shiue and C. Chakrabarti. 1999. "Memory exploration for low power, embedded systems." In Proc. 36th ACM/IEEE Conf. on Design Automation (DAC '99), pp. 140–145, New Orleans, Louisiana, June 21–25, 1999, M. J. Irwin, Ed., ACM Press, New York, 1999.
- P. Shivakumar and N. Jouppi. 2001. CACTI 3.0: An Integrated Cache Timing, Power and Area Model, WRL Research Report 2001/2, Aug. 2001.
- B. Shriver and B. Smith. 1998. *The Anatomy of a High-Performance Microprocessor: A Systems Perspective*. IEEE Comput. Soc., Los Alamitos, CA, 1998.

- SIA. 2003. *Int. Technology Roadmap for Semiconductors 2003 Edition*. Semiconductor Industry Association. <http://public.itrs.net>.
- SIA. 2005. *Int. Technology Roadmap for Semiconductors 2005 Edition*. Semiconductor Industry Association. <http://public.itrs.net>.
- H. M. Sierra. 1990. *An Introduction to Direct Access Storage Devices*. Academic Press, San Diego, CA, 1990.
- SimOS. 1998. SimOS: The Complete Machine Simulator. Stanford University. <http://simos.stanford.edu/>.
- R. L. Sites, Editor. 1992. *Alpha Architecture Reference Manual*. Digital Equipment Corporation, Maynard, MA.
- R. Sites. 1996. "It's the memory, stupid!" *Microprocessor Rep.*, 10(10), Aug. 1996.
- J. Sjodin, B. Froderberg, and T. Lindgren. 1998. "Allocation of global data objects in on-chip RAM." *Compiler and Architecture Support for Embedded Computing Systems (CASES '98)*, December 1998.
- J. Sjodin and C. Von Platen. 2001. "Storage allocation for embedded processors." *Compiler and Architecture Support for Embedded Computing Systems (CASES)*, November 2001.
- M. Slater. 1994. "AMD's K5 designed to outrun Pentium." *Microprocessor Rep.*, 8(14), Oct. 1994.
- SLDRAM. 1998. 4M x 18 SLDRAM Advance Datasheet. SLDRAM, Inc. <http://www.sldram.com/Documents/corp400b.pdf>.
- A. J. Smith. 1977. "Two methods for the efficient analysis of memory address trace data." *IEEE Trans. Software Eng.*, 3(1), 94–101, Jan. 1977.
- A. J. Smith. 1981a. "Long term file migration: Development and evaluation of algorithms." *Commun. ACM*, 24(8), 521–532, Aug. 1981.
- J. E. Smith. 1981. "A study of branch prediction strategies." In *Proc. 8th Ann. Symp. on Computer Architecture (ISCA-8)*, pp. 135–148, Minneapolis, MN, May 1981.
- A. J. Smith. 1982. "Cache memories." *Computing Surveys*, 14(3), 473–530, Sept. 1982.
- A. J. Smith, 1985a. "Disk cache: Miss ratio analysis and design considerations." In *Proc. 5th Ann. Symp. on Computer Architecture*, pp. 242–248, April 1985.
- A. J. Smith. 1985b. "Disk cache-miss ratio analysis and design considerations." *ACM Trans. Comput. Syst.*, 3(3), 161–203, Aug. 1985.
- J. E. Smith and A. R. Pleszkun. 1985. "Implementation of precise interrupts in pipelined processors." In *Proc. 12th Ann. Int. Symp. on Computer Architecture (ISCA'85)*, pp. 36–44, Boston, MA, June 1985.
- J. E. Smith. 1988. "Characterizing computer performance with a single number." *CACM*, 31(10), 1202–1206, Oct. 1988.
- J. E. Smith, G. E. Dermer, and M. A. Goldsmith. 1988. *Computer System Employing Virtual Memory*. US Patent No. 4,774,659. U.S. Patent Office.
- J. E. Smith and A. R. Pleszkun. 1988. "Implementing precise interrupts in pipelined processors." *IEEE Trans. Computers*, 37(5), 1988.
- M. J. Smith. 1997. *Application-Specific Integrated Circuits*. Addison-Wesley, Reading, MA, 1997.
- G. S. Sohi and S. Vajapeyam. 1987. "Instruction issue logic for high-performance, interruptable pipelined processors." In *Proc. 14th Ann. Int. Symp. on Computer Architecture (ISCA'87)*, June 1987.
- Y. Solihin, J. Lee, and J. Torrellas. 2002. "Using a user-level memory thread for correlation prefetching." In *29th Int. Symp. on Computer Architecture (ISCA)*, May 2002.
- Y. Solihin, J. Lee, and J. Torrellas. 2003. "Correlation prefetching with a user-level memory thread." *IEEE Trans. Parallel Distributed Systems*, June 2003.
- J. A. Solworth and C. U. Orji. 1990. "Write-only disk caches." In *Proc. 1990 ACM SIGMOD Int. Conf. on Management of Data (SIGMOD '90)*, pp. 123–132, Atlantic City, New Jersey, May 23–26, 1990, SIGMOD '90. ACM Press, New York, 1990.
- S. W. Son and M. Kandemir. 2006. "Energy-aware data prefetching for multi-speed disks." In *Proc. 3rd Conf. on Computing Frontiers (CF '06)*, pp. 105–114, Ischia, Italy, May 03–05, 2006, ACM Press, New York, 2006.
- S. Srinivasan, V. Cuppu, and B. Jacob. 2001. "Transparent data-memory organizations for digital signal processors." In *Proc. Int. Conf. on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2001)*, pp. 44–48, Atlanta, GA, Nov. 2001.
- A. Srivastava and A. Eustace. 1994. *ATOM: A System for Building Customized Program Analysis Tools*.

- Technical Report WRL-RR-94/2, DEC Western Research Laboratory.
- Staktek. 2006. Personal communication.
- J. W. Stamos. 1984. "Static grouping of small objects to enhance performance of a paged virtual memory." *ACM Trans. Comput. Syst.*, 2(2), 155–180, May 1984.
- Standard Performance Evaluation Corp. 1993. SPEC Newsletter, December 1993.
- B. Steensgaard. 1996. "Points-to analysis in almost linear time." In *Symp. on Principles of Programming Languages (POPL)*, St. Petersburg Beach, FL, January 1996.
- S. Steinke, L. Wehmeyer, B. Lee, and P. Marwedel. 2002a. "Assigning program and data objects to scratchpad for energy reduction." In *Proc. of the Conf. on Design, Automation and Test in Europe (DATE)*, p. 409, IEEE Comput. Soc., Los Alamitos, CA, 2002.
- S. Steinke, N. Grunwald, L. Wehmeyer, R. Banakar, M. Balakrishnan, and P. Marwedel. 2002b. "Reducing energy consumption by dynamic copying of instructions onto onchip memory." In *Proc. 15th Int. Symp. on System Synthesis (ISSS '02)*, pp. 213–218, Kyoto, Japan, October 02–04, 2002, ACM Press, New York, 2002.
- L. D. Stevens. 1981. "The evolution of magnetic storage." *IBM J. Res. Dev.* 25(5), 663–675, 1981.
- L. Stevens. 1998. "Data storage on magnetic disks." In E. Daniel, C. Mee, and M. Clark, Editors, *Magnetic Recording: The First 100 years*. IEEE Press, New York, 1988.
- H. S. Stone. 1993. *High Performance Computer Architecture*. Addison-Wesley, Reading, MA, 1993.
- M. Stonebreaker. 1981. "Operating system support for database management." *Commun. ACM*, 24(7), 412–418, July 1981.
- A. Stoutchinin, J. N. Amaral, G. R. Gao, J. C. Dehnert, S. Jain, and A. Douillet. 2001. "Speculative pointer prefetching of induction pointers." In *Compiler Construction 2001, European Joint Conferences on Theory and Practice of Software*, Genova, Italy, April 2001.
- STREAM. 1997. STREAM: Measuring Sustainable Memory Bandwidth in High Performance Computers. The University of Virginia. <http://www.cs.virginia.edu/stream/>.
- C. Su and A. M. Despain. 1995. "Cache design trade-offs for power and performance optimization: A case study." In *Proc. 1995 Int. Symp. on Low Power Design (ISLPED '95)*, pp. 63–68, Dana Point, California, April 23–26, 1995, ACM Press, New York, 1995.
- Sun. 1995. The UltraSPARC Processor. Sun Technology, November 1995. White Paper.
- Sun. 1997. Wabi 2.2 Product Overview. Sun Microsystems. <http://www.sun.com/solaris/products/wabi/>.
- H. Sussman. 2002. Personal communication.
- I. E. Sutherland and R. F. Sproull. 1991. "Logical effort: Designing for speed on the back of an envelope." *Advanced Res. VLSI*, 1–16, 1991.
- I. E. Sutherland et al. 1999. *Logical Effort: Designing Fast CMOS Circuits, 1st Ed.*, Morgan Kaufman, San Mateo, CA, 1999.
- S. Suzuki and S. Iwasaki. 1982. "Magnetization transitions in perpendicular magnetic recording." *IEEE Trans. Magnetics*, 18(2), 771–769, 1982.
- M. Swanson, L. Stoller, and J. Carter. 1998. "Increasing TLB reach using superpages. backed by shadow memory." In *Proc. 25th Ann. Int. Symp. on Computer Architecture (ISCA'98)*, pp. 204–213, Barcelona, Spain, June 1998.
- Synopsys. 2002. DesignWare DW8051 MacroCell Databook. Synopsys, December 2002.
- Systems Performance Evaluation Cooperative. SPEC Benchmarks. <http://www.spec.org>.
- C. D. Tait and D. Duchamp. 1991. "Detection and exploitation of file working sets." In *11th Int. Conf. on Distributed Computing Systems (Cat. No. 91CH2996-7)*, pp. 2–9, 20–24, Arlington, TX, IEEE, Press, New York, May 1991.
- M. Talluri, S. Kong, M. D. Hill, and D. A. Patterson. 1992. "Tradeoffs in supporting two page sizes." In *Proc. 19th Ann. Int. Symp. on Computer Architecture (ISCA-19)*, 1992.
- M. Talluri and M. D. Hill. 1994a. "Surpassing the TLB performance of Superpages with less operating system support." In *Proc. Sixth Int. Conf. on Architectural Support for Programming Languages and Operating Systems (ASPLOS-6)*, San Jose, CA, 1994.
- M. Talluri and M. D. Hill. 1994b. "Surpassing the TLB performance of superpages. with less operating system support." In *Proc. Sixth Int. Conf. on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 1994.

- M. Talluri, M. D. Hill, and Y. A. Khalidi. 1995. "A new page table for 64-bit address spaces." In Proc. Fifteenth ACM Symp. on Operating Systems Principles (SOSP-15). December 1995.
- Y. Tan and V. Mooney. 2003. "A prioritized cache for multi-tasking real-time systems." In Proc. 11th Workshop on Synthesis and System Integration of Mixed Information technologies (SASIMI), pp. 168–175, April 2003.
- Y. Taur and T. Ning. 1998. *Fundamentals of Modern VLSI Devices*. Cambridge University Press, Cambridge, England, 1998.
- G. Taylor, P. Davies, and M. Farmwald. 1990. "The TLB slice—A low-cost high-speed address translation mechanism." In Proc. 17th Ann. Int. Symp. on Computer Architecture (ISCA '90), pp. 355–363, Seattle, Washington, May 28–31, 1990, ACM Press, New York, 1990.
- TechReport. 2006. The Tech Report. <http://techreport.com/cpu/>.
- Texas Instruments. TMS320C6000 peripherals reference guide, TI Inc. <http://www-s.ti.com/sc/psheets/spru190d/spru190d.pdf>.
- A. Thomasian and M. Blaum. 2006. "Mirrored disk organization reliability analysis." *IEEE Trans. Computers*, 55(12), 1640–1644, 2006.
- A. Thomasian and C. Liu. 2002. "Disk scheduling policies with lookahead." *ACM SIGMETRICS Performance Evaluation Rev.*, 30(2), 31–40, 2002.
- A. Thomasian. 2006. "Multi-level RAID for very large disk arrays." *ACM SIGMETRICS Performance Rev. — SPECIAL ISSUE: Design Implementation and Performance of Storage Systems*, 33(4), 17–22, 2006.
- J. E. Thornton. 1970. *Design of a Computer: The Control Data 6600*. Scott, Foresman and Co., Glenview, IL, 1970.
- V. Tiwari, S. Malik, and A. Wolfe. 1994. "Power analysis of embedded software: A first step towards software power minimization." *IEEE Trans. VLSI Syst.*, 2(4), 1277–1284, Dec. 1994.
- V. Tiwari and M. T.-C. Lee. 1998. "Power analysis of a 32-bit embedded microcontroller." *VLSI Design J.*, 7(3), 1998.
- R. M. Tomasulo. 1967. "An efficient algorithm for exploiting multiple arithmetic units." *IBM J. Res. Dev.*, 11(1), 25–33, 1967.
- H. C. Torng and M. Day. 1993. "Interrupt handling for out-of-order execution processors." *IEEE Trans. Computers*, 42(1), 122–127, Jan. 1993.
- J. Torrellas, A. Gupta, and J. Hennessy. 1992. "Characterizing the caching and synchronization performance of a multiprocessor operating system." In Proc. Fifth Int. Conf. on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 1992.
- J. D. Touch and D. J. Farber. 1994. "An experiment in latency reduction." In Proc. IEEE Infocom, pp. 175–181, Toronto, June 1994.
- C. Tsang, R. Fontana, T. Lin, D. Heim, V. Speriosu, B. Gurney, and M. Williams. 1994. "Design fabrication and testing of spin-valve read heads for high density recording." *IEEE Trans. Magnetics*, 24(6), 3801–3806, 1994.
- C. Tsang, M. Chen, T. Yogi, and K. Ju. 1997. "Gigabit density recording using dual-element mr/inductive heads on thin-film disks." *IEEE Trans. Magnetics*, 26(5), 2271–2276, 1997.
- J. L. Turley. 1995. "Thumb squeezes ARM code size." *Microprocessor Rep.*, 9(4), 1–5, March 27, 1995.
- J. Turley. 1997a. "M.Core shrinks code, power budgets." *Microprocessor Rep.*, 11(14), 12–15, Oct. 1997.
- J. Turley. 1997b. "TI's new 'C6x DSP screams at 1,600 MIPS." *Microprocessor Rep.*, 11(2), 14–18, 1997.
- J. Turley. 1998a. "MCore: Does Motorola need another processor family?" *Embedded Systems Programming*, July 1998.
- J. Turley. 1998b. "M.Core for the portable millenium." *Microprocessor Rep.*, 12(2), 15–18, Feb. 1998.
- J. Turley. 1998c. "National kills in-house embedded x86 work." *Microprocessor Rep.*, 12(2), 10, Feb. 1998.
- G. Tyson, M. Farrens, J. Matthews, and A. R. Pleszkun. 1995. "A modified approach to data cache management." In Proc. 28th Ann. Int. Symp. on Microarchitecture (MICRO-28), pp. 93–103, Ann Arbor, MI, 1995.
- S.-Y. Tzou and D. P. Anderson. 1991. "The performance of message-passing using restricted virtual memory remapping." *Software—Practice and Experience*, 21(3), 251–267, 1991.
- K. Uchiyama et al. 1991. "Design of a second-level cache chip for shared-bus multimicroprocessor systems." *IEEE J. Solid-State Circuits*, 26(4), 566–571, Apr. 1991.
- S. Udayakumaran and R. Barua. 2003. "Compiler-decided dynamic memory allocation for scratchpad based embedded systems." In Proc. Int. Conf. on Compilers, Architectures and Synthesis for Embedded Systems (CASES), pp. 276–286, ACM Press, New York, 2003.

- S. Ueno, T. Yamashita, H. Oda, S. Komori, Y. Inoue, and T. Nishimura. 1998. "Leakage current observation on irregular local Pn junction forming the tail distribution of DRAM retention time characteristics." In International Electron Devices Meeting Technical Digest (IEDM), pp. 153–156, 1998.
- R. Uhlig, D. Nagle, T. Mudge, and S. Sechrest. 1994. "Trap-driven simulation with Tapeworm-II." In Proc. Sixth Int. Conf. on Architectural Support for Programming Languages and Operating Systems (ASPLOS-6), San Jose, CA, 1994.
- O. S. Unsal, R. Ashok, I. Koren, C. M. Krishna, and C. A. Moritz. 1990. "Coolcache for hot multimedia." In Proc. Int. Symp. on Microarchitecture (MICRO), pp. 274–283, 1990.
- M. Upton. 1997. Personal communication.
- A. Vahdat, A. Lebeck, and C. Ellis. 2000. "Every joule is precious: The case for revisiting operating system design for energy efficiency." In SIGOPS European Workshop, Kolding, Denmark, September 2000.
- A. Varma and Q. Jacobson. 1998. "Destage algorithms for disk arrays with nonvolatile caches." *IEEE Trans. Comput.* 47(2), 228–235, Feb. 1998.
- A. Varma, B. Ganesh, M. Sen, S. R. Choudhary, L. Srinivasan, and B. Jacob. 2003. "A control-theoretic approach to dynamic voltage scaling." In Proc. Int. Conf. on Compilers, Architectures, and Synthesis for Embedded Systems (CASES 2003), pp. 255–266, San Jose, CA, October 2003.
- R. K. Venkatesan, S. Herr, and E. Rotenberg. 2006. "Retention-aware placement in DRAM (RAPID): Software methods for quasi-non-volatile DRAM." In Proc. 12th Int. Symp. on High Performance Computer Architecture (HPCA), pp. 157–167, 2006.
- M. Verma, L. Wehmeyer, and P. Marwedel. 2004. "Cache-aware scratchpad allocation algorithm." In Proc. Conf. on Design, Automation and Test in Europe (DATE), IEEE Comput. Soc., Los Alamitos, CA, 2004.
- N. Vijaykrishnan, M. Kandemir, M. Irwin, H. Kim, and W. Ye. 2000. "Energy-driven integrated hardware-software optimizations using simplepower." In Proc. 27th Ann. Int. Symp. on Computer Architecture (ISCA'00), pp. 95–116, Vancouver, BC, June 2000.
- M. A. Viredaz and D. A. Wallach. 2003. "Power evaluation of a handheld computer." *IEEE Micro*, 23(1), 66–74, Jan./Feb. 2003.
- F. Vivien and M. Rinard. 2001. "Incrementalized pointer and escape analysis." In Proc. ACM SIGPLAN 2001 Conf. on Programming Language Design and Implementation (PLDI), pp. 35–46, ACM Press, New York, 2001.
- P. Vogt. 2004a. "Fully buffered DIMM (FB-DIMM) server memory architecture: Capacity, performance, reliability, and longevity." Intel Developer Forum, Session OSAS008, February 2004.
- P. Vogt. 2004b. "Fully buffered DIMM (FB-DIMM) Architecture." Denali MemCon, Westford, MA, May 2004.
- R. Wahbe, S. Lucco, T. E. Anderson, and S. L. Graham. 1993. "Efficient software-based fault isolation." In Proc. Fourteenth ACM Symp. on Operating Systems Principles (SOSP-14), pp. 203–216, 1993.
- W. Walker and H. G. Cragon. 1995. "Interrupt processing in concurrent processors." *IEEE Computer*, 28(6), June 1995.
- A. Walker. 2002. Personal communication.
- W.-H. Wang, J.-L. Baer, and H. M. Levy. 1989. "Organization and performance of a two-level virtual-real cache hierarchy." In Proc. 16th Ann. Int. Symp. on Computer Architecture (ISCA-16), pp. 140–148, 1989.
- S. X. Wang and A. M. Taratorin. 1999. *Magnetic Information Storage Technology*. Academic Press, San Diego, CA, 1999.
- D. Wang, B. Ganesh, N. Tuaycharoen, K. Baynes, A. Jaleel, and B. Jacob. 2005. "DRAMsim: A memory-system simulator." *SIGARCH Computer Architecture News*, 33(4), 100–107. Sept. 2005.
- D. L. Weaver and T. Germand, Editors. 1994. *The SPARC Architecture Manual Version 9*. PTR Prentice Hall, Englewood Cliffs, NJ, 1994.
- C. F. Webb. 1988. "Subroutine call/return stack." *IBM Technical Disclosure Bulletin*, 30(11), April 1988.
- L. R. Wechsler. 1973. "The effect of look-ahead paging in a virtual memory system as determined by simulation." In Proc. 1st Symp. on Simulation of Computer Systems, pp. 234–241, (Gaithersburg, Maryland, June 19–20, 1973, H. J. Highland, Ed., Ann. Simulation Symposium. IEEE Press, Piscataway, NJ, 1973.
- L. Wehmeyer, U. Helmig, and P. Marwedel. 2004. "Compiler-optimized usage of partitioned memories." In Proc.

- 3rd Workshop on Memory Performance Issues (WMPI2004), 2004.
- M. Weiser, B. Welch, A. Demers, and S. Shenker. 1994. "Scheduling for reduced CPU energy." In Proc. First USENIX Symp. on Operating Systems Design and Implementation (OSDI'94), pp. 13–23, Monterey, CA, November 1994.
- S. Weiss and J. E. Smith. 1984. "Instruction issue login in pipelined supercomputers." *IEEE Trans. Computers*, 33(11), 1984.
- S. Weiss and J. E. Smith. 1994. *POWER and PowerPC*. Morgan Kaufmann, San Francisco, CA, 1994.
- D. Weiss, J. J. Wu, and V. Chin. 2002. "An on-chip 3MB subarray-based 3rd level cache on an Itanium microprocessor." In Proc. Int'l. Solid-State Circuits Conference (ISSCC) 2002.
- T. A. Welch. 1978. "Memory hierarchy configuration analysis." *IEEE Trans. Computers*, 27(5), 408–413, May 1978.
- M. Wells. 1972. "File compression using variable length encodings." *The Computer J.*, 15(4), 308–313, Nov. 1972.
- B. Wheeler and B. N. Bershad. 1992. "Consistency management for virtually indexed caches." In Proc. Fifth Int. Conf. on Architectural Support for Programming Languages and Operating Systems (ASPLOS-5), pp. 124–136, October 1992.
- M. White, P. Hingwe, and T. Hirano. 2004. "Comparison of a mems microactuator and a pzt milliactuator for high-bandwidth hdd servo." In American Control Conference 2004, pp. 541–546, Boston, MA, 2004.
- K. Wilcox and S. Manne. 2001. "Alpha Processors: A History of Power Issues and A Look to the Future." Compaq Computer Corporation, 2001.
- M. V. Wilkes. 1965. "Slave memories and dynamic storage allocation." *IEEE Trans. Electronic Computers (Short Notes)*, EC-14, 270–271, April 1965.
- M. V. Wilkes. 1971. "Slave memories and segmentation." *IEEE Trans. Computers (Short Notes)*, C-20(6), 674–675, June 1971.
- R. Williams. 1997. *Data Powers of Ten*. Center for Advanced Computing Research, Caltech, Pasadena CA. <http://www.cacr.caltech.edu/roy/dataquan/>.
- S. Williams, M. Abrams, C. R. Standridge, G. Abdulla, and E. A. Fox. 1996. "Removal policies in network caches for World-Wide Web documents." In Proc. ACM SIGCOMM '96 Conf. on Applications, Technologies, Architectures, and Protocols for Computer Communications, pp. 293–305, Stanford, CA, August 1996.
- R. Wilson. 1997. "MoSys tries synthetic SRAM." *EE Times Online*, July 15, 1997. <http://www.eetimes.com/news/98/1017news/tries.html>.
- K. M. Wilson, K. Olukotun, and M. Rosenblum. 1996. "Increasing cache port efficiency for dynamic superscalar microprocessors." In Proc. 23rd Ann. Int. Symp. on Computer Architecture (ISCA '96), pp. 147–157, Philadelphia, Pennsylvania, May 22–24, 1996, ACM Press, New York, 1996.
- P. R. Wilson. 1991. "Pointer swizzling at page fault time: Efficiently supporting huge address spaces on standard hardware." *ACM Computer Architecture News*, June, 6–13, 1991.
- S. Wilton and N. Jouppi. 1994. An Enhanced Access and Cycle Time Model for On-chip Caches, WRL Research Report 93/5, DEC Western Research Laboratory, 1994.
- S. J. Wilton and N. P. Jouppi. 1996. "CACTI: An enhanced cache access and cycle time model." *IEEE JSSC*, 31(5), May 1996.
- M. S. Wojtyna and P. A. de Maine. 1988. "SOLID: A high-speed data- and question-independent information management system." In Proc. 1988 ACM Sixteenth Ann. Conf. Computer Science (CSC '88), PP. 652–657, Atlanta, Georgia, ACM Press, New York, 1988.
- M. E. Wolf and M. S. Lam. 1991. "A data locality optimizing algorithm." In Proc. SIGPLAN Conf. on Programming Language Design and Implementation (PLDI), ACM, New York, June 1991.
- O. Wolf and J. Bier. 1998. "StarCore launches first architecture: Lucent and Motorola disclose new VLIW-based approach." *Microprocessor Rep.*, 12(14), 22–55, 1998.
- A. Wolfe and A. Chanin. 1992. "Executing compressed programs on an embedded RISC architecture." In Proc. 25th Ann. Int. Symp. on Microarchitecture (MICRO 1992), pp. 81–91, Portland, OR, December 1992.
- M. Wolfe. 2005. "How compilers and tools differ for embedded systems." Keynote address, International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2005), San Francisco, CA, September 2005.
- D. A. Wood, S. J. Eggers, G. Gibson, M. D. Hill, J. M. Pendleton, S. A. Ritchie, G. S. Taylor, R. H. Katz,

- and D. A. Patterson. 1986. "An in-cache address translation mechanism." In Proc. 13th Ann. Int. Symp. on Computer Architecture (ISCA-13), 1986.
- D. A. Wood. 1990. "The design and evaluation of in-cache address translation." PhD thesis, University of California at Berkeley, 1990.
- B. Worthington, G. Ganger, and Y. Patt. 1994. "Scheduling algorithms for modern disk drives." In Proc. 1994 ACM SIGMETRICS Joint Int. Conf. on Measurement and Modeling of Computer Systems, pp. 241–251, Nashville, TN, 1994.
- B. Worthington, G. Ganger, Y. Patt, and J. Wilkes. 1995. "On-line extraction of SCSI disk drive parameters." In Proc. 1995 ACM SIGMETRICS Joint Int. Conf. on Measurement and Modeling of Computer systems, pp. 146–156, Ottawa, Canada, 1995.
- W. A. Wulf and S. A. McKee. 1995. "Hitting the memory wall: Implications of the obvious." *ACM Computer Architecture News*, 23(1), pp. 20–24, March 1995.
- S. Wuytack, J. Diguët, F. V. Catthoor, and H. J. De Man. 1998. "Formalized methodology for data reuse exploration for low-power hierarchical memory mappings." *IEEE Trans. Very Large Scale Integr. Syst.*, 6(4), 529–537, Dec. 1998.
- D. S. Yaney, C. Y. Lu, R. A. Kohler, M. J. Kelly, and J. T. Nelson. 1987. "A Meta-Stable Leakage Phenomenon in DRAM Charge Storage—Variable Hold Time." In International. Electron Devices Meeting Technical Digest (IEDM), pp. 336–338, 1987.
- C.-L. Yang and A. R. Lebeck. 2000. "Push vs. pull: Data movement for linked data structures." In Int. Conf. on Supercomputing, pp. 176–186, May 2000.
- Y. Ye, S. Borkar and V. De. 1998. "A new technique for standby leakage reduction in high-performance circuits." In Symp. on VLSI Circuits Dig. Tech. Papers, 1998.
- K. C. Yeager. 1996. "The MIPS R10000 superscalar microprocessor." *IEEE Micro*, 16(2), 28–40, April 1996.
- T.-Y. Yeh and Y. N. Patt. 1991. "Two-level adaptive training branch prediction." In Proc. 24th Ann. Int. Symp. Microarchitecture (MICRO-24), pp. 51–61. 1991. DOI= <http://doi.acm.org/10.1145/123465.123475>
- T. Yeh and Y. N. Patt. 1992. "Alternative implementations of two-level adaptive branch prediction." In Proc. 19th Ann. Int. Symp. Computer Architecture (ISCA '92), pp. 124–134. Queensland, Australia, May 19–21, 1992, ACM Press, New York, 1992.
- T. Yeh, D. T. Marr, and Y. N. Patt. 1993. "Increasing the instruction fetch rate via multiple branch prediction and a branch address cache." In Proc. 7th Int. Conf. on Supercomputing (ICS), pp. 67–76, Tokyo, Japan, July 1993.
- Y. C. Yeo et al. 2000. "Direct tunneling gate leakage current in transistors with ultrathin silicon nitride gate dielectric." *IEEE Electron Device Letters*, Nov. 2000.
- M. Yoshimoto et al. 1983. "A divided word-line structure in the static RAM and its application to a 64K full CMOS RAM," *IEEE J. Solid-State Circuits*, SC-18(5), 479–485, Oct. 1983.
- S. Zarandioon and A. Thomasian. 2006. "Optimization of online disk scheduling algorithms." ACM SIGMETRICS Performance Evaluation Review - SPECIAL ISSUE: Design implementation and performance of storage systems, 33(4), 42–46, 2006.
- M. J. Zekauskas, W. A. Sawdon, and B. N. Bershad. 1994. Software Write Detection for a Distributed Shared Memory, Proceedings of the First Symposium on Operating Systems Design and Implementation (OSDI), 1994.
- Z. Zhang and J. Torrellas. 1995. "Speeding up irregular applications in shared-memory multiprocessors: Memory binding and group prefetching." In 22nd Int. Symp. Computer Architecture (ISCA), pp. 188–199, June 1995.
- C. Zhang and S. McKee. 2000. "Hardware-only stream prefetching and dynamic access ordering." In Proc. 14th Int. Conf. on Supercomputing, 2000.
- Z. Zhang, Z. Zhu, and X. Zhang, 2000. "A permutation-based page interleaving scheme to reduce row-buffer conflicts and exploit data locality." In Proc. 33rd IEEE/ACM Int. Symp. on Microarchitecture (MICRO), pp. 32–41, Dec. 2000.
- L. Zhang, Z. Fang, M. Parker, B. Mathew, L. Schaelicke, J. Carter, W. Hsieh, and S. McKee. 2001. "The impulse memory controller." *IEEE Trans. Computers* 50(11), Nov. 2001.
- T. Zhang. 2001. "RTOS performance and energy consumption analysis based on an embedded system testbed." Master's thesis, University of Maryland at College Park, May 2001.
- Z. Zhang, Z. Zhu, and X. Zhang. 2002a. "Breaking address mapping symmetry at multi-levels of memory

- hierarchy to reduce DRAM row-buffer conflicts." *The J. Instruction-Level Parallelism*, 3, 2002.
- Y. Zhu and Y. Hu. 2002. "Can large disk built-in caches really improve system performance?" In Proc. ACM SIGMETRICS 2002 (extended abstract), pp. 284–285, Marina Del Rey, CA, June 15–19, 2002.
- Z. Zhu, Z. Zhang, and X. Zhang. 2002. "Fine-grain priority scheduling on multi-channel memory systems." In Proc. 8th Int. Symp. on High Performance Computer Architecture (HPCA), February 2002.
- Z. Zhu and Z. Zhang. 2005. "A performance comparison of DRAM memory system optimizations for SMT processors." In Proc. 11th Int. Symp. High-Performance Computer Architecture (HPCA), February 2005.
- J. Ziegler et al. 1998. "IBM experiments in soft fails in computer electronics." *IBM J. Res. Dev.*, 40(1), 1998.