Efficient Far-Field Radio Frequency Energy Harvesting for Passively Powered Sensor Networks

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***Abstract*—An RF-DC power conversion system is designed to efficiently convert far-field RF energy to DC voltages at very low received power and voltages. Passive rectifier circuits are designed in a 0.25 μm CMOS technology using floating gate transistors as rectifying diodes. The 36-stage rectifier can rectify input voltages as low as 50 mV with a voltage gain of 6.4 and operates with received power as low as 5.5 μW (−22.6 dBm). Optimized for far field, the circuit operates at a distance of 44 m from a 4 W EIRP source. The high voltage range achieved at low load current make it ideal for use in passively powered sensor networks.**

***Index Terms*—Far field, floating gate, high efficiency, interface circuit, micro power, passively powered, power conversion, RF powered, rectifier, sensor network.**

I. Introduction

PASSIVELY powered devices are becoming increasingly important for a wide range of sensing applications. Also known as remotely powered devices, passively powered devices do not require any internal power source while extracting their power from propagating radio waves, sunlight, mechanical vibration [1], thermal gradients, convection flows or other forms of harvestable energy. One of the most popular power extraction methods for passively powered devices is to harvest power from propagating radio frequency (RF) signals [2].

RF powered devices are often used in applications such as structural monitoring where the RF powered devices are embedded into a structure making battery replacement impossible without destroying the structure. Some applications employing RF powered devices require deployment of these devices in very large numbers thus, making individual node battery replacement impractical.

RF powered devices are often part of telemetry systems to remotely measure and report data back to a central processing unit [3]–[6]. Devices powered by propagating RF waves are most often used in passive radio frequency identification (RFID) or passive RF tags to replace the bar code as a new form of data collection [2], [7]. Passive RFID tags are typically used in the range of 1–3 meters. Many modern biomedical implants are passively powered with radio waves to prolong the lifetime of the implanted device, and to reduce the chances of infection and chemical instability from the use of batteries [8], [9]. Bionic implants generally operate within close proximity of the base station (typically 1–50 cm) and must be robustly designed since there is little tolerance for error in implanted devices. RF powered devices are also used in ultra-low-power sensor networks in remote areas to eliminate the use of batteries in the sensor system and to keep the sensor network free of maintenance [10], [11]. The applications for these sensor networks normally require an operating distance of 3 to 100 meters and they usually have a backup battery in case the power provided by the RF radiation is insufficient. Other applications for RF powered devices include access control, equipment monitoring and even personal identification.

In all of these applications, there must be a power conversion circuit that can extract enough DC power from the incident electromagnetic waves for the passive device to operate. Previously reported far field RF powered devices generally operate from distances of less than 10 meter from the RF source due to the high power loss from RF wave propagation at UHF frequencies [12]. Others previous work achieved sufficient power but provides low output voltage with higher load current making it inadequate for use in passively powered wireless sensor networks [13]. A highly efficient passive power conversion circuit is needed for long distance passive sensing in distributed sensor networks.

In a far field RF energy harvesting system, RF energy must be extracted from the air at very low power density since the propagation energy drops off rapidly as distance from the source is increased [14]. In free space, the electric field and power density drop off at the rate of $1/d^2$, where d is the distance from the radiating source. The available power to the receiver decreases by 6 dB for every doubling of distance from the transmitter. With multi-path fading, the power density drops off at a much faster rate than $1/d^2$, it is therefore critical that the power conversion circuit operate at very low receive power to achieve longer operating distance. Rectification circuits for such systems must be optimized to improve on the minimum power-threshold it takes for the system to operate. To overcome this power-threshold, the system requires significantly more efficient circuit and system level design [15].

One of the major challenges to achieving this goal is the relatively high voltage requirement of rectifying circuits currently employed [16]–[18]. When the available RF power to the receiver is under 100 μW, the available voltage for rectification in the RF to DC conversion system falls below 0.3 V, much too low to overcome the threshold voltage $(V_{\rm th})$ of conventional rectifier circuits. Alternative solutions must be found to circumvent or diminish the "dead-zone" in voltage rectification and otherwise reduce the effective threshold voltage in standard CMOS rectifier designs.

This paper describes highly sensitive and efficient rectifier circuit techniques as well as system level design issues for RF to DC power conversion. Fully passive rectifier circuits are

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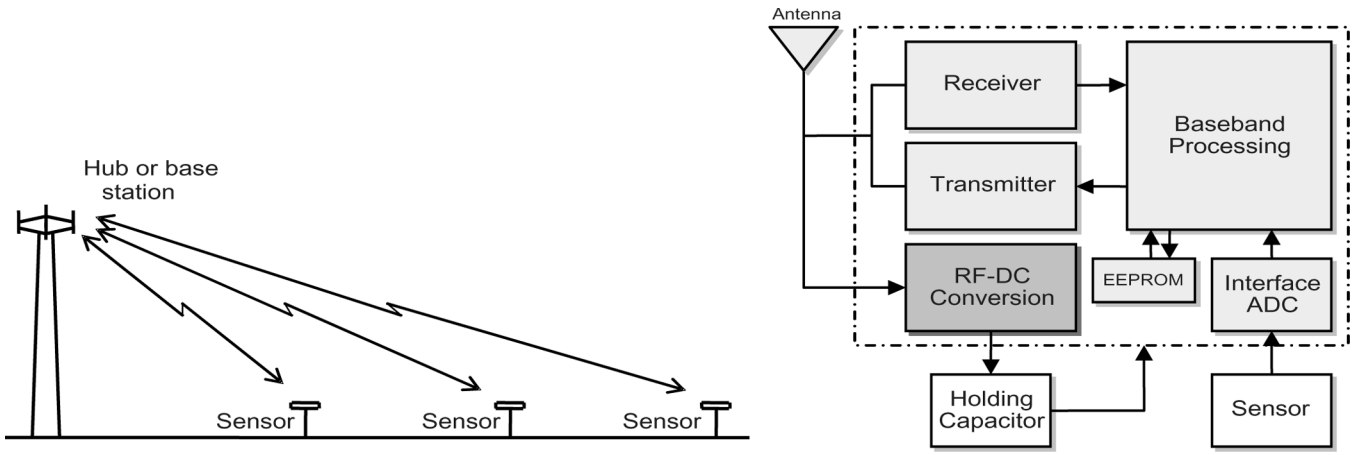

Fig. 1. (a) Illustration of communication links between base station (hub) and sensors in a passively powered sensor network. (b) Block diagram illustrating the RF-DC power conversion system in a passively powered sensor.

designed in a 0.25 μm CMOS technology optimized to operate at very low received power. A receive antenna is designed in a 4-layer FR4 board to maximize power transfer in the system. Section II provides the system overview of the far-field RF power conversion system and describes the importance of each of the major blocks and design issues in the system. Section III presents the circuit level design of the far-field RF-DC power conversion system where the different rectifier designs are shown. Section IV provides the design and measurement details for the receive antenna. Section V describes the overall test setup and experimental results for the full system and compares the results to recently published designs.

II. System Overview

When RF powered devices harvest their power from RF wave radiation, a radiating source or base station is required to transmit a high-intensity RF signal wirelessly through the air. Fig. 1(a) shows how the system operates as a network where multiple sensors receive their energy from the same power source. The high-intensity RF signal is then picked up by a receiving antenna on the sensor and the RF signal is converted to a DC voltage as shown in Fig. 1(b). The DC voltage is stored on a holding capacitor and supplies power to the integrated circuits.

The RF to DC power conversion system is designed to operate in UHF frequencies in the ISM band of 902–928 MHz. In this frequency range, RF power is transmitted more efficiently for longer distances and experiences lower propagational losses than higher frequency bands (i.e., 2.4 GHz). The system is optimized to operate at distances above 10 meters, with load current below 1 μA, and with the capacity to store charge for long periods of time. Given that the power density drops off at the rate of $1/d^2$ in free space, the propagational RF signal loss through the air at 915 MHz can be calculated to be 51.6 dB with the Friis equation for freespace loss [19]. The maximum transmit power allowed by the FCC in the 902–928 MHz band is 36 dBm EIRP (30 dBm maximum transmit power with 6 dB antenna gain) [20], thus the received power for distances greater than 10 meters is below 27 μW, this translates to less than 75 mV in a 50 Ω matched system. The power conversion circuit must be highly sensitive for long range operation, thus the threshold voltage of the system must be greatly reduced to improve power conversion efficiency at distances greater than 10 meters. It is also essential to come up with design techniques at the system level that can increase the voltage available for rectification to further increase the power conversion efficiency.

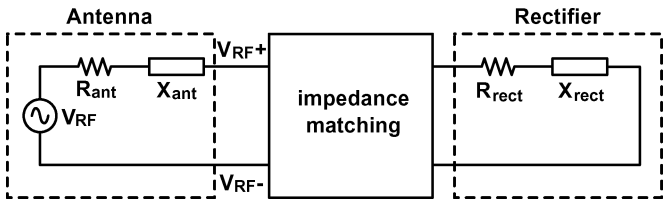

Fig. 2. Passive RF-DC conversion circuit showing the equivalent circuit representation for the antenna and rectifier.

An RF-DC power conversion system is designed to passively amplify the voltage available for rectification by forming a high-Q resonator. The main intent of the system is to maximize the voltage coming into the RF-DC power conversion system so that it can provide a stable DC output voltage at ultra-low receive power. The system, shown in Fig. 2, consists of an antenna to pick up the power radiated by the RF waves, an impedance matching network to ensure maximum power transfer in the system, and a rectifier circuit to convert the RF signal to a DC voltage. The passive amplification of voltage is done by matching the impedances between the receive antenna and the rectifier circuit. Due to the high-Q nature of the voltage rectification circuit, to be shown later in Section III, the impedance matching creates a high-Q resonator between the receive antenna and the rectifier circuit. The details of each block shown in Fig. 2 as well as system level design issues are subsequently discussed to define specifications and limitations of the power conversion system.

A. High-Q Resonator

The key method to improve the efficiency of the RF-DC power conversion at the system level is to maximize the input voltage to the rectifier. This is done by forming a resonator with

high loaded quality factor, Q, between the impedances of the receive antenna and the rectifier circuit. By doing this, it passively amplifies the incoming RF signal. To ensure the maximum possible power is transferred to the rectifier circuit, the receive antenna impedance is matched to the input impedance of the rectifier circuit [21]. Due to the fact that systems with high-Q resonate with greater amplitude at the resonant frequency than systems with low-Q, the high-Q resonator acts as a passive voltage-amplifier to increase the peak voltage coming into the input of the rectifier without dissipating additional power. The passive voltage gain from the high-Q resonator is directly proportional to its loaded Q. With an increase in the amplitude of the voltage coming to the input of the rectifier, the output voltage of the rectifier also increases and, therefore, increases the overall power conversion efficiency of the system. One drawback of the high-Q resonator is it can reduce the operating bandwidth of the RF-DC power conversion system since

$$Q = \omega \cdot \left(\frac{\text{Energy Stored}}{\text{Average Power Dissipated}} \right) \text{ or } Q = \frac{f_c}{\Delta f} \quad (1)$$

where ω is the resonant frequency in radians/second, f_c is the center frequency of operation, and Δf is the bandwidth of the system [21]. For the far-field RF-DC power conversion system operating in the band 902–928 MHz, the maximum loaded Q that can be attained without sacrificing bandwidth is 35. This limitation on the system Q does not cause much concern since on-chip components rarely have unloaded-Q of more than 10, and the parasitic resistance from these components damp out the resonator to prevent the Q of the system from limiting the bandwidth. In the case of a series connected matched *LC* resonator, the reactive components are complex conjugates of each other and the resistive components are matched. The loaded Q of the resonator is therefore

$$Q = \frac{1}{2}\frac{\omega L}{R} = \frac{X_L}{2R} \text{ or } Q = \frac{1}{2}\frac{1}{\omega RC} = \frac{X_C}{2R} \quad (2)$$

where X_L and X_C are the reactive components, and R is the resistive component of the *LC* resonator. The loaded Q of the resonator is half the unloaded Q of the rectifier and antenna since the resistance in the series connected matched resonator is doubled. To achieve a high system Q, it is therefore desirable to increase the reactive components of the rectifier and antenna while reducing resistive components.

B. Impedance Matching

A matching network between the receive antenna and rectifier is necessary to fine tune the impedance match between the antenna and the rectifier to further reduce transmission loss and increase the voltage gain [22], [23]. Coarse impedance matching is done through circuit and antenna design but fine impedance matching must also be done on the PCB for more accurate matching. Fig. 3 shows the simulated effect of impedance mismatch for a typical high-Q resonator. The maximum voltage gain that can be attained is equal to the loaded Q of the resonator, or half that of the unloaded rectifier Q. With impedance mismatch greater than 7%, the passive voltage gain from the resonator is reduced to below 3 regardless

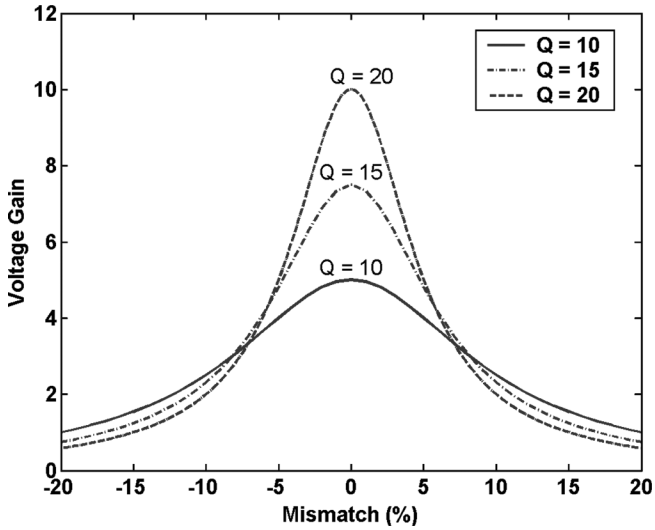

Fig. 3. Effect of impedance mismatch in high-Q resonators.

of the resonator Q. With impedance mismatch greater than 15%, the high-Q matching network provides no voltage gain and even yields a voltage attenuation that becomes greater with increasing Q. The impedance mismatch between the antenna and rectifier must be minimized to obtain a high voltage gain.

C. Rectifier Circuit

From the top level block diagram, the rectifier circuit is modeled by an impedance with a real part R_{rect} and a reactive part X_{rect} (Fig. 2). From the system point of view, the rectifier circuit must be designed to reduce threshold voltage loss (V_{th}) as much as possible to improve the efficiency of the RF-DC power conversion system. The rectifier circuit must also be designed so that the output voltage can be scaled by cascading multiple rectifier stages in series. Improving the Q of the rectifier input impedance is essential to increasing the power conversion efficiency of the overall system. The rectifier input impedance Q should also be kept as high as possible and parasitic components in the rectifier must be kept as low as possible to maintain a high overall system Q and thus power conversion efficiency.

The number of cascaded rectifier stages in the RF-DC conversion system also has a significant effect on the rectifier input impedance. In a conventional voltage rectification circuit design in CMOS technology, the rectifier impedance as seen from the input is capacitive and resistive due to the gate capacitance and the channel resistance (r_{ds}) of the MOS transistor [24]. In general, cascading multiple rectifier stages in series causes capacitive components to increase linearly with the number of stages while providing parallel paths causes the resistive component to decrease. With a large number of stages, the resistive component from the rectifier is so low that it is dominated by other sources of parasitic resistance (i.e., drain and source connection resistors) and hence, the Q of the system is reduced due to a linear increase in parasitic capacitance.

If there are too few rectifier stages in cascade, the output voltage of the rectifier may not be high enough to operate the sensor node. As the number of rectifier stages increases, the DC output voltage increases until the number of rectifier stages

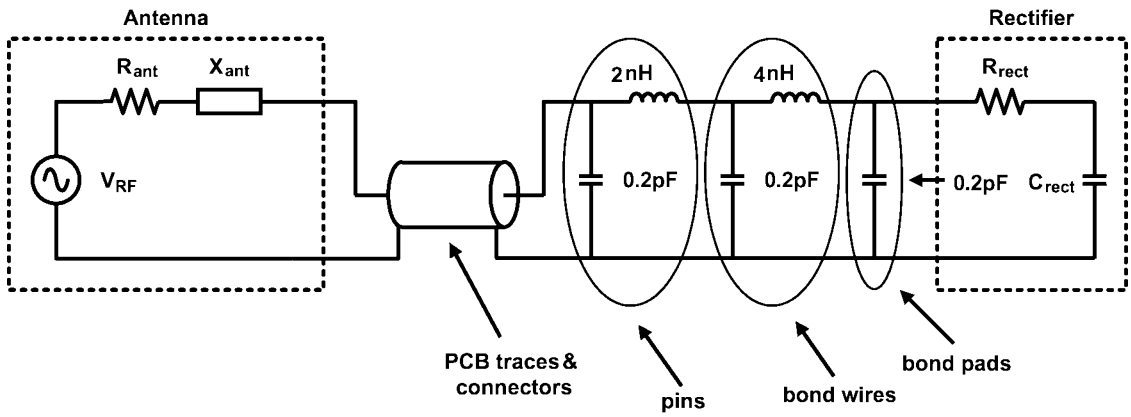

Fig. 4. Parasitic components that affect performance of the RF-DC power conversion circuit.

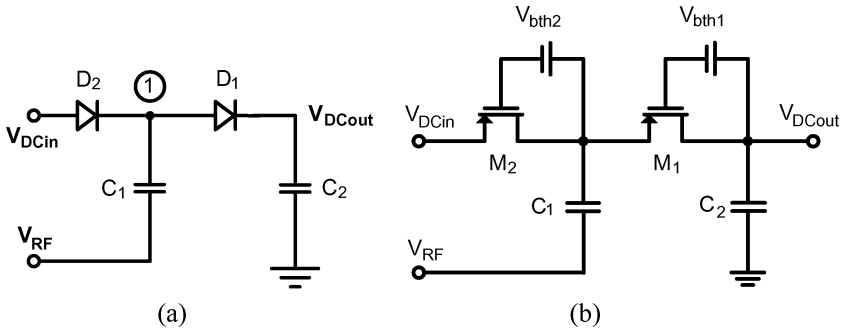

Fig. 5. (a) Conventional voltage doubler rectifier. (b) PMOS floating-gate rectifier.

reaches an optimal point. Adding more stages beyond the optimal point reduces the system Q and causes a reduction in the DC output voltage. Thus, it is critical for the number of rectifier stages to be selected through extensive circuit simulation so that the output DC voltage is maximized while maintaining a high system Q to achieve maximum power conversion efficiency.

D. Parasitic Components

A major design issue at the board level is reduction of the unwanted parasitic components that affect system performance. Since the system is to be designed with a high-Q resonator, any additional parasitic components between the antenna and rectifier will greatly diminish the performance of the power conversion system. It is therefore critical to specify an accurate parasitic model for simulating the effect of all parasitic components that affect power conversion efficiency. In the design of the RF-DC power conversion system, the traces connected to inputs of the rectifier are most sensitive to parasitics since a high-Q resonance is required at these inputs. Fig. 4 shows the equivalent circuit model for the parasitic components that affect the power conversion efficiency of the rectifier circuit.

These parasitic components cannot be avoided altogether, but the value of each parasitic component can be reduced through careful layout and package selection. The bond pad can be designed to be minimum size and only consisting of the top two metal layers to reduce bond pad capacitance to the substrate. The package for the integrated circuit is selected so that pin parasitics are minimized and critical input pins are placed in locations where the length of bond wires is minimized. PCB traces are made as short as possible and they are impedance controlled to reduce the parasitic capacitance and inductance.

E. Receive Antenna

The antenna design is critical in the RF-DC power conversion system since it must extract the power radiated by the RF waves. The antenna performs best when it is impedance matched to the rectifier circuit at the operating frequency to reduce transmission loss from PCB traces. Also, the antenna must be small in area and must have a bandwidth large enough to cover the frequency band from 902–928 MHz. More details of the specific design employed here is given in Section IV.

III. Rectifier Design

A study of different rectifier designs is done and the voltage doubler rectifier configuration is chosen [25]. Fig. 5 shows the conventional voltage doubling rectification circuit and the proposed floating-gate rectification circuit. For the floating-gate rectification circuit, floating-gate devices are used to create a gate-source bias to reduce the threshold voltage loss of the MOS transistor.

A. Conventional Voltage Doubler Rectifier

The voltage doubler rectifier structure is considered for the design of the RF-DC power conversion system because it rectifies the full-wave peak-to-peak voltage of the incoming RF signal and it can be arranged in cascade to increase the output voltage. The voltage doubler rectifier in Fig. 5(a) consists of a peak rectifier formed by D_1 and C_2 and a voltage clamp formed

by D_2 and C_1. The voltage clamp and the peak rectifier are arranged in cascade configuration to provide a passive level shift in voltage before rectification.

In the negative phase of the input, current flows through diode D_2 while D_1 is cutoff. The voltage across diode D_2 stays constant around its threshold voltage and the voltage at node 1 is charged to $-V_{\rm th2}$. At the negative peak, the voltage across capacitor C_1 is $V_{\rm amp} - V_{\rm th2}$ (where $V_{\rm amp}$ is the amplitude of the input signal.) In the positive phase of the input, current flows through diode D_1 while D_2 is in cutoff. The voltage across capacitor C_1 remains the same as the previous phase because it has no way to discharge. At the positive peak, the voltage across D2 is $2V_{\rm amp} - V_{\rm th2}$. Since D_1 is conducting current to charge C_2, the voltage at the output is a threshold voltage below that across D_2, i.e., the voltage at the output $V_{\rm out}$ is $2V_{\rm amp} - V_{\rm th2} - V_{\rm th1}$.

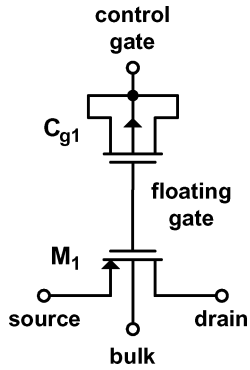

Fig. 6. PMOS implementation of a floating gate transistor.

B. Floating-Gate Voltage Doubler Rectifier

The floating gate devices may be designed to passively reduce the threshold voltage of the rectifier circuit. In a floating gate device, when charge is injected into the floating gate of the transistor, it remains in the gate oxide because of the high impedance provided by the oxide layer. There are previous methods designed to compensate for the threshold voltage drop in voltage rectification circuits [28], [30]. The threshold reduction method shown in [28] requires the input voltage to be sufficiently large to start up the circuit. This method also requires a bias resistor R_b which generally has resistance in the megaohm range (i.e., large physical size). Although the static power dissipated from this resistor is minimal, it causes a bias voltage much less than the desired threshold voltage. The voltage drop across a diode tied transistor under 10 nA bias is much different than one drawing 10 μA of current, this voltage difference is typically 100 mV for every decade of current difference, yielding an effective threshold of a few hundred millivolts. The threshold reduction technique in [29] suffers from the same constraint, as it uses diode-tied transistors biased at 2 nA to generate bias voltages for diode-tied transistors drawing current in the microamp range. This method would also require extra circuitry to generate a voltage bias and differential clock which requires a secondary battery. Zero-threshold transistors may also be used for voltage rectification but they only have zero threshold for a small current range. The floating-gate rectifier technique allows the threshold of the rectifier circuits to be programmed and can be optimized to operate over a wide range of currents. For the floating-gate rectifier circuit, the overall rectifier architecture is the same as the voltage doubler rectifier circuit. The diodes D_1 and D_2 are replaced by diode-tied floating gate transistors. The gate oxide is a very good insulator which keeps the charge from leaking off in the floating gate [26].

To design a floating gate device in a standard CMOS process, a MOS capacitor is placed in series with the gate of the diode-tied transistor as shown in Fig. 6. The gate of the diode-tied transistor and the gate of the MOS capacitor are connected together to form a high-impedance node to trap charges in the floating gate. The charge in the floating gate is therefore fixed which results in a fixed voltage bias across the MOS capacitor. The charges that are trapped inside the floating gate device act as a gate-source bias to passively reduce the effective threshold voltage of the transistor.

The floating-gate devices need to be initially programmed to reduce the threshold voltage of the rectifier, thus enhancing the power conversion efficiency. The charge on the floating gate can be injected via Fowler–Nordheim (F-N) tunneling when the rectifier is not operating, or it can be charged by injecting a relatively large sinusoidal signal to the input of the rectifier at any time. The F-N tunneling technique charges the floating gate to the desired voltage much faster, but the amount of charge is harder to control and also, additional circuitry is needed to inject or remove charge from the floating gate. Similar to programming a non-volatile Flash EEPROM, the programming node is driven by a high-voltage pulse to force a sharp bend in the energy band diagram of the floating-gate device. This enables charge to enter the insulated floating-gate by means other than the mechanism of F-N tunneling. The applied programming sinusoidal input voltage has amplitude larger than the threshold voltage of the transistor used for rectification. Charge is injected into the floating gate via the parasitic capacitance between the gate-source and gate-drain junction of the transistor and by hot electron effects. The large sinusoidal signal is externally generated and applied directly to the input of the rectifier until the output reaches an optimal point. If the floating-gate node is over charged, a negatively biased sinusoidal wave may bring it back to the optimal point. The sinusoidal signal can be applied in pulses with peak voltages between 5–6 V with 2.5–3.0 V DC bias or by a continuous train of signals at lower voltages and bias, depending on the duration of the pulse train.

The programming pulse does not need to be sinusoidal, but as the pulse is applied to the input node (which is high-Q), the pulse will be transformed to more of a sinusoidal signal. By applying a sinusoidal signal, the amplitude of the applied pulse can be better controlled. In our work, all floating-gate programming nodes are capacitively coupled and can be programmed simultaneously from the same programming pin, with all other circuitry grounded, via a F-N tunneling technique, and by the application of the sinusoidal signal at the input nodes when the rectifier is operating. The floating-gate rectifier is programmed with iterations of 20 pulses with a 5 ms trigger, 5 V amplitude and 2.5 V DC offset and repeated until the output voltage is at the maximum point for a wide range of currents. If the floating-gate is over charged, 10 deprogramming pulses with 5 ms trigger time,

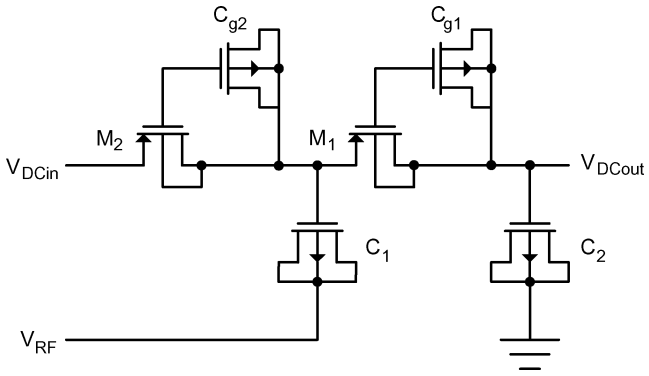

Fig. 7. Transistor level schematic of PMOS floating-gate rectifier.

−6 V and −3.0 V DC offset are injected at the programming node to recover charge on the floating-gates.

With the floating-gate device, the threshold voltages of the diode-tied transistors M_1 and M_2 are reduced by creating a gate-source bias. The gates of transistors M_1 and M_2 in Fig. 5(b) are high-impedance nodes so any charge trapped in the floating gates can be retained for a long time. Retaining charge in floating-gate devices is critical to the useful lifetime for the power conversion circuit under discussion. With the 70 angstrom oxide thickness in the 0.25 μm CMOS process, the device retains charge in the floating gate in excess of 10 years for normal operation at room temperature [32]. However, the performance of the rectifier circuit may reduce slightly as charge is leaked from the floating gate. During fabrication, the residual charge trapped in the floating gate may also affect the threshold voltage of the rectifier circuit, hence the floating gate must be programmed to account for these residual charges. Removal of residual charge may be done initially with the F-N tunneling method, which is a high-voltage pulse applied to a separate control gate of the floating-gate device.

The transistor level schematic of the 36-stage floating-gate rectifier is shown in Fig. 7. V_{RF} represents the input signal extracted from the RF wave, V_{DCin} is the input DC voltage coming from the previous rectifier stage and V_{DCout} is the output DC voltage of the rectifier. The 36-stage design uses diode-tied PMOS transistors as rectifying devices and a MOS capacitor (MOSCAP) is used to create the gate-source bias for each individual diode-tied transistor in the rectifier. The MOSCAPs (C_{g1} and C_{g2}) are designed to operate for the most part in the depletion region and their capacitance is a function of the applied voltage. To create the gate-source bias, a large sinusoidal signal is applied at the input of the rectifier and charge is injected over time through the parasitic capacitance of the diode-tied transistors. When the gate-source bias reaches a potential close to V_{th}, the capacitance reaches a flat point and remains constant. The amount of charge stored in the floating gate reaches equilibrium and the MOSCAP operates in the inversion region, the source-gate bias voltage is, therefore, approximately the threshold voltage of the diode-tied transistors (M_1 and M_2).

C. Multistage Rectifier Circuit

The individual stages of the floating-gate voltage doubler rectifier circuit can be arranged in cascade to increase the output voltage of the rectifier [16], [31], [35]. Fig. 8 shows N stages of a voltage doubler rectifier in cascade. When the rectifier stages are cascaded, each rectifier stage acts as a passive voltage level shifter in addition to the voltage shift in voltage clamp and peak rectification. The number of rectifier stages used in the design is important since too few rectifier stages yields insufficient output voltage and too many rectifier stages damps out the effect of the high-Q resonator.

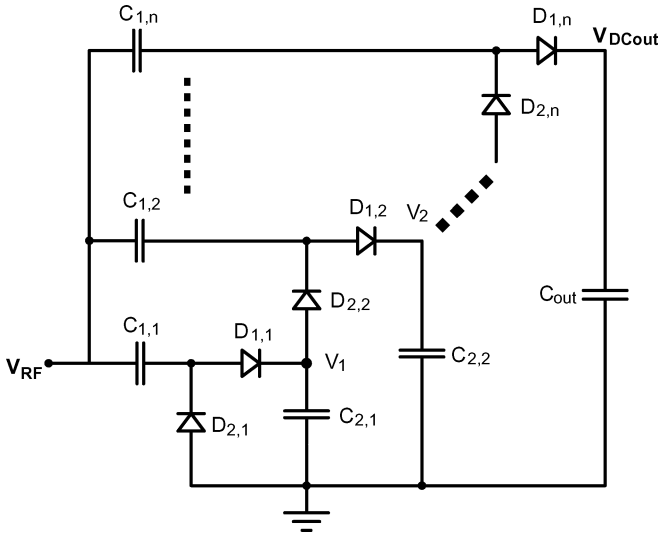

Fig. 8. Rectifier with N gain stages in cascade.

One of the important tradeoffs in the design of the voltage doubler rectifier is the size of the transistor versus parasitic capacitance [33], [34]. The smaller the transistor size, the less parasitic capacitance it has, however, rectification efficiency is lowered by the smaller transistor size since smaller transistor can deliver less current to the load. The transistor sizes can be reduced to a few times the minimum width to reduce parasitic capacitance as seen from the input of the rectifier, however, the reduction in channel width may cause a decrease in the performance of the rectifier due to the increase in the channel resistance of the diode-tied transistors. Two different designs are implemented to compare the tradeoffs between a reduction in the parasitics and the rectifier performance.

D. Rectifier Designs and Optimization

Two designs in a 0.25 μm CMOS process are evaluated to illustrate the tradeoffs in the design. The first design uses a relatively large device size of 12 μm/0.24 μm (NMOS) and the second uses 2 μm/0.24 μm PMOS devices. The larger device-size, NMOS floating-gate rectifier is first designed to test the functionality of the floating-gate rectifier circuits while the smaller device-size, PMOS rectifier is a follow-up design to improve the performance of the RF power conversion circuit for longer distance operation. The PMOS rectifier is designed with smaller device sizes to decrease the parasitic capacitance for each stage and consequently to increase the number of rectifier stages. This leads to a higher output voltage and longer operating range. Also, the PMOS transistor is chosen over an NMOS transistor to reduce the variation of threshold voltages between the different rectifier stages due to the body effect. Fig. 9(a)

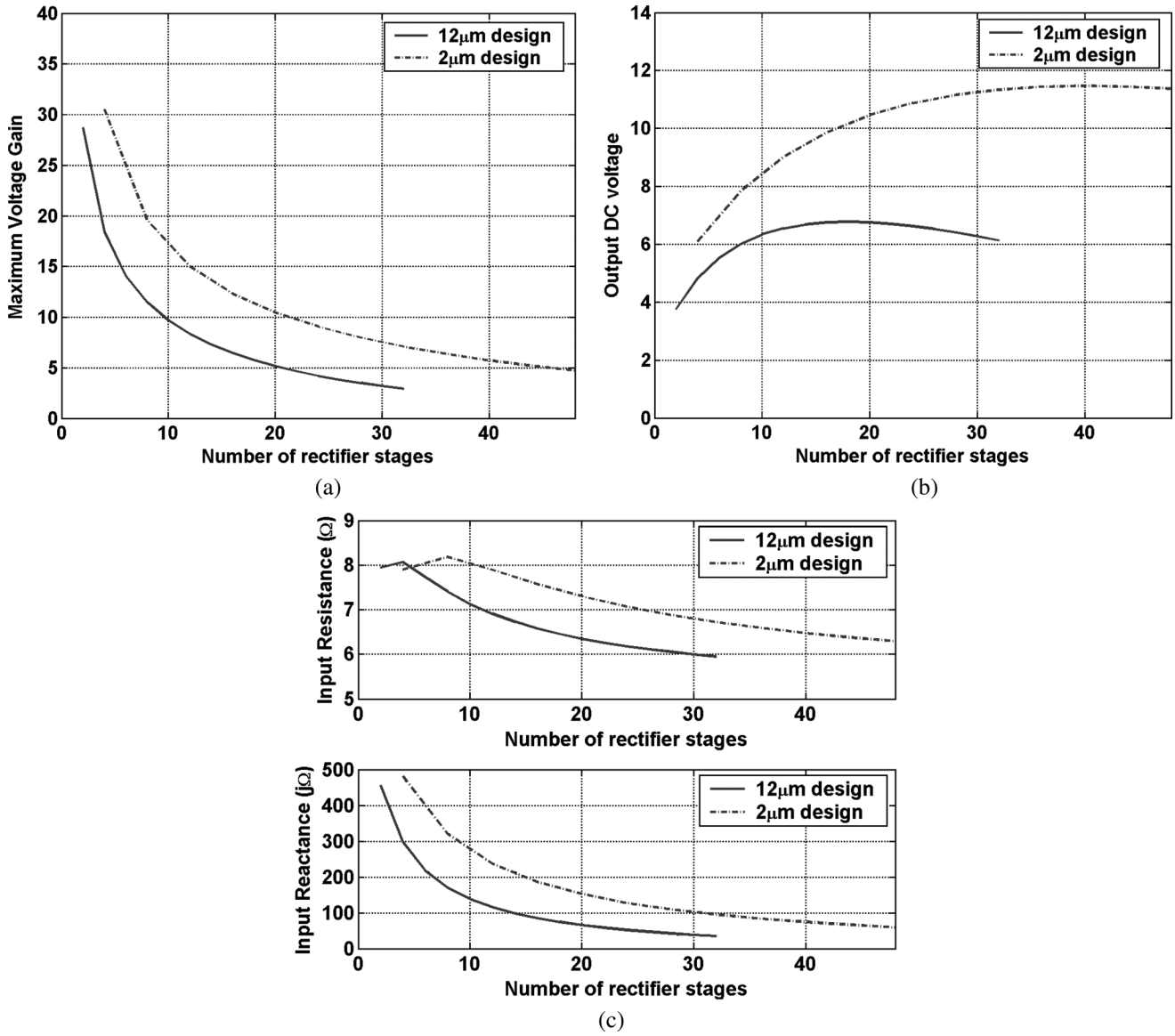

Fig. 9. Effect of number of rectifier stages on (a) maximum voltage gain, (b) output DC voltage, and (c) input impedance of rectifier.

shows the maximum voltage gain that can be achieved in the rectifier with different numbers of floating-gate rectifier stages arranged in cascade. As the number of rectifier stages increase, the resonator Q between the antenna and rectifier impedance is reduced. In fact, the resonator Q is inversely proportional to the number of rectifier stages.

The output voltage of the rectifier for both designs with an input voltage with 300 mV amplitude is shown in Fig. 9(b). The output voltage initially increases as more rectifier stages are added until an optimal point then it reduces as the resonator Q is decreased. The impact of the number of rectifier stages on the input impedance is shown in Fig. 9(c). As the number of rectifier stages increases, the capacitive component in the rectifier input impedance increases thus reducing the reactive component of the rectifier input impedance. The reactive component of the rectifier input impedance is found to be inversely proportional to the number of rectifier stages. With the decrease in the reactive component, the maximum voltage gain that can be achieved at the input is also decreased at the same rate since the resistive component in the input impedance stays fairly constant.

The optimized number of cascaded rectifier stages for the 12 μm (NMOS) and 2 μm (PMOS) designs is 16 and 36 stages, respectively. The simulated input impedance for the two designs is $6.6 - j85\,\Omega$ and $6.6 - j84\,\Omega$, almost identical to each other.

To establish the tradeoff between the transistor sizes used for rectification versus the number of rectifier stages, a model is extracted by curve fitting of the output voltage data for the two different designs. Fig. 10(a) shows a three-dimensional surface plot for the rectifier output voltage as a function of the number of rectifier stages and the transistor width. It can be observed that a width of 2 μm is the best design choice for the highest output voltage when the number of rectifier stages is below 40. Any increase in device size from 2 μm results in a reduction in the output voltage. Reducing the device size below 2 μm could lead to a slight improvement in the output voltage. However, the number of rectifier stages required is significantly increased

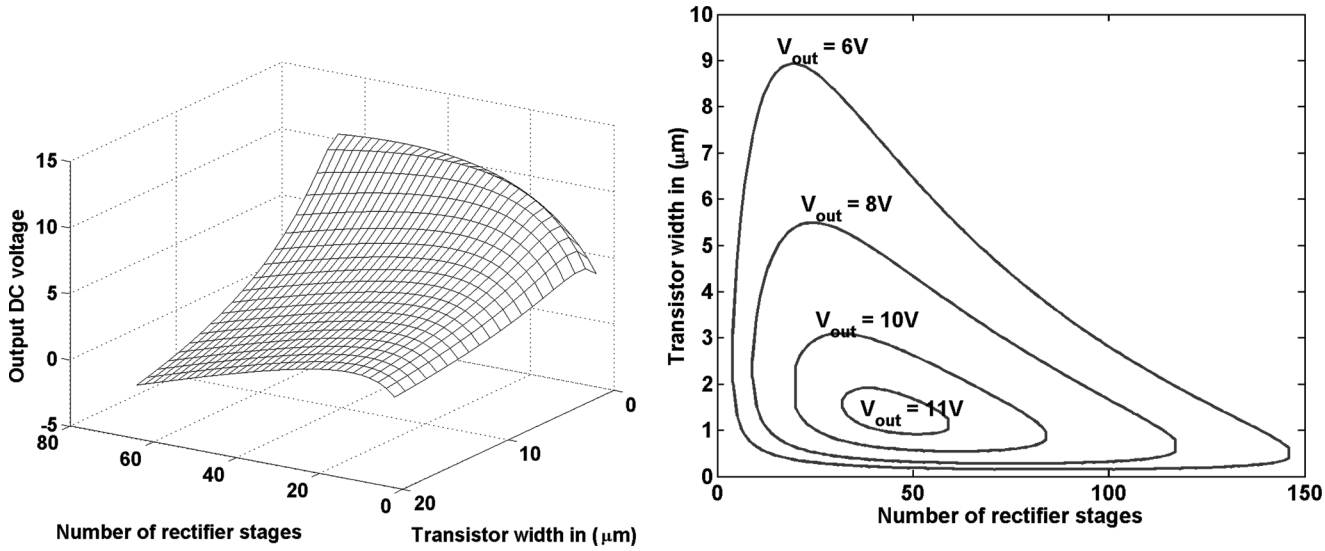

Fig. 10. (a) Output voltage curves as function of the number of rectifier stages and the transistor width. (b) Contour plot of constant output voltage.

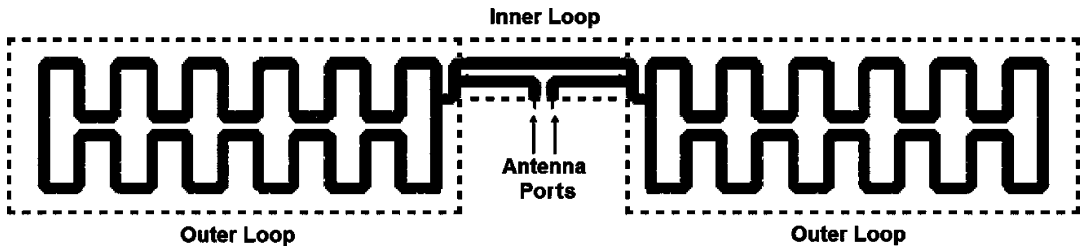

Fig. 11. Antenna design for RF-DC converter.

which results in a larger die size. Fig. 10(b) shows the constant output voltage contour plot as function of the transistor width and the number of rectifier stages. The 36 stage design with a 2 μm device size is very close to the highest voltage contour, thus, this design is optimal for the output voltage.

IV. Antenna Design

The antenna for the RF-DC conversion circuit is designed with meander lines on a printed circuit board to reduce the area of the antenna and to provide the desired antenna input impedance to the impedance matching network. Fig. 11 shows the antenna design with two outer loops on each side connected to an inner loop in the center. The antenna ports are in the middle of the design and connect to the antenna through the inner loop to transform the impedance as seen from the outer loops of the antenna. To achieve resonance at the desired frequency, the antenna is designed to match with the input impedance of the floating-gate rectifier circuit. The outer loop of the antenna is designed to tune the antenna to the correct operating frequency and the perimeter of the loop is 35 cm, roughly equal to one wavelength at 916 MHz. The perimeter of the inner loop varies depending on the value of the input impedance of the rectifier. The line of symmetry between the two sides of the antenna splits the antenna into two identical parts and acts as a virtual ground to create the fully differential signal at the antenna ports. The dimension of the drawn area of the antenna is 15 cm $\times$ 2 cm (6 $\times$ 0.8 inches).

The antenna design is tuned for maximum received power at 916 MHz and the antenna is designed on the top layer of a four-layer FR4 board with carefully controlled impedance to ensure the impedance of PCB traces does not vary from the intended values. The traces in the antenna are exposed so that they can be tapped to fine tune the operating frequency. The impedance matching network can be placed anywhere along the antenna to fine tune the matching between the antenna and the rectifier circuit. The antenna is designed with a bandwidth of about 40 MHz to maintain a high antenna Q. Due to the fact that the antenna must be impedance matched to the rectifier, the loop design provides little antenna gain in the antenna throughout the frequency bandwidth it operates.

Fig. 12(a) shows the simulated and measured input impedance of the antenna around the operating frequency band. The measured resistive component shows less than 1 Ω variation from the simulated value and the reactive component also correlates well with the simulated results. The measured input impedance components of the receive antenna for the 36-stage rectifier design are shown in Fig. 12(b). The reactance component for the rectifier is capacitive while the reactance for the antenna is inductive. From the measurement data, the measured resistive components of the antenna and rectifier match well throughout the intended bandwidth for both designs. The reactive component of the 36-stage design matches at 910 MHz.

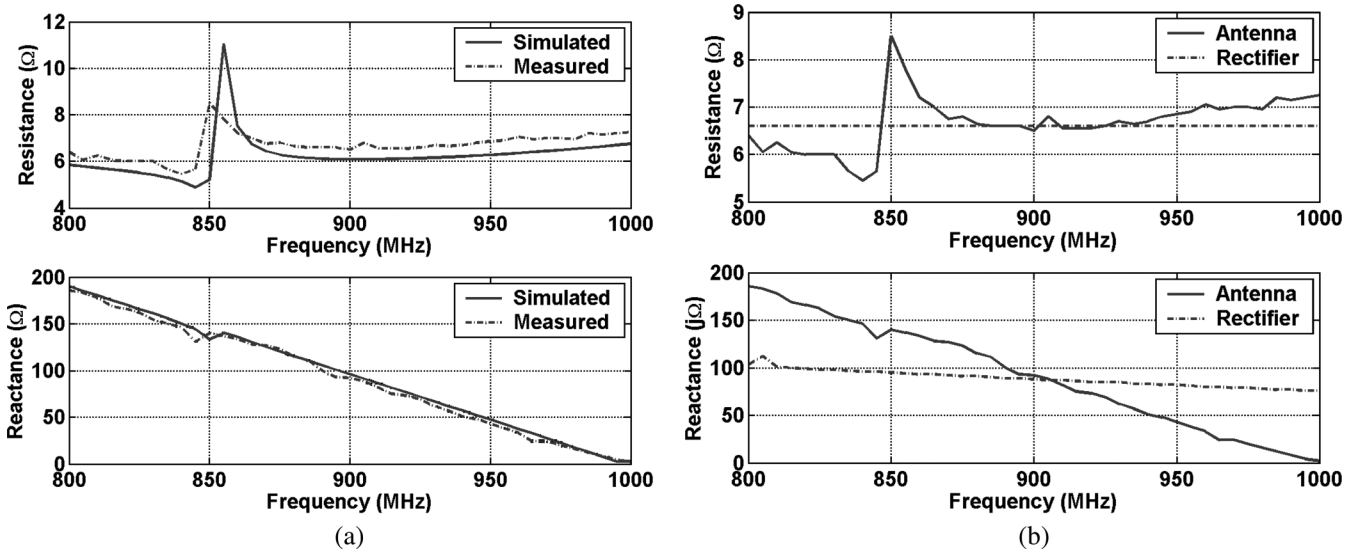

Fig. 12. (a) Simulated and measured components of the antenna input impedance. (b) Measured input impedance of antenna and rectifier circuit.

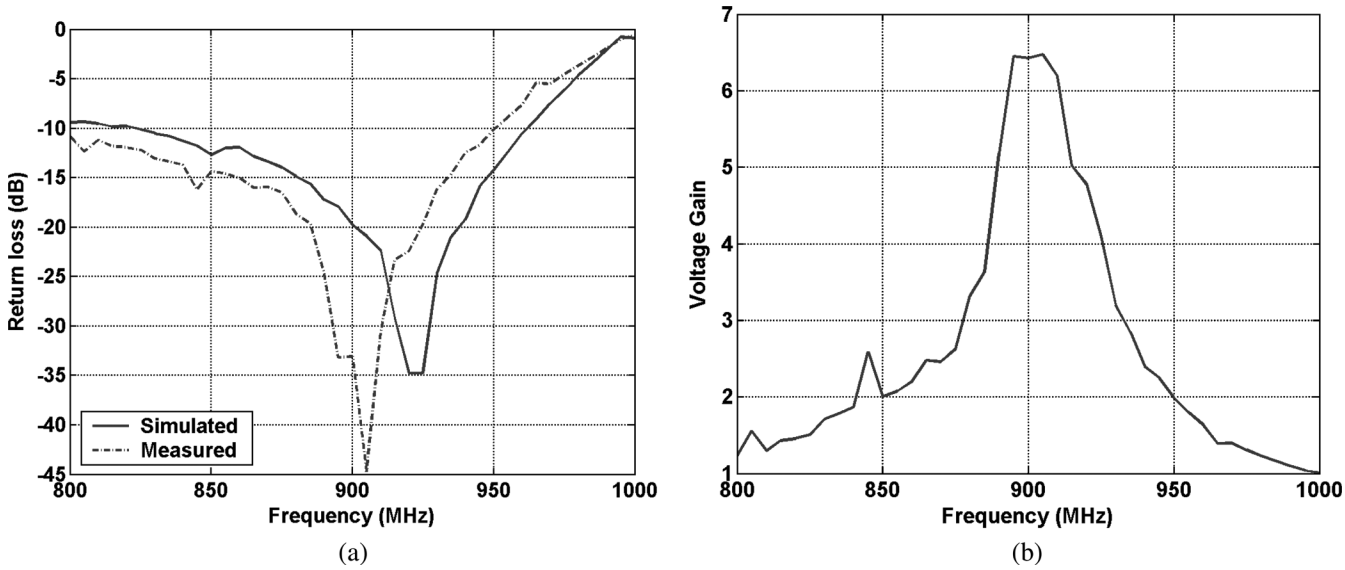

Fig. 13. (a) Measured return loss and (b) voltage gain for 36-stage rectifier design.

Fig. 13 shows the plot of the return loss (S_{11}) and voltage gain for the 36-stage design. The antenna is designed to match well enough so that less than 1% of the transmitted signal is reflected back to the antenna (i.e., S_{11} below -20 dB) in the frequency band of operation 902–928 MHz. The design achieves voltage gain above 5 in a 30 MHz bandwidth, however the peak voltage gain is shifted down by approximately 10 MHz from the intended 915 MHz center frequency.

V. Experimental Results

A. RF-DC Rectifier Circuit Performance

Rectifier designs with 16 NMOS stages and 36 PMOS stages were fabricated in a 0.25 μm five-metal single-poly CMOS process as shown in Fig. 14. The active die areas are 350 μm $\times$ 600 μm and 400 μm $\times$ 1000 μm, respectively. The majority of the active area is consumed by the MOSCAPs for floating gate devices and the holding capacitors. The 16-stage and 36-stage rectifier layouts are arranged in two rows of eight stages each and six rows of six stages each, respectively. Both dies have a pair of one-stage rectifiers included so that the functionality of the NMOS and PMOS diode-tied floating-gate devices can be individually characterized. Each rectifier is packaged in a 0.5 mm pin pitch QFN-32 package to reduce bond wire parasitics and trace lengths on the PCB.

In order to test the rectifier circuit, a small amplitude 1 MHz sinusoidal signal is applied directly to the input. The low-frequency signal is used to minimize parasitic effects introduced by the board as well as voltage losses in the PCB traces. The purpose of this experiment is to quickly obtain the desired output voltage characteristics of the floating-gate rectifier using a controlled input signal so the floating-node can be more easily programmed to reduce the threshold voltage of the rectifying transistors. At 900 MHz, the rectifying transistor output voltage is

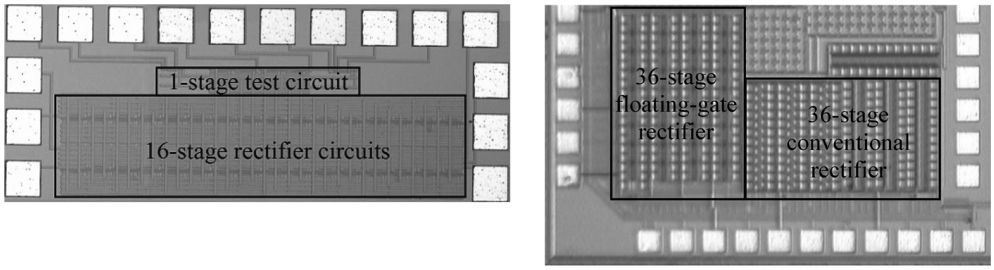

Fig. 14. Die photograph of (a) 16-stage rectifier circuit, and (b) 36-stage rectifier circuit fabricated in a 0.25 μm CMOS process.

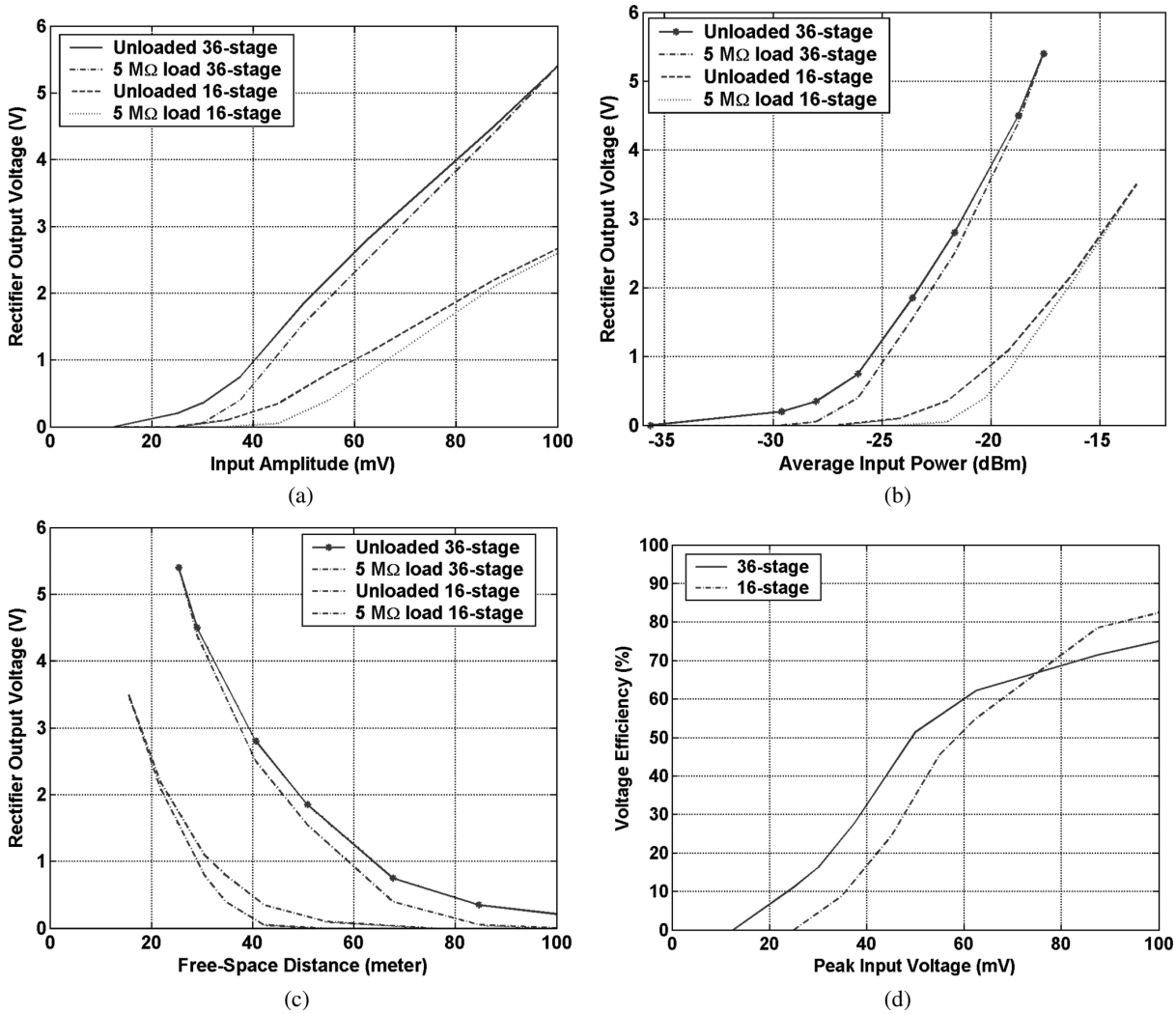

Fig. 15. Measured output DC voltage (a) as a function of the sinusoidal input, (b) as function of input power, (c) as function of distance, and (d) measured voltage efficiency.

reduced by approximately 1 mV/stage due to the delay in the diode response. The threshold voltage of the PMOS and NMOS transistors are approximately 550 mV and 450 mV, respectively, before the injection of charge. After charging the floating gate, the effective threshold voltage for both is between 30–50 mV. This can be seen in Fig. 15(a) as a sharp increase in the output voltage is observed in this voltage range. Fig. 15(a) shows the measured output DC voltage unloaded and with a 5 MΩ load for both rectifier designs as a function of the input sinusoidal amplitude. From a straight line extrapolation of the output voltage curves, the threshold voltage for the 16-stage rectifier is 36 mV compared to 30 mV for the 36-stage rectifier. Since the difference in threshold voltages is very small between the two rectifier designs, the improvement in the output voltage of the 36-stage rectifier is primarily due to the higher number of cascaded rectifier stages used in the design. The performance of the rectifier

TABLE I
TRANSIENT RESPONSE TIME OF FLOATING-GATE RECTIFIERS WITH 10 μF LOAD CAPACITANCE

Input amplitude	16-stage rectifier		36-stage rectifier	
	Unloaded	5MΩ load	Unloaded	5MΩ load
100 mV	1.06 s	1.03 s	2.34 s	2.31 s
80 mV	1.84 s	1.81 s	6.34 s	6.01 s
60 mV	4.60 s	4.42 s	19.32 s	16.54 s
40 mV	96.0 s	90.0 s	49.66 s	34.69 s

circuit can be specified by the sensitivity of the rectifier or the minimum input power required for voltage rectification. The average input power can be expressed as:

$$P = \frac{(V_{\rm rms}/Q)^2}{R} = \frac{(V_{\rm amp}/Q)^2}{2R} \tag{3}$$

where Q is the passive voltage gain from the antenna to the input of the rectifier, $V_{\rm rms}$ is the input rms voltage to the rectifier, $V_{\rm amp}$ is the rectifier input amplitude and R is the input impedance of the rectifier circuit. The voltage gain of the 16-stage and 36-stage rectifiers, measured from the return loss of the matching between the rectifier and antenna, is 4.8 and 6.4, respectively. Assuming a rectifier input impedance of 7 Ω, the equivalent input power is derived and shown in Fig. 15(b). In the case of the 16-stage rectifier, 2 V is achieved for 80 mV input, which is equivalent to a power of 20.95 μW (−16.8 dBm). Using the Friis formula for free-space wave propagation, this corresponds to an operating distance of 23 meters [Fig. 15(c)] assuming a 4 W radiating source [20]. This is the maximum theoretical distance that can be achieved with this design while keeping radiated power and antenna gain under the FCC emission limit. For the 36-stage rectifier circuit design, the rectifier performs better with low voltages due to the increased number of voltage doubler rectifier stages and the higher passive voltage gain. The 36-stage rectifier circuit achieves 2 V for an input voltage amplitude as low as 50 mV. Using (3), these values are equivalent to 4.7 μW of power (−23.3 dBm) at 2.0 V output. In free-space, this corresponds to 49 meters in distance.

Table I shows the transient rise-time of both floating-gate rectifier designs. The transient rise-time is defined as the time it takes for the rectifier output to charge to 90% of the maximum voltage with a 10 μF capacitive load. For the 16-stage floating-gate rectifier, the effective threshold voltage is approximately 36 mV. The transient response time of this rectifier is very slow when the input voltage is close to the threshold voltage but increases very rapidly as the over-drive voltage ($V_{\rm GS} - V_{\rm TH}$) increases, as a result, increasing the driving current. The charging time of the capacitor decreases by a factor of about 3 for every 20 mV increase in input amplitude. For the 36-stage floating-gate rectifier, the effective threshold voltage is approximately 30 mV and the transient charging has the same behavior as the 16-stage rectifier. The transient rise-time of the 36-stage rectifier also decreases by a factor of about 3 for every 20 mV increase in input amplitude as the input amplitude is greater than the threshold voltage.

Defining the voltage efficiency as the percentage of the theoretical voltage achieved [27], the theoretical output for the voltage doubler architecture is the number of cascaded rectifier stages times the peak-to-peak voltage into the rectifier. In the case of the 16-stage rectifier, the theoretical output voltage is 16 times the input peak-to-peak voltage. For input voltages above 100 mV, the rectifier efficiency is over 80% as shown in Fig. 15(d) and, hence, it is more efficient at higher input voltages. The voltage efficiency for the 36-stage design is higher as compared to the 16-stage rectifier design for low voltages.

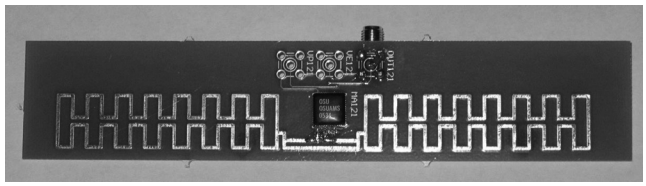

Fig. 16. PCB to test performance of the RF-DC power converter at the system level.

B. RF-DC Power Conversion System Performance

To test the overall performance of the RF-DC rectifier in actual applications, a custom printed circuit board was designed that includes the antenna with exposed metal traces for impedance and frequency tuning as shown in Fig. 16. The chip is directly soldered to the board and physically abuts to the antenna to minimize any stray inductance. The output DC voltage is observed via the SMA connector with an oscilloscope or a digital multimeter (DMM).

The performance of the RF-DC power conversion system can be measured wirelessly with propagating electromagnetic wave radiation. The output of an HP/Agilent 8665A signal generator is amplified by a Mini Circuits LZY-2 power amplifier to generate signals with 6W of power in the frequency range of 902–928 MHz. The signal at the output of the power amplifier is then fed to an antenna through several series connected SMA cables. The losses in the cable combined with the return loss between the power amplifier combined with the gain in the transmit antenna are measured to be around 1.7 dB. Thus, the maximum radiated power is about 36 dBm (4 Watts EIRP).

Only the 36-stage rectifier design is wirelessly measured since it has superior performance in terms of received power sensitivity. Before measuring the overall performance, it is necessary to tune the frequency of the resonator circuit. The resonant frequency can be tuned to the 902–928 MHz range by placing a shorted stub tuning on the bare metal trace at the end of the antenna on the PCB. The tuning of the resonant frequency does affect the output voltage of the RF-DC conversion circuit, since the shorted stub tuning slightly modifies the physical shape of the antenna. The decrease in the output voltage is greater when the original resonant frequency is further from the desired (i.e., longer length stub tuning) band and the decrease is smaller for a resonant frequency closer to the desired band. Although the frequency tuning does affect the output voltage, this change in output voltage is much smaller compared to the change in output voltage caused by impedance mismatch. For the 36-stage rectifier design, the resonant frequency is originally 860 MHz so the size of the loop is reduced only

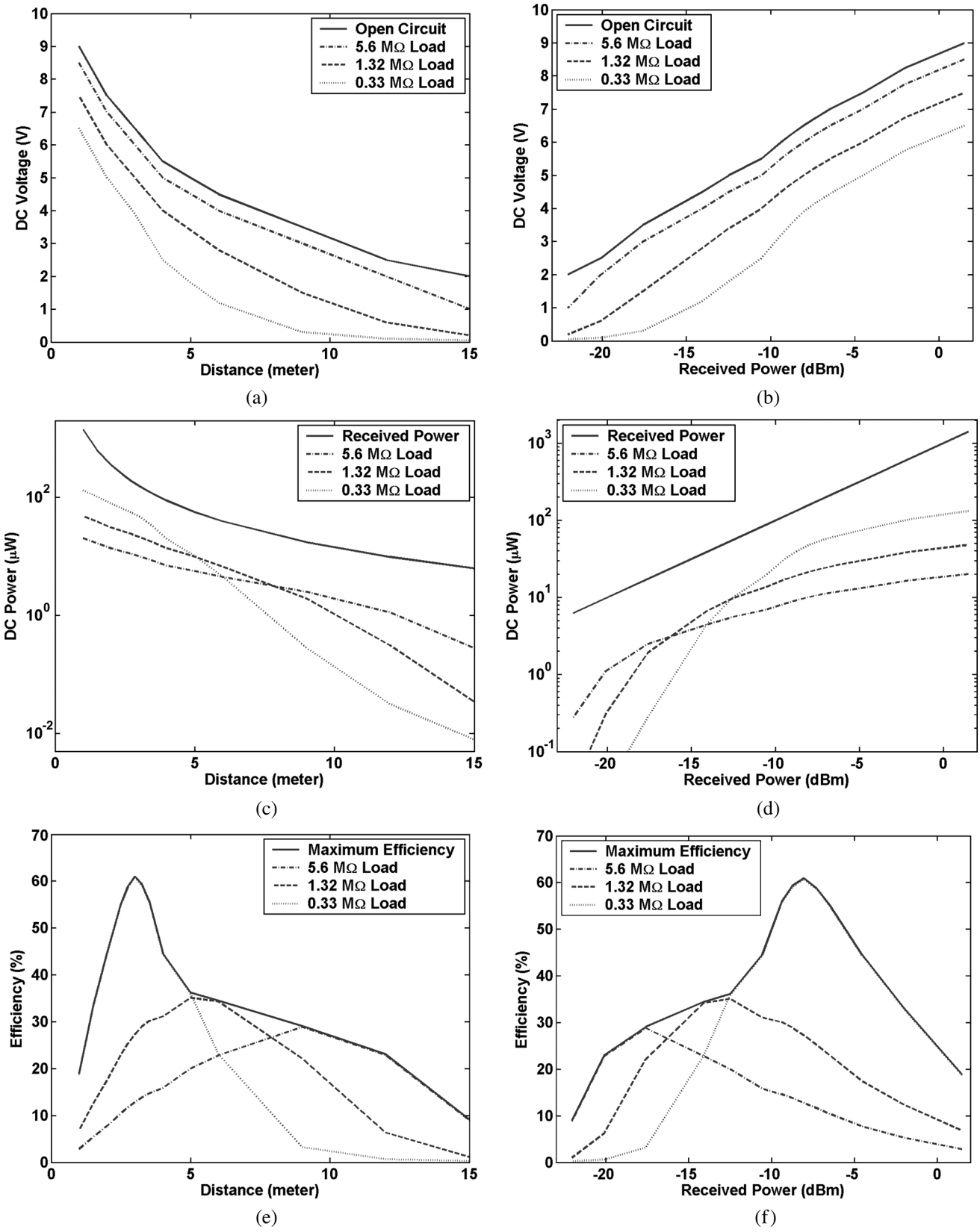

Fig. 17. Measured DC output voltage (a) as function of distance and load for the 36-stage rectifier, and (b) as function of received power for the 36-stage rectifier. (c) Measured output power performance as function of distance and load for the 36-stage rectifier. (d) Measured output power as function of received power for the 36-stage rectifier. (e) Measured power conversion efficiency curves as function of distance and load for the 36-stage rectifier. (f) Measured power conversion efficiency curves as function of received power for the 36-stage rectifier.

slightly to increase the resonant frequency to 906 MHz. For the wireless measurement of the RF-DC power conversion circuit, the center frequency is set at 906 MHz for the 36-stage rectifier design.

Fig. 17(a) and (b) shows the measured output voltage of the 36-stage rectifier as a function of distance and input power for various resistive loads. The 36-stage conversion circuit is capable of outputting DC signal levels of 2 V at distances up to 15 meters with a 36 dBm radiating source when it is not loaded as shown in Fig. 17(a). The measured output DC voltage decreases exponentially as distance increases and also decreases as the load resistance is decreased. With a 0.33 MΩ load, the conversion circuit operates within 7 meters from the radiating source while providing 1 V DC. From observation, the operating distance of the rectifier reduces quickly as the load current is increased while at closer distances, the dependence on load current is much less. Fig. 17(b) shows the output voltage curves of the 36-stage design as function of received power calculated from the Friis equation for free-space propagation loss. The slope of the output voltage curves is relatively constant over the full range since the output voltage is inversely proportional to the log of the operating distance. The 36-stage design operates well when the received power is higher than −22 dBm. Measurement of the far-field RF power harvesting system is done in a shielded lab, where the pathloss is enhanced by multipath and standing wave patterns. The same measurement is also performed in an open area with lower transmitted power and the distance of the measurement is increased by up to 1.4 times.

Fig. 17(c) shows the measured output power as a function of distance. The top curve represents the theoretical received power in free-space as calculated by the Friis formula for free-space propagation loss given a 36 dBm radiating source. With a 0.33 MΩ resistive load, the current requirement at the load is higher so more current is drawn from the output of the rectifier to drive the load hence the curve shows a steeper slope. The slope of the roll off is directly proportional to the load current at the output of the rectifier. With a 1.32 MΩ load, 1 μW at 10 meters is possible and up to 12.3 meters with the 5.6 MΩ load. Fig. 17(d) shows the output power as function of received power. From this plot, the point where the power curve starts to roll off from the straight (open circuit) line can be seen more clearly. For the 36-stage rectifier design, the output power starts to roll off at about −8 dBm for the 0.33 MΩ load, −13 dBm for the 1.32 MΩ load, and −18 dBm for the 5.6 MΩ load.

The measured power conversion efficiency versus distance curves are shown in Fig. 17(e) and (f). The power conversion efficiency curve for each individual load is shown as well as the maximum efficiency that can be achieved at a particular distance. For a perfectly matched resonator network, the power available for rectification is half of the received power in the antenna since only half of the power is dissipated in the rectifier. The power conversion efficiency of the RF-DC power conversion system is defined as the ratio between the DC output power and available power for rectification (half of the received power) from the antenna. The maximum efficiency measured is 60% with the 0.33 MΩ load. The power conversion efficiency peaks at around −8 dBm received power due to the fact that the output voltage reaches a maximum point of approximately 9 V, due to the reverse breakdown voltage of the p-n junctions. This peak can be moved or optimized, for example, by changing the number of rectifier stages and transistor sizes. For lower load currents, the power conversion efficiency is optimized at lower received power or longer distances from the RF source. On the other hand, at higher load currents, the power conversion efficiency is optimized at higher received power or shorter distances. The design of the 36-stage rectifier shows highest efficiency at 3 meters with a 0.33 MΩ load, and the power conversion efficiency curves rolls off as the inverse of distance from the RF source. The peak efficiency with the 5.6 MΩ and 1.32 MΩ load is 29% at about 9 meters and 35% at about 5 meters, respectively.

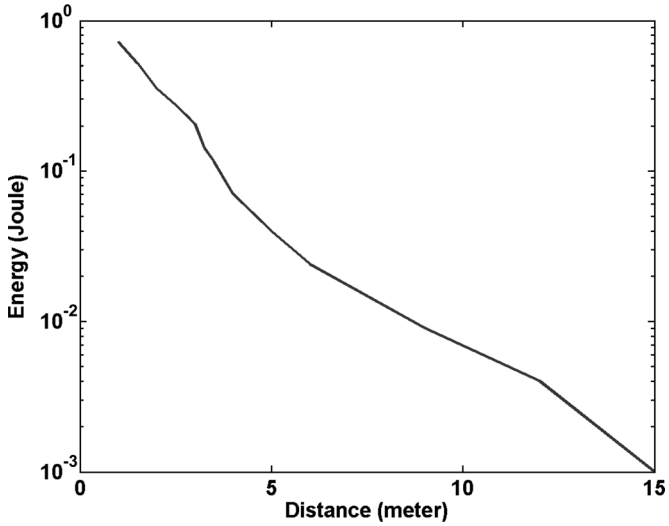

Fig. 18. Measured energy extracted per hour as function of distance for the 36-stage rectifier.

Fig. 18 shows the maximum energy that can be extracted from the RF signal in one hour at various distances from the radiating source. From the logarithmic plot of extracted energy against distance, the extracted energy curve is approximately a straight line. The maximum extractable energy in an hour is 0.8 J at 1 meter, 40 mJ at 5 meters, 7 mJ at 10 meters and about 1 mJ at 15 meters from the source. With one hour charge time, the RF-DC power conversion circuit acquires and replenishes enough energy to operate a circuit that dissipates 1 mW for one second or 100 mW for 10 ms at distances up to 15 meters. For an increase of every meter in distance, the amount of energy that can be extracted from the RF signal is reduced by a factor of 2.6. This establishes the trade off between power dissipation and operating distance of the integrated circuit powered by the RF-DC power conversion circuit.

Fig. 19(a) compares the voltage performance of the 36-stage power conversion circuit with recently published work [28], [29]. The work in [29], [30] uses an active switched capacitor circuit with a clock generator and an external power supply to actively bias the gate-source voltage of the diode-tied transistor in the rectifier circuit. The work in [28] uses a passive method

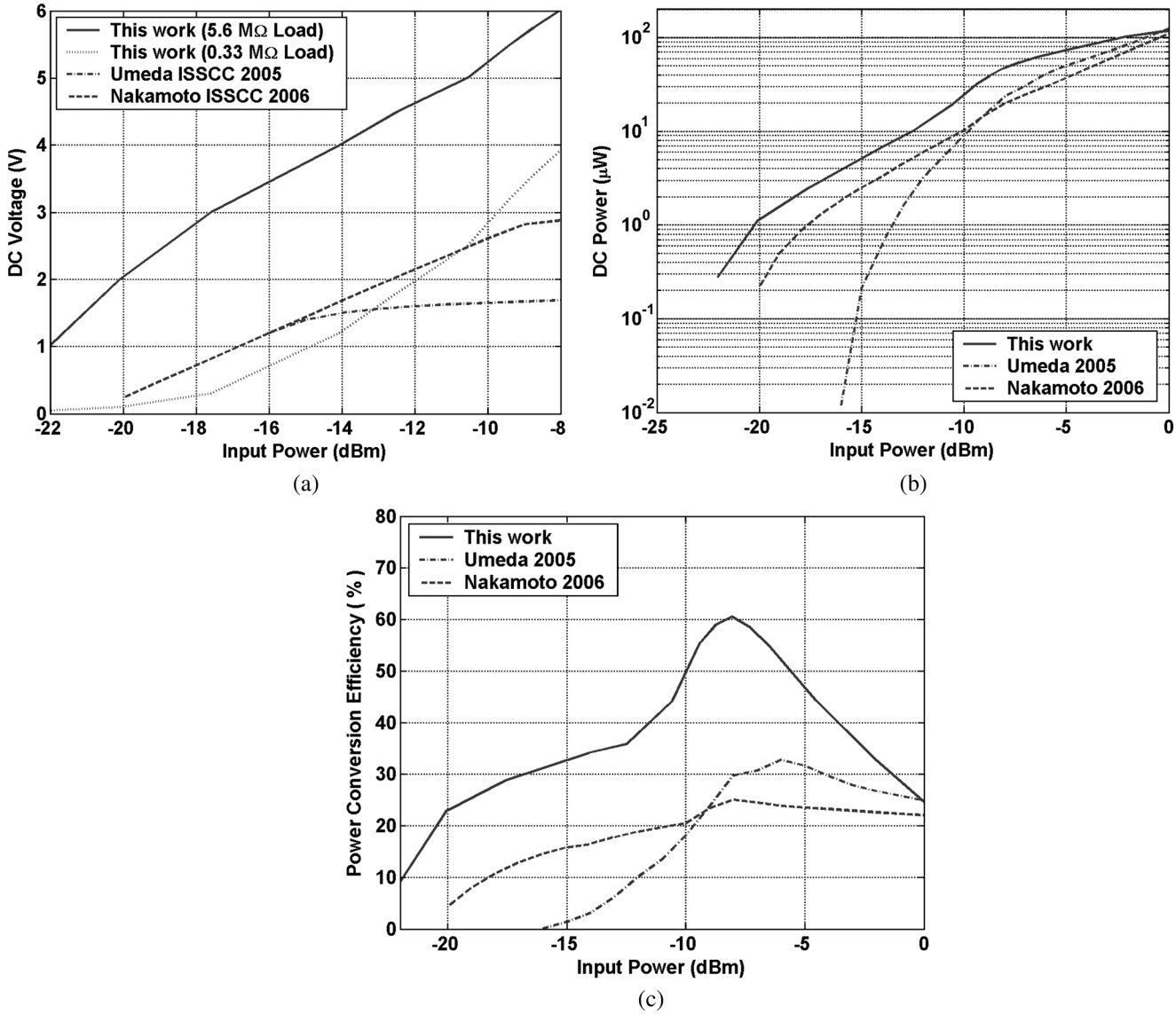

Fig. 19. (a) Output DC voltage as function of the input power. (b) Output DC power as function of the sinusoidal input. (c) Power conversion efficiency as function of the sinusoidal input.

to bias the gate-source voltage of the diode-tied transistor, however, the passive circuit does require static power to maintain the gate-source bias. This gate-source bias needs a large turn-on sinusoidal signal to start-up and takes a long time for the bias to charge up when a signal level below threshold voltage is applied. Once the power source is turned off, the gate-source bias will be discharged from the static current. The work in [29] requires the generation of a bias voltage $V_{\rm th}$ which uses a reference current in the nanoamp range, although the static power dissipated from the resistor is minimal, it causes a bias voltage much less than the desired threshold voltage. In other words, the voltage drop across a diode-tied transistor under 2 nA bias is much different than one drawing 2 μA of current. This voltage difference is typically 100 mV for every decade of current difference. Also, this method would require extra circuitry to generate a voltage bias and a differential clock and it would also require a secondary battery. The results obtained from [28] and [29] are measured from an applied sinusoidal input and the distance performance is calculated using the Friis equation for free-space. Distance performance in this work is the actual measured distance from the radiation source. Because [28] and [29] both have voltage regulation, only the voltage at the far distance is compared. The rectifier design in [29] is one stage, and in [28] is six stages, hence the output voltage is much lower than the 36-stage design under a 5.6 MΩ load, however, the output current with the 5.6 MΩ load is lower compared to [28] and [29]. With the 0.33 MΩ load, the current is increased but the output voltage is only comparable to the other two designs.

Fig. 19(b) shows the output power curves for the same three designs. The output power of this work greatly exceeds other designs and, for received power below −20 dBm, it gives output power level 5 times the output power of the closest design. The comparison of the power conversion efficiency is shown in Fig. 19(c). This design is 30% more efficient throughout the full range with a peak efficiency of 60%. Table II summarizes this work as compared to previously published work.

TABLE II
PERFORMANCE SUMMARY

Design	**This work**	Umeda	Nakamoto	Karthaus	Kocer
Technology	**0.25 µm**	0.30 µm	0.35 µm	0.5 µm	0.25 µm
Max. Efficiency	**60 %**	33 %	24 %	28 %	11 %
Min. RF Power	**5.5 µW -22.6 dBm**	40 µW -14 dBm	100 µW -10 dBm	16.7 µW -17.8 dBm	60 µW -12.3 dBm
Distance (Free space)	**42 meters @ 4W**	17 meters @ 4W	11 meters @ 4W	26 meters @ 4W	13 meters @ 4W
Distance (Measured)	**15 meters @ 4W**	2 meters @ 4W	4.3 meters @ 4W	4.5 meters @ 1W	1.7 meters @ 60mW

VI. CONCLUSION

A passively powered RF-DC conversion circuit operating at 906 MHz is presented. A novel rectifier circuit is designed and demonstrated to work with signals as low as 50 mV and has a maximum measured efficiency of 60%. This allows an increase in the operable distance between the circuit and the radiation source. The system operates with received power as low as -22.6 dBm (5.5 μW), corresponding to 42 meters distance in free-space with a 4 W radiation source. A measured distance of 15 meters is achieved with 1 V DC and a 0.3 μA load current.

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